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CHAPTER 2

Mechanisms and interfacial layers in silicide formation

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2.1 INTRODUCTION

In integrated circuits constraints which lie outside the semiconductor itself are the metallization layers that provide a contact between the semiconductor and the outside world. Processing techniques including diffusion, ion implantation, oxidation, and gettering are sufficiently well developed so that in themselves they often do not limit device performance or degradation. As device size reduces to micron dimensions metallization becomes a major factor.

There are at least two major divisions in metallization schemes: contact to the semiconductor and interconnections between active devices. In the early development of integrated circuits one metal and one process temperature were used to perform both contact and interconnection functions. With the increased complexity of integrated circuits the one metal approach is not adequate and, therefore, different metals, depositions and heat treatments are used for the two different functions. This is a natural development because the requirements for interconnection—good conductivity, resistance to electromigration and corrosion, adhesion—are different than the requirements for contracts. In this chapter we concentrate on the metal–semiconductor contact even though the concepts which we develop may apply to interconnects.

There are two broad classes of metal–silicon reactions: eutectics and compounds (silicides). The Al–Si eutectic system dominated contact metallization schemes in the early years when device dimensions exceeded several microns in depth and lateral extent. The primary requirement of the metal was to make contact to diffused regions.

The major limitation of Al is the relatively high solubility and diffusivity of Si in Al which leads to the dissolution of silicon into aluminium during thermal processing and the consequent erosion of the surface. The erosion is not

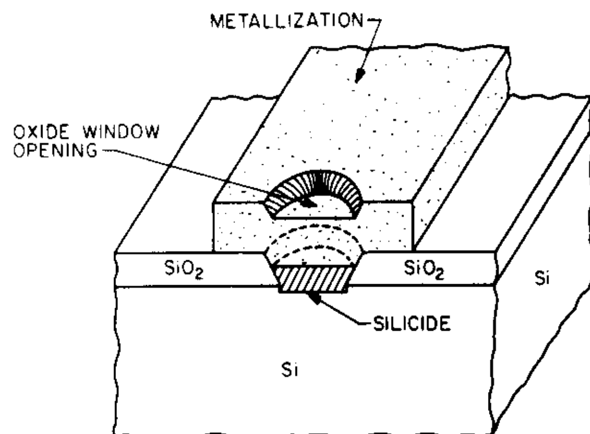

Figure 2.1. Schematic view of a metallization scheme for a silicon device structure. A silicide contact to the silicon is made in the opening etched in the oxide and the upper metallization (Al) layer provides the interconnection with other contact areas

uniform and pits can extend deeply enough in the silicon to short-circuit p–n junction characteristics.

Silicide forming systems offer the advantage that uniform and reproducible contacts are formed at the silicon–silicide interface. There are a wide variety of silicide forming metals and consequently there is a choice of barrier heights on n-type silicon between 0.5 and 0.9 eV. Silicide formation can also be achieved in the temperature range of 200–600 °C, a range that is compatible with device processing technology. A typical metallization scheme, Figure 2.1, involves a silicide and a metal.

In this chapter we are primarily concerned with silicide forming systems. The applications of such silicide forming metals require an understanding of the reactions that occur during thermal processing. For example, impurities such as oxygen can influence the rate of formation of silicides. To determine the amount of silicon consumed for a given metal thickness, one must know the identity and the thickness of the phases which are formed. Electrically active dopants in the silicon can redistribute at the silicon–silicide interface. The interconnect metal may react with the silicide layer necessitating the use of a diffusion barrier. The purpose of this chapter is to present a general view of the physical mechanisms involved in silicide formation.

2.2 OVERVIEW OF SILICIDE FORMATION

2.2.1 Sample preparation and analysis

In the fabrication of devices for integrated circuits the metal layer, typically 500–2000 Å thick, is deposited on a SiO_2 patterned wafer. The metal reacts with silicon in the narrow openings in the oxide layer. For most analytical studies of silicide formation, the metal is deposited directly on an unpatterned silicon wafer. We point out this difference in substrate preparation at an early stage so that the reader may be aware of possible differences in the formation behaviour of silicides in small area and large area structures. For example, for the silicon–Al system formation of pits have been noted at the periphery of the oxide windows.

Generally, the samples are prepared by depositing thin metal films either by electron-gun evaporation under dry vacuum conditions or by sputter-deposition in a well controlled atmosphere. The samples are then annealed either in vacuum or in a controlled atmosphere.

At every stage in sample preparation impurities have been shown to affect silicide formation. We will discuss these effects in a later section (Section 2.4.4), and summarize the general features here. The native oxide layer on the silicon surface can slow or block silicide formation at low temperature. The impurity content of the metal film is also important. Oxygen is known to affect interface sharpness, to retard growth kinetics and to change the sequence of phases that are formed. Consequently the studies of silicide formation under conditions where the films were deposited under poor vacuum conditions are suspect. The same comment can be made for samples annealed under relatively poor ambient conditions. Therefore, the control of impurities will play a role in device reliability as well as in analytical studies of silicide formation.

Various techniques can be used to analyse the samples and the choice depends upon the particular problem to be solved. Generally, it is always useful to use more than one. In compound formation the major interest has been in identifying the various phases formed and to measure their growth as a function of annealing temperature or time. Auger Electron Spectroscopy (AES) combined with ion sputtering[1] and MeV Ion Rutherford backscattering[2] are the two techniques mainly used to obtain growth kinetics and chemical composition. Ion backscattering is a fast technique, is non-destructive, and is so convenient that most silicide kinetic studies have been made with this technique.

The positive identification of the phases is provided by glancing angle X-ray diffraction.[3] The diffraction patterns can be obtained using various systems and again the one chosen depends upon the kind of sample analysed. Transmission electron microscopy (TEM) is used to investigate the microstructure of the silicide layers.

2.2.2 General features

The phase diagrams of metal–silicon couples in silicide forming systems can be represented in a general fashion by the Pt–Si phase diagram, Figure 2.2. There are well-defined phases and eutectic points. The lowest temperature at which a liquid appears is greater than 800 °C and is well above metallization process temperatures commonly used in integrated circuit fabrication. In silicon device processing, silicide formation is truly a solid phase reaction.

The Pt–Si phase diagram[4,5] shown in Figure 2.2 has three eutectic points and six stable phases and at least one metastable phase (not shown). A dramatic demonstration of the existence of all six stable phases is found in bulk diffusion couples.[6] An electron microprobe scan across such a couple is shown in Figure 2.3. The steps in the silicon concentration reflect the change in composition as one traverses from one phase to the next. The steps are relatively sharp and well defined indicating that phases are well separated one from each other.

In terms of semiconductor metallization layers, the distances observed in bulk diffusion samples are enormous. The 100 micron PtSi layer in Figure 2.3 is three orders of magnitude thicker than the 0.1 micron PtSi layer found in Si

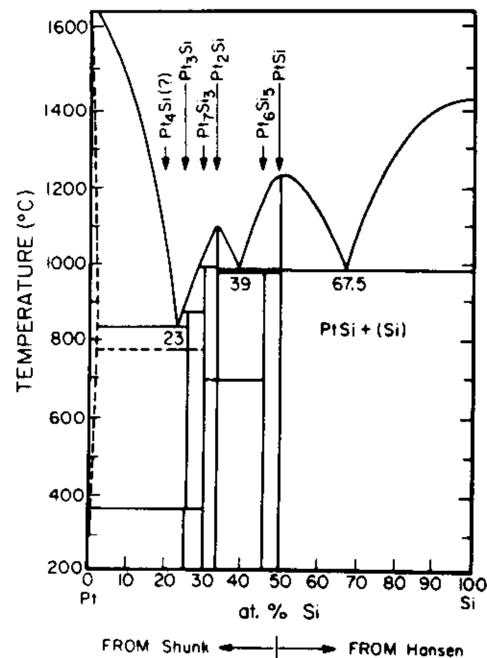

Figure 2.2. The Pt–Si phase diagram as adapted from Hansen[4] and Shunk[5]

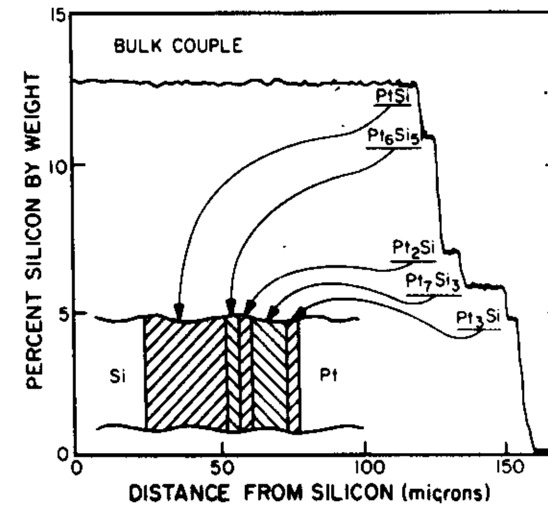

Figure 2.3. Electron microprobe scan across a silicon–platinum bulk diffusion couple annealed at 700 °C for 96 hours (from Claassen[6])

contacts. There are other differences between bulk and thin film systems. In the latter, generally no more than two silicide phases are formed at any stage in the annealing sequence. As shown schematically in Figure 2.4, one phase dominates in the initial stage of silicide formation. At longer annealing times, the width, W, of the Pt_2Si phase increases until all the platinum is consumed. A new phase PtSi develops at the Pt_2Si–Si interface.

At this point we present a model which takes into account the main features of silicon–metal interactions. We use as a reference the near-noble metals and in particular platinum. The extension to other metals is straightforward. In order to form a compound two major conditions should be fulfilled: nucleation and growth.[7] Nucleation and growth require a continuous supply of silicon and metal atoms provided by the reaction between metal and semiconductor.

The reaction is unique in that it occurs between covalently bonded silicon atoms and a metallic material. The presence of high energy phonons required

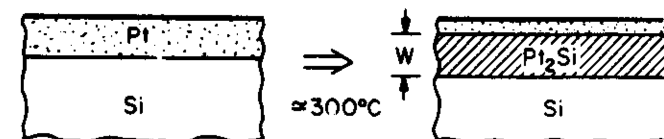

Figure 2.4. Formation of a Pt_2Si layer of thickness W at the interface between platinum and silicon

to break the silicon bonds is not justified at the low formation temperature (≈ 300 °C) of near-noble metal silicides. However, these temperatures are high enough to break the metal bonds. As a mechanism to explain compound formation at low temperatures, it has been proposed that the silicon bonds are softened by an intermixing between the silicon and the metal atoms. A reasonable way to get such intermixing is by interstitial diffusion of metal in silicon.[8] The existence of interstitial nickel atoms at the Ni–Si interface has been shown by channelling measurements.[9] Photo- and Auger electron spectroscopy analysis has indicated the presence of an interfacial layer having electronic properties which do not correspond to those of either the metal or the stoichiometric compound.[10–14] Channelling[15] and electron microscopy[16] also show the presence of an interface layer. A 'metallic-glass' interfacial layer was proposed to account for first-phase nucleation in silicides.[17,18]

In this intermixed layer whose thickness seems to be a few monolayers the Si bonds are weakened and are available for reaction with the metal at low temperature. A continuous supply of silicon and metal atoms is required for compound growth. The silicon atoms are supplied by the reaction at the interfacial layer and the metal atoms arrive at the Si-compound interface by

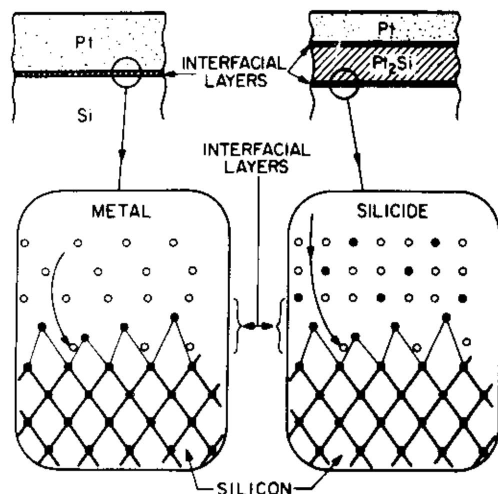

Figure 2.5. Schematics of the interfacial layers formed in Pt–Si and Pt–Pt_2Si–Si structures. The interfacial layer is formed by intermixing of metal and silicon atoms at the interface. The growth of the silicide requires a supply of Pt atoms to the interfacial layer

diffusing through the compound. The sketch in Figure 2.5 shows the main features of the model. The presence of such an interfacial layer has been shown to exist at both the metal–Si and silicide–Si interface.[14]

We believe that the interfacial layer not only is responsible for the low temperature reaction of the system but also has a composition which determines the specific compound which forms.[19] This composition can be adjusted by controlling the supply of silicon or metal atoms. In thin film couples, for example, different phases are formed when the supply of either silicon or metal atoms is reduced by consumption of the silicon or metal layer.[20,21] For the case of Pt–Si couples, the compound which first forms is Pt_2Si. As soon as the metal is consumed, the supply of metal atoms to the interfacial layer decreases and PtSi, the next phase, richer in Si than Pt_2Si, grows.[20] If the silicon layer is consumed before the metal, the supply of silicon atoms to the interfacial layer decreases and Pt_3Si, the next phase richer in metal than Pt_2Si, grows.

The model described above applies to all near-noble metals. It can also be extended to the refractory metals. A pronounced interstitial component is not now required because of the higher reaction temperature of these systems. An interfacial layer must exist and the compound formed must depend on the composition of such a layer. Hence the compound formed will also depend on the supply of either metal or silicon atoms to the interfacial layer. We also assume that the interfacial layer controls the electrical as well as metallurgical properties of the silicide/silicon system.

2.3 PLATINUM SILICIDE SYSTEM

We have chosen to illustrate the concepts of silicide formation by an overall description of the Pt-silicide system. Because of high barrier height of Pt-silicide ($\phi_B \approx 0.87$ eV on n-type silicon), it was one of the first silicides mentioned in applications to Schottky barrier diodes.[22] This system continues to be in popular use in a wide variety of integrated circuit structures. The barrier height of platinum silicide to silicon can be reduced in a controllable fashion by taking advantage of dopant redistribution during silicide formation or by using an alloy combination. One of the attractive features is that it can be formed at a relatively low temperature, and its formation is not strongly sensitive to the presence of a native oxide layer at the Pt–Si interface. It is a stable, reproducible contact.

The platinum silicide contact system is not trouble-free. Impurities like oxygen contained within the film can modify the reaction kinetics and the reaction products. Moreover, aluminium, a common interconnection metal, reacts with the silicide and can degrade the electrical properties of the con-

tact.[23-27] There is broad interest in developing diffusion barriers that will preserve the integrity of the contact.

2.3.1 Phase formation

One can pick up most of the phases indicated in the phase diagram by use of controlled thickness, thin film diffusion samples. Figure 2.6 shows the sequence of phases, a silicide family tree, that are formed in Pt–Si thin film couples.[20] The initial phase which is formed is Pt_2Si. This phase grows until all the metal or silicon is consumed. If the silicon is consumed (left side of Figure 2.6), subsequent phase formation is in the direction of increasingly metal-rich compounds. In the case where the metal is consumed and excess silicon is

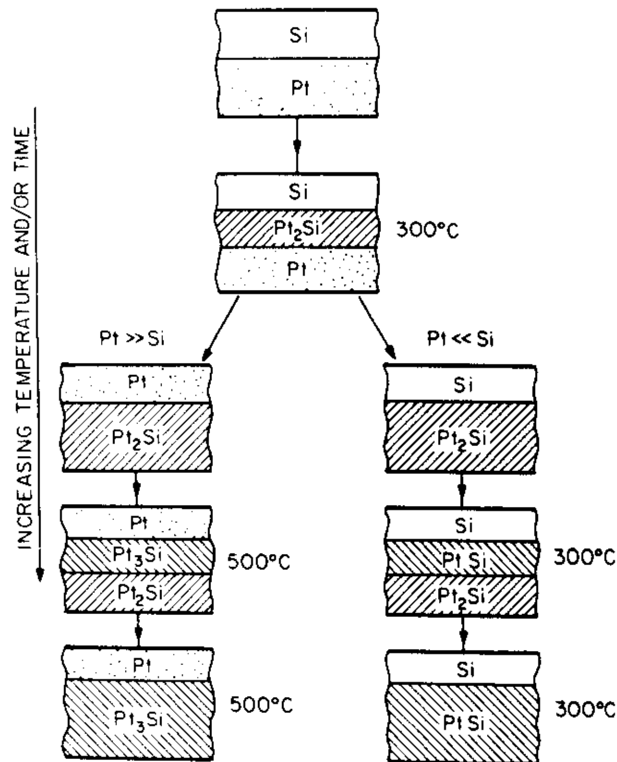

Figure 2.6. Sequence of phases formed in Pt–Si thin film couples. The initial phase formed is Pt_2Si; at longer times or higher temperatures more metal-rich (left side) or more silicon-rich silicides are formed depending on the availability of platinum on silicon. (Adapted from data given by Canali *et al.*[20])

present (right hand side of Figure 2.6), PtSi is formed. This is, of course, the situation found in standard metallization of platinum films on silicon, a progression from Pt to Pt_2Si to PtSi.

The structure of such a 'tree' cannot be explained on the basis of either thermodynamics or kinetics. According to known heat of formation values, PtSi should be formed before Pt_2Si.[7] Diffusion kinetics cannot account for the fact that the second phase forms only after the Pt or Si is consumed. We believe that the phase sequence is determined by the composition at the interface as discussed in Section 2.2.

2.3.2 Phase formation sequence

Rutherford backscattering spectrometry (RBS) is the primary technique used in studies of silicide formation kinetics to measure the thickness and composition of the growing phase.[2,28] In this section we present some RBS spectra to give an indication of the nature of the data. Figure 2.7 shows two superimposed backscattering spectra taken from a sample of platinum deposited on silicon (solid line) and from a sample annealed at 350 °C (closed points).[29] The

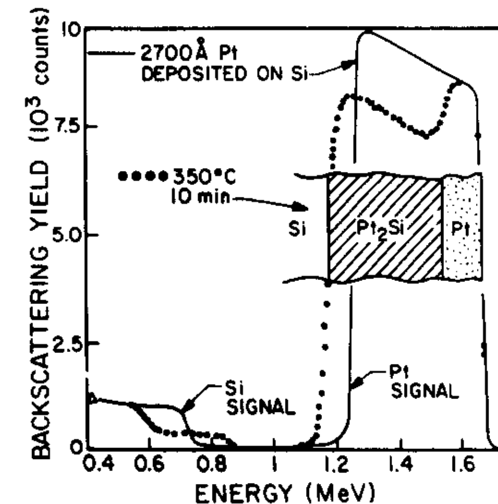

Figure 2.7. Rutherford backscattering spectra for 1.8 MeV ^4He ions incident on a 2700 Å Pt film deposited on silicon (solid line) and on the sample after annealing at 350 °C for 10 min. The backscattering signals from the Pt atoms appear at energies above 1 MeV and those from Si atoms below 1 MeV. The width and height of the steps in the signal indicate the thickness and composition of the silicide (from Canali *et al.*[29])

energy width of the signal from the platinum film indicates a film thickness of 2700 Å. After the sample was annealed, the platinum signal has a step whose height corresponds to platinum in Pt_2Si and whose width corresponds to 400 Å of Pt_2Si. The sharpness of the step indicates that the silicide layers are uniform over the 1.5 mm dimensions of the analysis beam. The location of the step indicates that growth occurs between platinum and silicon.

The first phase, Pt_2Si, exhibits $(time)^{1/2}$ growth behaviour[30] as shown in Figure 2.8. This behaviour is typical of a process limited by the diffusion of one element in the growing compound; platinum is the diffusing species. On the basis of the model, it is necessary to supply platinum atoms at the Pt_2Si–Si interface in order to account for the low temperature of reaction.

When all the platinum deposited on the silicon wafer is converted into Pt_2Si, a new phase PtSi, starts to grow layer by layer at the original Pt_2Si–Si interface. The second phase, as shown in Figure 2.9, also has a $(time)^{1/2}$ growth behaviour. Moreover its growth rate is not substantially different from the previous one. The onset of the second phase does not occur until after all the

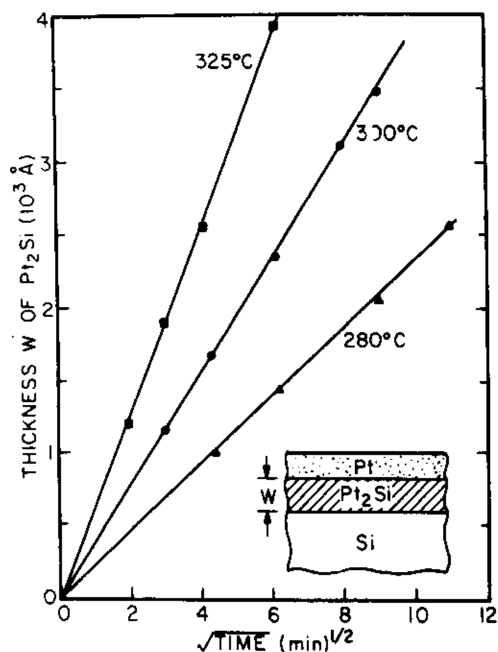

Figure 2.8. The thickness W of Pt_2Si as a function of $(time)^{1/2}$ for samples annealed at different times. The kinetic behavior was determined from Rutherford backscattering spectra similar to those shown in Figure 2.7 (from Ottaviani *et al.*[30])

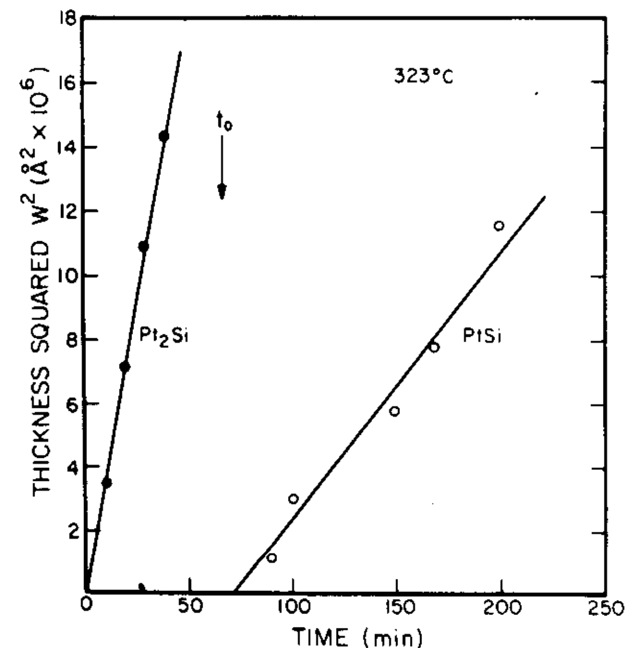

Figure 2.9. The $(thickness)^2$ versus annealing time behaviour of the formation of Pt_2Si and PtSi at 323 °C. The onset of the second phase PtSi occurs at time t_0 when all the Pt has been consumed (from Canali *et al.*[29])

platinum has been consumed in the formation of Pt_2Si. The fact that the second phase, PtSi, grows at about the same rate as the first phase is a clear indication that kinetics alone cannot explain the delay in the formation of the second phase. We attribute the onset to a change in the availability of excess platinum atoms at the Pt_2Si–Si interface. The complete consumption of the platinum film leads to a decrease in the supply of platinum atoms and can trigger a change in composition of interface which in turn allows the formation of a more silicon rich phase. This phase in turn grows and converts Pt_2Si to PtSi.

The delay in the formation of the second phase can be tested directly by annealing samples with different platinum thicknesses together in the same annealing furnace.[31] In samples with thin platinum layers the platinum is consumed at the same rate as in thick samples. Figure 2.10 shows backscattering spectra for a thin (1150 Å) and thick (3570 Å) platinum film annealed at 325 °C. For samples annealed for 5 min, the steps in the platinum signal have the same width indicating that the same thickness of Pt_2Si is formed. For samples annealed for a longer time, the sample with the thick Pt layer continues to show the growth of Pt_2Si. In the thin sample where all the platinum

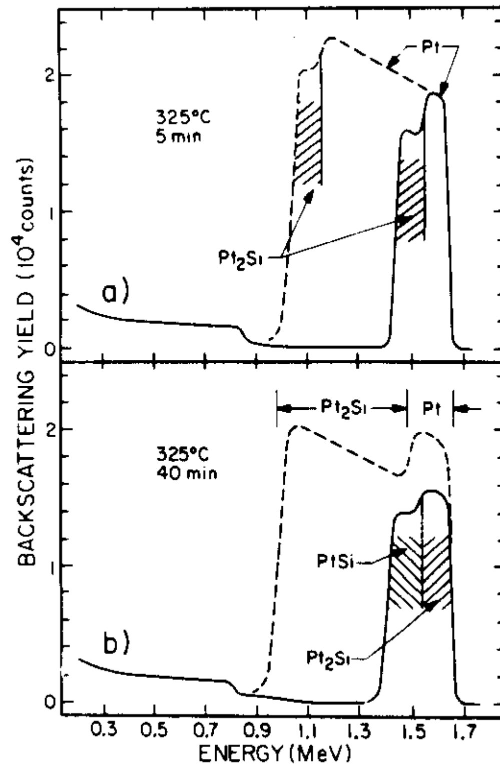

Figure 2.10. Rutherford backscattering spectra for thick (3570 Å) and thin (1150 Å) Pt films on Si annealed at 325 °C for (a) 5 minutes and (b) 40 minutes. The spectra show that the silicide phase sequence is affected by film thickness (from Canali *et al.*[31])

was consumed after a 10 minute anneal PtSi is formed. Consequently, the second phase PtSi forms in thin samples while the first phase Pt_2Si is still growing in the thicker sample. Again this is a manifestation of the influence of the supply of platinum on phase formation.

A more dramatic demonstration of the same phenomena is the decomposition of PtSi.[30] According to our model the second phase PtSi cannot exist in a Pt rich environment. Consequently a sample with platinum deposited on PtSi should form an intermediate phase of Pt_2Si after thermal annealing. As shown in Figure 2.11 for such a sample annealed at 325 °C, platinum reacts with PtSi and forms Pt_2Si at the PtSi–Pt interface. The back interface between PtSi and silicon does not shift indicating that silicon is supplied from the PtSi layer to form Pt_2Si.

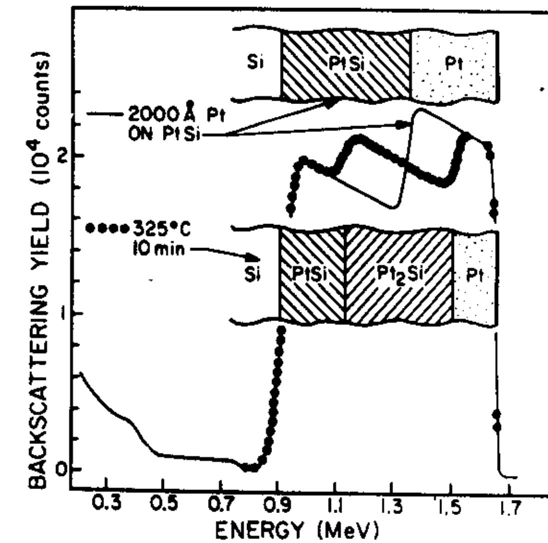

Figure 2.11. Backscattering spectra for 2000 Å Pt films deposited on PtSi (solid line) and annealed at 325 °C for 10 minutes (•). The presence of Pt causes decomposition of PtSi and formation of Pt_2Si at the Pt–PtSi interface (from Ottavani *et al.*[30])

In the experiments described in this section, phase formation was determined by the presence or absence of unreacted platinum. An alternate method of influencing the supply of platinum to the interface is to modify the transport of platinum by introducing a diffusion barrier. As we show in the next section, the incorporation of impurities, oxygen in this case, can establish such a barrier. One can also modify the supply of Pt by controlling the release of the platinum atoms from a matrix containing a mixture of platinum and a second metal. This effect occurs when an alloy of platinum and chrome is deposited on silicon and reacted to form PtSi without the formation of Pt_2Si as an intermediate phase.

2.3.3 Influence of impurities

One of the striking features of the reaction of platinum with silicon is the insensitivity of Pt–silicide formation to the presence of the native silicon oxide layer on the silicon surface. The native oxide layer contains pinholes or weak spots. Platinum can penetrate the weak areas to initiate silicide formation. It was also found[32] that the reaction kinetics were essentially unchanged when comparing silicide formation on two silicon surfaces: one prepared by the standard cleaning procedure using wet etching and other cleaned by sputter

etching and high temperature annealing. Of course, the formation of platinum silicide can be blocked if there is a thick (a few hundred Å) SiO_2 layer at the interface. The presence of intermediate oxide layers such as those grown by a dip in HNO_3 can lead to an irregular interface. The major point, however, is that the native oxide layer which is formed in normal device processing does not have a major influence on silicide formation.

The same situation does not hold for impurities incorporated within the platinum film.[32a,33-36] Oxygen, for example, can slow down the reaction rate and can, at higher concentrations, stop the silicide growth.

The influence of oxygen can be seen directly by comparing the growth behaviour of silicides from platinum films deposited in ultra-high vacuum conditions (10^{-10} torr) or in conventional evaporation (10^{-7} torr) or sputtered deposition conditions. Figure 2.12 plots the $(\text{thickness})^2$ of the initial phase Pt_2Si versus annealing for samples prepared under three different conditions: ultra-high vacuum deposition and anneal,[32a] sputter deposition and vacuum anneal,[29] and sputter deposition, oxygen implantation and vacuum anneal.[33] For all three sets of samples, the initial thickness increases as

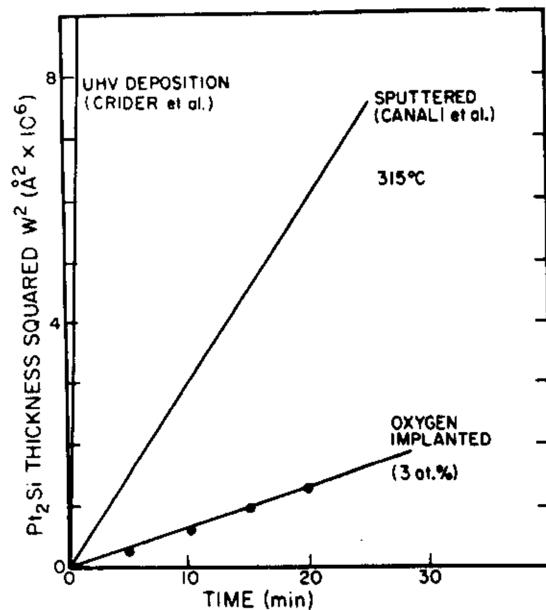

Figure 2.12. The $(\text{thickness})^2$ versus anneal time behaviour of the formation of Pt_2Si at 315 °C. The differences in the growth curves are attributed to the presence of oxygen. The UHV deposited films were annealed *in situ*[32,32a] and the sputtered[29] and ion-implanted[33] samples annealed in vacuum ambients

$(\text{time})^{1/2}$ indicative of a diffusion limited process. The magnitude of the diffusion coefficient is a factor of 60 greater in the UHV films that in the sputter-deposited films.

Auger electron spectroscopy (AES) analysis of the sputter deposited films showed[29] that the oxygen concentration was less than 0.1 per cent. However, the formation of the compound led to an accumulation of oxygen at the Pt_2Si–Pt interface (Figure 2.13). In this case, the concentration of oxygen at the interface was about 0.8 per cent.

In the oxygen implanted sample where the implanted oxygen concentration was about 3 per cent, there was a much greater accumulation of oxygen at the Pt_2Si–Pt interface.[33] In this case the amount of oxygen was sufficient to affect phase sequence behaviour. As shown in Figure 2.14, the growth of Pt_2Si is inhibited and the second phase PtSi starts to grow before all the platinum is consumed. The growth of PtSi consumes the Pt_2Si layer and after 100 minutes at 315 °C, the reaction does not proceed further and leaves unreacted platinum at the surface. The oxygen is contained in the unreacted platinum layer.

The implanted sample represents an extreme case of oxygen contamination. Even so, samples prepared by deposition under 10^{-7} to 10^{-8} torr partial

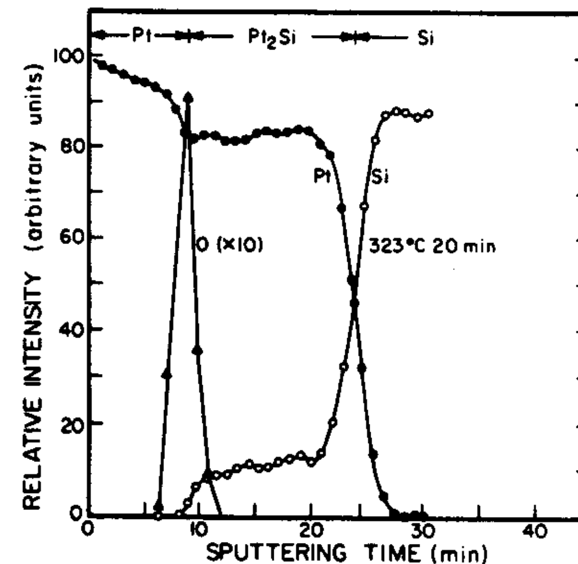

Figure 2.13. The distributions of Pt, Si, and O as determined by Auger electron spectroscopy analysis of a Pt–Si sample annealed at 323 °C for 20 minutes Oxygen accumulates at the Pt–Pt_2Si interface (from Canali *et al.*[29])

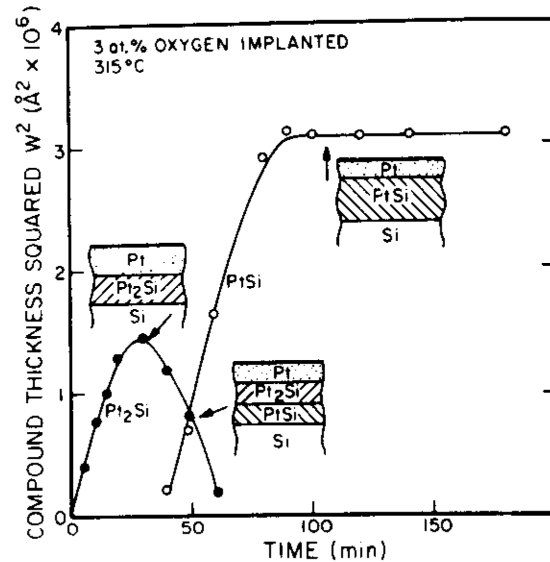

Figure 2.14. The (thickness)^2 *vs.* annealing time for the growth of Pt_2Si and PtSi in an oxygen-implanted sample annealed at 315 °C. The presence of oxygen in platinum influences the phase formation sequence (from Nava *et al.*[33])

pressure of O_2 also exhibited the presence of Pt_2Si, PtSi, and Pt at the same time.[32] The same behaviour was also noted in sputter-deposited samples contaminated with oxygen and aluminium.[34,35] In these samples, accumulation of both aluminium and oxygen occurs at the Pt_2Si–Pt interface.

The effect of the oxygen is two-fold: it slows the growth rate and modifies the phase sequence by changing the supply of platinum to the Pt_2Si–Si interface. The latter feature is shown in Figure 2.15 which depicts the phase sequence for samples with low and high oxygen concentrations. With low concentrations, the sequence observed are in agreement with the predictions of the model presented in Section 2.2. At higher oxygen concentrations, the presence of large concentrations of oxygen at the Pt_2Si–Pt interface limits the Pt supply at the Pt_2Si–Si interface.

Annealing in an oxygen ambient can modify the final structure.[37–40] Analysis of samples[38] annealed in oxygen at temperatures of 400 to 700 °C all showed the presence of a thin layer of platinum separated from the PtSi by an oxide layer. The oxide layer increases in thickness with increasing annealing temperature.

Post-annealing of PtSi films in oxygen ambients leads to the formation of a SiO_2 layer on the outer surface of the silicide film. The presence of this oxide

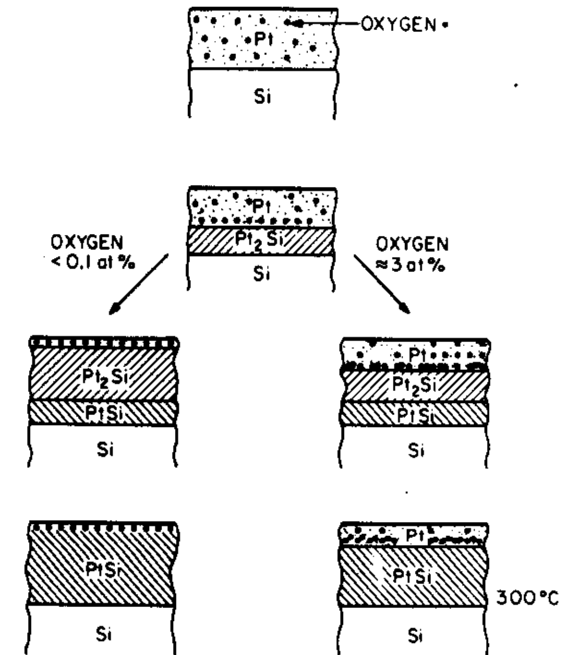

Figure 2.15. Schematic diagram of the influence of oxygen in a platinum film on silicon when the structure is annealed at 300 °C. Oxygen accumulates at the Pt–Pt_2Si interface in the initial stages of silicide growth. For long anneals of the sample containing 3 atomic per cent oxygen, the accumulation of oxygen in Pt stops silicide growth (see also Figure 2.14)

layer has been utilized in some metallization schemes in which unreacted platinum (platinum on SiO_2 adjacent to a window) is etched by aqua regia which does not react with SiO_2.

Any marked deviation from the normal sequence of phase formation is strong indication of the influence of impurities.

2.3.4 Alloys and bilayers

In the previous sections the impurities act as a diffusion barrier to the supply of platinum. Another way to change the supply of platinum is to influence the rate of release from a metal-platinum compound. This was accomplished by depositing alloys of Pt–Cr[41] and Pt–V.[42] Both chromium and vanadium react with silicon to form silicides at temperatures higher (400–600 °C) than the ones necessary to form platinum silicides. Here we use the platinum-rich

($Pt_{90}Cr_{10}$) alloy, as illustration of the behaviour. Annealing at 300 °C produces the formation of PtSi. The platinum is depleted from the alloy leaving a two layer structure with PtSi formed between silicon and the Pt–Cr alloy. There is no evidence for the formation of Pt_2Si. This follows because the supply of platinum is now governed by the depletion of the Pt–Cr alloy.[41] For the Cr-rich alloy the reaction occurs at temperatures above 600 °C and again there was no evidence of Pt_2Si formation.

2.4 PROPERTIES OF SILICIDES

There are a number of reviews which cover silicide formation.[7,43–45] In this section we concentrate on silicide forming systems in which layer by layer growth is observed. By this we mean that the growing silicide front advances uniformly with average irregularities less than a few hundred Å over mm lateral dimensions. These conditions hold for many silicide forming systems, it holds particularly for those that form in the temperature region of 200–600 °C; a temperature region of greatest interest in device fabrication.

In layer by layer growth at fixed processing temperature, the compound thickness increases with annealing time either linearly or proportional to $(time)^{1/2}$. The difference in time dependence is due to the differences in the limiting mechanisms for the growth. A $(time)^{1/2}$ growth rate means that the process is mainly limited by the transport through the silicide layer. The material transported can either be silicon or metal or both at the same time. The $(time)^{1/2}$ rate results from the transport equation and in the increase in transport distance as the silicide becomes thicker. A linear relationship means that the growth is mainly limited by interfacial reactions.

The scheme of layer by layer growth at temperatures generally below 600 °C seems to be followed by most of silicide forming systems. There are exceptions as PdSi, $HfSi_2$, $NiSi_2$, Rh_4Si_5, Rh_3Si_4, $IrSi_3$. These compounds a e formed only after annealing at high temperatures and their appearance seems to be nucleation controlled.[46]

2.4.1 Phase formation

This section is intended as a presentation, primarily in tabular form, of the formation behaviour and properties of the silicides. References are given in the earlier reviews[7,45] from which the tables were adapted. We separate silicide forming systems into the near-noble metals, the transition metals and the refractory metals. This separation is not purely arbitrary but follows the behaviour pattern of silicide formation; for example, the near-noble metals form at temper ıtures around 200 °C, the phase M_2Si is formed first, and the metal is the moving species. In contrast, the refractory metals form the disilicide, MSi_2. The formation temperature is higher (500–600 °C) and silicon is the moving species.

2.4.1.1 Near-noble methods

An overall picture of the reaction of near-noble metals is given in Table 2.1. This table indicates by an asterisk the first compound which is formed, in all cases, M_2Si, as well as the growth rate and activation energy for this compound. As in the case of Pt_2Si, the growth of M_2Si exhibits a $(time)^{1/2}$ dependence, and an activation energy of 1.5 eV is found. For all the metals reported in this table, the first phase forms at low temperatures and the metal is the moving species.

The second phase formed depends upon the relative quantity of material available for the reaction as indicated by the 'tree' in Figure 2.6. For the case of metal films which are deposited on Si substrate, Table 2.1 indicates that monosilicides are formed with a $(time)^{1/2}$ growth dependence and an activation energy near that of the first phase. With the exception of PdSi, the monosilicides form at temperatures near that of the first phase. The phase PdSi forms only after thermal annealing at temperatures around 825–850 °C.

Table 2.1 Silicides formed with near-noble metals.[a] The asterisks indicate the first phase formed

Silicide	Formation temperature (°C)	Activation energy (eV)	Growth rate	Moving species	Density (g cm^{-3})	Heat formation (kcal g atom^{-1})
*Co_2Si	350–500	1.5	$t^{1/2}$	Co	7.42–7.28	9.2
Cosi	375–500	1.9	$t^{1/2}$	—	6.57	12.0
$CoSi_2$	550	—	—	—	4.95–5.3	8.2
*Ni_2Si	200–350	1.5	$t^{1/2}$	Ni	7.35–7.2	11.2–10.5
NiSi	350–750	1.4	$t^{1/2}$	Ni	5.93	10.3
$NiSi_2$	≥750	—	—	—	4.93	6.9
Ni_5Si_2	400	—	—	—	—	10.3
Ni_3Si	450	—	—	—	—	8.9
*Mg_2Si	200	—	—	Mg	1.94	6.2
*Pd_2Si	100–300	1.5	$t^{1/2}$	Pd,Si	8.23	6.9
PdSi	850	—	—	—	7.69	6.9
Pd_3Si	350	—	—	—	—	—
Pd_4Si	400	—	—	—	—	—
Pd_5Si	650	—	—	—	—	—
*Pt_2Si	200–500	1.5	$t^{1/2}$	Pt	11.4	6.9
PtSi	300	1.6	$t^{1/2}$	—	12.6–7.31	7.9
Pt_3Si	400	—	—	—	—	8.1

[a]Table adapted from References 7 and 45.

For nickel and cobalt, the disilicides are listed and indeed these compounds are formed as the end phase in metal films on silicon structures. As implied by the dashes in Table 2.1 there is little known about the formation kinetics of these near-noble metal disilicides.

Thin film reactions in which metals are in excess have been carried out only for Ni, Pd, and Pt. There is progression from the M_2Si phase toward increasingly metal-rich silicides in these systems.

2.4.1.2 *Intermediate metals*

There are a number of silicides whose formation behaviour lies intermediate between the near-noble metal and refractory metals. The importance of these metals because of their adhesion on SiO_2 or to their barrier height warrant their inclusion. The common feature of these materials is that the monosilicide is the first phase formed. For those silicides where the kinetic behaviour has been measured in detail, the growth follows a $(\text{time})^{1/2}$ dependence, and Si is the diffusion species (Table 2.2). All the components have an activation energy somewhat less than 2 eV, with the exception of HfSi.

With metal films on a silicon substrate, the disilicide is the second phase formed. For iridium and rhodium more Si-rich phases can be formed at temperatures above 800 °C.[47,48]

Table 2.2 Silicides formed with intermediate metals[a]

Silicide	Formation temperature (°C)	Activation energy (eV)	Growth rate	Moving species	Density ($g\ cm^{-3}$)	Heat formation (kcal g $atom^{-1}$)
FeSi	450–550	1.7	$t^{1/2}$	Si	6.16	8.8
$FeSi_2$	550	—	—	—	4.54	6.2
RhSi	350–425	1.95	$t^{1/2}$	Si	8.5	8.1
Rh_2Si	400	—	—	—	—	—
Rh_4Si_5	825–850	—	—	—	—	—
Rh_3Si_4	925	—	—	—	—	—
HfSi	550–700	2.5	$t^{1/2}$	Si	16.71	—
$HfSi_2$	750	—	—	—	7.98	—
TiSi	500	—	—	—	4.24	15.5
Ti_5Si_3	550	—	—	—	—	17.3
$TiSi_2$	600	—	—	Si	4.10	10.7
MnSi	400–500	—	—	—	5.82	13.3
$MnSi_2$	800	—	—	—	5.24	2.6
IrSi	400–500	1.9	$t^{1/2}$	—	—	8.0
$IrSi_{1.75}$	500–1000	—	—	—	—	6.1
$IrSi_3$	1000	—	—	—	—	4.6

[a]Table adapted from References 7 and 45.

2.4.1.3 *Refractory metals*

The refractory metals exhibit a common behaviour pattern. The silicides all form at relatively high temperatures (450–650 °C) with the disilicides as the only phase; this is also the end phase which one may predict from the equilibrium phase diagram. Silicon appears to be the predominantly moving species.

These metals are all strongly influenced by the presence of impurities. The presence of oxygen influences the growth kinetics and consequently we cannot state with confidence that the growth follows a linear time dependence or that the activation energy follows the values given in Table 2.3. For example, Nb samples prepared in ultra-high vacuum conditions exhibit a $(\text{time})^{1/2}$ dependence, while a linear relationship has been found on samples prepared under poor vacuum conditions.[49]

2.4.2 Epitaxial silicides

In four cases, the crystalline structure of the silicides has a close match with the underlying silicon substrate and epitaxy has been observed.[50–59] From a technological standpoint such epitaxial silicides provide a high-conductivity layer which could act as a template for epitaxial growth of deposited silicon layers. Silicide layers between crystal silicon regions opens the possibility for device structures with buried interconnects or novel devices such as the metal-base transistor.

Epitaxial layers of Pd_2Si, PtSi, $NiSi_2$, and $CoSi_2$ have been formed. The structure of both $CoSi_2$ and $NiSi_2$ are cubic (CaF_2) with a lattice constant close to that of silicon. The mismatch of the lattice parameter compared to that of Si is 0.5 per cent for $NiSi_2$ and 1.1 per cent for $CoSi_2$. With these silicides, epitaxial growth have been found on ⟨111⟩ and ⟨100⟩ oriented Si crystals.

Table 2.3 Silicides formed with refractory metals[a]

Silicide	Formation temperature (°C)	Activation energy (eV)	Growth rate	Moving species	Density ($g\ cm^{-3}$)	Heat formation (kcal g $atom^{-1}$)
$CrSi_2$	450	1.7	t	—	4.98	7.7
$MoSi_2$	525	3.2	t	Si	6.27–6.3	8.7–10.5
$NbSi_2$	650	2.1	$t^{1/2}$	—	5.66	10.7
VSi_2	600	2.9, 1.8	$t, t^{1/2}$	Si	4.64–4.42	24.3
WSi_2	650	3.0	$t, t^{1/2}$	Si	9.28–9.4	7.3
$TaSi_2$[b]	650	3.7	t	Si	9.06	8.7–9.3
$ZrSi_2$	700	—	—	—	4.86	12.9–11.9

[a]Table adapted from References 7 and 45.
[b]Activation energy and growth rate from J. E. E. Baglin (private communication).

The hexagonal structure of Pd_2Si and the orthorhombic structure of PtSi necessitate use of ⟨111⟩ oriented silicon.

The epitaxial nature of the silicide layer has been investigated by channelling and Rutherford backscattering techniques. These measurements show that high quality epitaxial layers of $NiSi_2$ and Pd_2Si can be formed. The layers of $CoSi_2$ and PtSi have a pronounced spread ($\approx 0.5°$ or greater) in the angular distribution of crystallite axes oriented with respect to the silicon crystal axes.

The epitaxial quality of $NiSi_2$ and Pd_2Si layers improves with increased annealing temperatures. Process temperatures of 700 to 800 °C are used for good epitaxy. The epitaxial quality also depends on layer thickness. For example, with $NiSi_2$ layers greater than 2000 Å, fractures are found.[58]

2.4.3 Stress

The processes of thermal annealing and silicide growth introduce stress.[60,61] Silicides have a different thermal expansion coefficient than silicon and there is a volume difference between the metal–Si and silicide–Si systems.

Measurements of the curvature of silicon wafers have been made using X-ray diffraction techniques.[60] During isothermal annealing of Pd–Si structures, for example, compressive stress increases with time due to volume changes during silicide formation. The stress reaches a maximum when all the palladium is consumed (Fig. 2.16). Further annealing promotes the relaxation

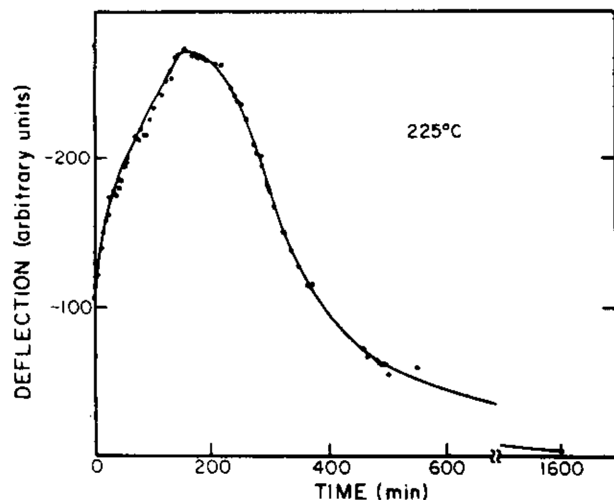

Figure 2.16. The deflection (compressive) of the substrate as a function of time for a 2000 Å Pd film on ⟨100⟩ Si annealed at 225 °C. The stress increases during Pd_2Si formation (from Angilello, *et al.*[60])

of the stress itself. In the example shown, about an order of magnitude longer time is required to relax the stress than to reach the maximum. When the sample is cooled to room temperature a tensile stress now develops. This stress is mainly due to the differences in thermal expansion coefficient of the silicon wafer and silicide film.

This example indicates that the amount and sign (tensile or compressive) of the stress depends upon the thermal history of the sample. Several silicides have been investigated. In all cases stress has been found generally tensile in nature, in the 10–20 × 10^{19} dyn cm^{-2} range.

2.4.4 Influence of impurities

Impurities modify the growth kinetics of silicide formation and the kind of compound formed. We emphasize the role of oxygen, the impurity which has a strong effect on silicide formation. Depending on the location of the impurities in the sample, a broad range of impurity phenomena can be roughly classified as: (1) impurities contained in the metallic layers, (2) impurities introduced during the annealing, (3) impurities at the Si–metal interface, and (4) impurities in silicon.

Impurities contained in the film generally slow down the kinetic behaviour. The influence of oxygen on Pt–Si was described in Section 2.3.3. Disilicide formation in refractory metals is also affected by impurities. For example, in the formation of VSi_2, the presence of oxygen in amounts of 10 per cent can significantly decelerate the reaction.[62] With higher oxygen content in the vanadium films, V_3Si rather than VSi_2 is formed.[63] In terms of the model presented in Section 2.2, we believe that the presence of oxygen modifies the properties of the interface.

Impurities can also be introduced in the film during thermal annealing and a strong effect on compound formation has been found. As an example, nickel behaves differently if the annealing is performed in vacuum or in an atmosphere with some oxygen.[31] Figure 2.17 shows the backscattering spectra of a 1700 Å film on a (100) silicon substrate before and after annealing at 325 °C in a vacuum furnace (10^{-6} torr) or in commercially pure flowing nitrogen. While vacuum annealed samples show the normal evolution (Ni_2Si forms first, then NiSi when all nickel is reacted) in samples annealed in nitrogen (Figure 2.17(b)) the coexistence of Ni_2Si, NiSi, and unreacted nickel was observed. This behaviour strongly suggests that oxygen diffuses through the nickel to the silicide–metal interface and modifies the supply of nickel to the Ni_2Si–Si interface. In a related experiment, it was found that oxygen implanted in a nickel film influences the sequence of phase formation and that oxygen accumulates at the Ni_2Si–Si interface.[64] Analysis by X-ray photoelectron spectroscopy showed the oxygen was bonded to silicon at the silicide–Ni

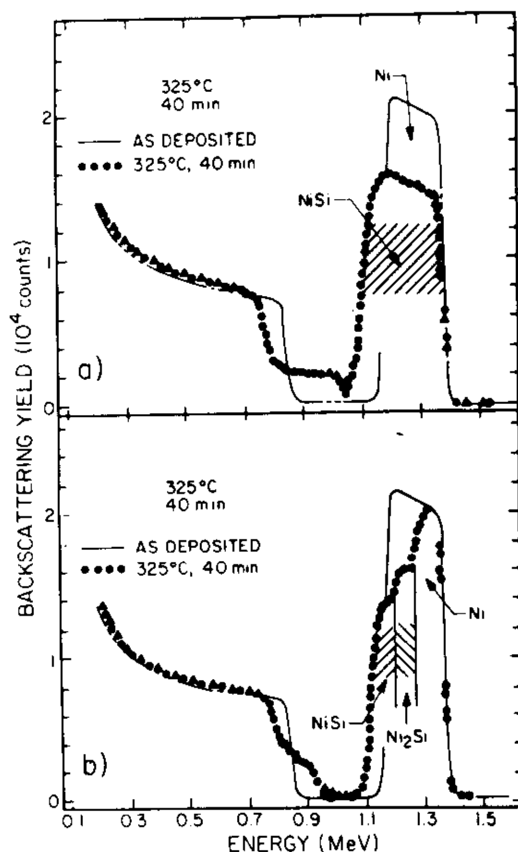

Figure 2.17. Rutherford backscattering spectra for a 1700 Å Ni film on silicon annealed for 40 min. at 325 °C in (a) vacuum ambient or (b) flowing nitrogen. Impurities introduced during annealing affect the silicide phase sequence (from Canali *et al.*[31])

interface. We believe that the build-up of the oxide layer forms a diffusion barrier.

In the case where one anneals a silicide in an oxygen ambient, SiO_2 can be formed on top of the silicide. As shown in Figure 2.18(a), SiO_2 is formed on WSi_2 after processing in steam at 1000 °C.[65,66] Radio tracer measurements of the growth of SiO_2 on $CoSi_2$ at 1000 °C show that the self-diffusion coefficient of Si in the silicide layer is very high at 1000 °C.[67] The transport of Si in SiO_2 is very low at 1000 °C so that the growth of SiO_2 occurs at the silicide–oxide interface.

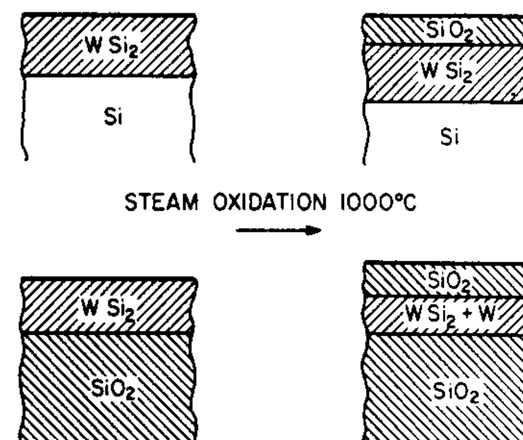

Figure 2.18. Schematic showing the formation of SiO_2 on sputtered deposited WSi_2 annealed at 1000 °C in steam. Formation of tungsten-rich silicides occurs in samples deposited on an SiO_2 substrate

The disilicide structure can be maintained as long as there is an adequate supply of silicon. Depending upon annealing conditions and sample configuration, metal-rich silicides can be formed during oxidation. If the supply of silicon from the substrate is not adequate, the incorporation of silicon in SiO_2 will deplete the amount of silicon in the silicide layer leading to the growth of more metal-rich silicides. For example, with WSi_2 deposited on SiO_2, oxidation causes the formation of W_5Si_3 (Figure 2.18(b)).

The impurities contained at the metal–silicon interface affect silicide formation by decreasing or inhibiting the silicon supply. An extreme case is when the metal is directly deposited on SiO_2.[62,68–70] After heat treatment, various cases can be observed: no reactions as in the case of Au; a metal oxide as in the case of Al, Pb, and Sn, and metal silicide and metal oxide as in the case of refractory metals. The influence of SiO_2 on vanadium silicide formation is shown in Figure 2.19. The disilicide is formed from vanadium on silicon but V_3Si and VO_x are formed if the substrate is SiO_2.[62,68] In the latter case, higher processing temperatures are required and vanadium rather than silicon is the moving species through the V_3Si layer.[71]

Impurity redistribution within the silicon substrate can occur during silicide formation. Dopants such as arsenic or antimony introduced into silicon by ion implantation before metal deposition can accumulate at the silicide–Si interface during silicide growth.[72] The accumulation of dopant atoms at the interface leads to a change in the electrical properties of silicide–silicon contacts. The concept was used as a method of lowering the barrier height of PtSi–*n*-Si Schottky barrier diodes.[73]

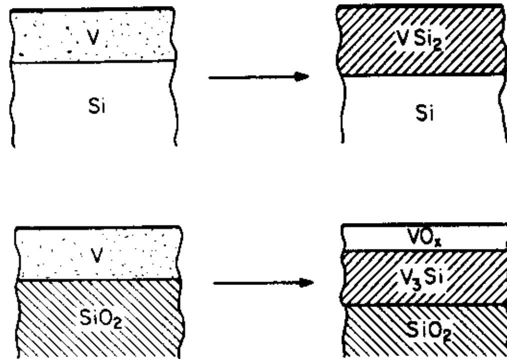

Figure 2.19. Schematic diagram of silicide formation in vanadium films deposited on Si and SiO_2. With a silicon substrate, VSi_2 is formed (Si is the moving species) and with SiO_2, V_3Si is formed (V is the moving species)

2.5 ALLOY AND BILAYER SILICIDES

It must be apparent to the reader that with the possible exception of impurity effects there is a clear understanding of the empirical behaviour of single metal silicide formation. An obvious extension of past experience is to consider the application of multilayer or alloy metal films in order to meet the more stringent requirements imposed by increasingly complex integrated circuit design. The shrinkage of dimensions toward one micron lateral and submicron depth dimensions provides a strong push for development of more sophisticated metallization schemes.[74] One requirement is to have a uniform silicide contact that requires only a limited consumption of silicon. This cannot be achieved under production conditions by the deposition of hundred Å layers. The thinness of such layers and the difficulty of obtaining uniform and reliable coverage over a wafer virtually precludes their use. Another requirement is to provide a diffusion barrier between the silicide contact and the interconnect metallic layer.

An ideal structure is shown in Figure 2.20. Two-metal silicides can be used to achieve such a structure; one approach is to deposit a sequence of layers of metal forming silicides (bilayers), and the other approach is to codeposit a mixture of metals (alloys). There are so many possible metal combinations that for the convenience of the reader we consider only two broad categories; the near-noble metal silicides, Ni, Pd, Pt, and the refractory metal silicides of the group IV, V, VI metals, Ti, V, Cr, W, etc.

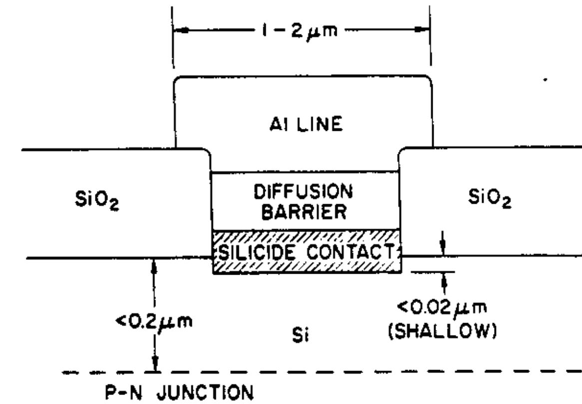

Figure 2.20. Cross-sectional view of a shallow silicide contact with a diffusion barrier between the silicide and the aluminum interconnect line (from Tu *et al.*[41])

2.5.1 Alloy silicides

The alloy systems investigated to date have been obtained by either co-deposition using dual electron-guns or sputter deposition onto a silicon wafer. The systems have been combinations of either near-noble and refractory metals,[41,42,75,76] as PtCr, PdV, and PtV or two refractory metals as TiW.[77]

Although the details of reaction temperatures and kinetics can be different, the general behaviour is the same for all the near-noble and refractory metal combinations.[42,75] We illustrate this behaviour pattern by using Pt-rich ($Pt_{90}Cr_{10}$) and Cr-rich ($Pt_{10}Cr_{90}$) alloys.[41] For the Pt-rich, $Pt_{90}Cr_{10}$, sample the formation of platinum silicide was detected at 300 °C; the amount of PtSi increases with annealing up to 600°. The platinum is depleted from the alloy leaving a two layer structure; a layer of PtSi next to the silicon and an outer layer of Cr enriched PtCr alloy. For the Cr-rich alloy, $Pt_{10}Cr_{90}$, there is no structural evidence for silicide formation for annealing at 400 °C for up to four hours. As expected, there are large reactions at annealing temperatures of 450 °C since single layers of Cr form $CrSi_2$ at 450 °C.

The results of alloy formation in the PtCr system are bounded between the reaction temperature of Pt (around 200 °C) and that of Cr (450 °C). A wider temperature range is obtained with a refractory metal, V, which reacts with silicon at higher temperature, 600 °C. In all these alloy systems investigated, annealing up to temperatures as high as 800 °C has not resulted in a ternary system, but rather in phase separation with the near-noble metal silicide next to the silicon and the refractory disilicide formed near the surface.

Ternary compounds have been obtained by reacting at 700–800 °C films of W-30 atomic per cent Ti deposited by RF sputtering on silicon substrates.[77]

The results show a layer by layer growth of a $Ti_xW_ySi_2$ compound without phase separation. Further systematic work is required in alloy systems made by refractory materials before a general picture can be presented.

2.5.2 Bilayer silicides

On the basis of the reaction temperature of the metals, the bilayers can be classified in three main categories, shown in Figure 2.21. The metals are indicated only for simplicity in the discussion and similar results have been obtained in other systems. In the systems investigated the only changes observed are in the reaction temperature, but not the general behaviour.

In the case of bilayers constituted by near-noble metals[78,79] heat treatment at low temperatures produced the formation of the metal-rich silicide compound Ni_2Si. The other metal does not react with Si even when all the nickel is completely consumed. At higher temperatures platinum penetrates by grain boundary diffusion and forms a silicide at the interface between silicon and the Ni_2Si compound. One example of such grain boundary diffusion is shown

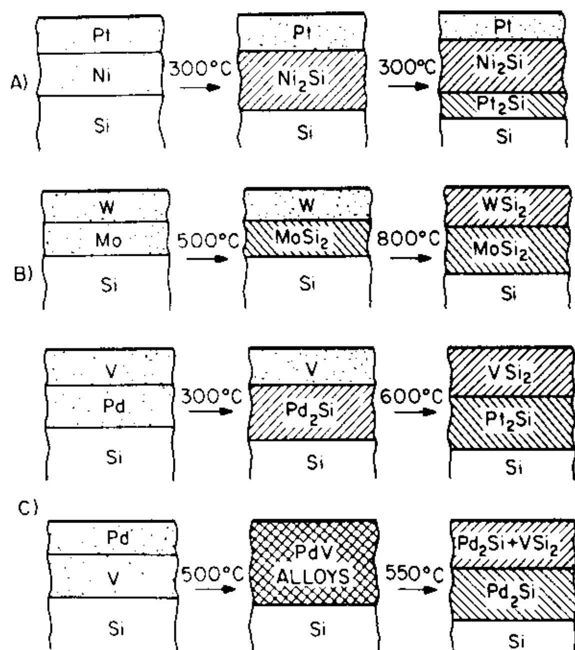

Figure 2.21. Composite diagram of silicide formation for bilayers composed of (a) near-noble metals (Pt–Ni), (b) refractory metals (W–Mo), (c) near-noble and refractory metals (V–Pd)

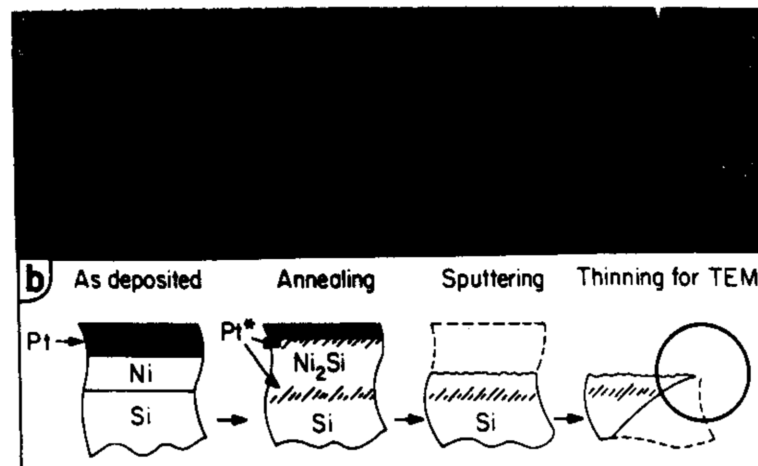

Figure 2.22. (a) TEM micrograph of sample with Pt deposited on a Ni film on Si and annealed at 350 °C for 20 minutes, (b) sample preparation procedure. The TEM view shows platinum (dark regions) decorating the grain boundaries in Ni_2Si (from Finstad[79])

in the TEM micrograph of Figure 2.22. The schematic shows the sample preparation. The cell-like structure indicates that platinum decorates the grain boundaries of Ni_2Si.

These results can be interpreted on the basis of the model for compound formation outlined in Section 2.2. It is not surprising that Ni reacts first since Ni is in contact with silicon and the formation mechanisms of Ni_2Si and Pt_2Si seem to be the same. In the near-noble systems the metal is the main moving species. After the nickel has been consumed, further reaction needs more metal atoms at the silicon surface, atoms which are provided by interstitial diffusion of platinum.

The details of the transformation at longer times and higher temperatures varies from sample to sample. Above 700 °C the distribution of Pt and Ni becomes homogeneous. This result along with X-ray diffraction data indicates the formation of ternary silicides.

A bilayer of two refractory metals behaves in a different way. For Mo deposited on Si and W deposited on Mo (Figure 2.21(b)), the formation of $MoSi_2$ is completed after 500 °C as predicted from results with Mo only.[80,81] The tungsten film remains intact without reacting with the molybdenum film. When the temperature is increased to 800 °C, the tungsten film is transformed to WSi_2. With further anneal up to 1000 °C, there was still clear separation of the $MoSi_2$ and WSi_2 phases without evidence for ternary formation.

The results with Mo–W system are not surprising because $MoSi_2$ is formed at temperature below WSi_2. More insight was found from the work with Ta-V

bilayers, where vanadium reacts at higher temperatures than tantalum does.[82] The same behaviour of phase separation and kinetics of formation were found irrespective of the order of deposition. The only difference is that the reaction temperature is lower when vanadium is in contact of silicon and higher with tantalum. These results agree with the fact that silicon is now the moving species and the refractory metals tend not to interdiffuse. Consequently, no layer reversal can be expected as was found in the case of near-noble metal bilayers.

The intermediate case between the near-noble and the refractory metal bilayer, is provided by a near-noble refractory metal bilayer (Figure 2.21(c)). The reactions of structures of Pd and V with Si are governed by the low formation temperature of Pd_2Si with palladium as the moving species and with the high formation temperature of VSi_2 with silicon as the moving species.[75] The simplest case is that of the Si–Pd–V structure in which uniform layers of Pd_2Si are formed first followed by a higher temperature formation of uniform layers of VSi_2. With the bilayer structure Si–V–Pd higher temperatures are required. The first step provides intermixing between palladium and vanadium. Later Pd_2Si is formed in contact with the underlying Si and at even higher temperatures a non-uniform structure of Pd_2Si and VSi_2 is formed in the outer layer. In these structures, the tendency is to form an alloy between the V and Pd and then to release the Pd from the Pd–V alloy to form Pd_2Si.

A major problem with the use of silicides as Schottky barrier contacts is the degradation due to the reaction of the interconnect metallization, usually Al, with the silicide.[23–27,83–86] It has been shown that the barrier height of PtSi decreases 0.2 eV when the Al contact is heated to 610 °C for 30 min.[23]

In order to prevent degradation of the Schottky contact it is necessary to prevent a reaction between PtSi and Al. One method to accomplish this is to interpose a sacrificial layer between PtSi and aluminium. This concept of the use of a sacrificial layer is an extension of the near-noble refractory metal bilayer. An example of such sacrificial barrier is to use chromium as a barrier to the interaction of Pd_2Si with aluminium.[85] In such samples chromium reacts with Pd_2Si to form $CrSi_2$ and chromium reacts with aluminium to form a Cr–Al compound. As long as a layer of unreacted chromium is present the integrity of the Pd_2Si layer on the silicon substrate is preserved. In this case, the lower temperature reacting layer is in contact with the silicon and forms a silicide at relatively low temperatures. At higher temperatures, the high temperature silicide and Al–metal compounds are formed. This concept was also shown directly with a Pt–Cr alloy layer in contact with Al.[41] The outer chromium layer preserves the stability of PtSi contact for up to 1 hour at 450 °C. The contact degraded after annealing at 500 °C for 1 hour.

If the metallization system must go through metallization procedures above 450 °C, other barriers must be considered. One possibility is to use a bilayer or alloy of tungsten with platinum. For example, it has been shown that WSi_2 can be formed at 750 °C on samples formed by depositing thin film of tungsten on PtSi.[83,84]

There are other approaches to the development of diffusion barriers that can be used to prevent reaction between the Schottky barrier contact and Al.[87] We have described the use of sacrificial barriers. Alternative approaches involve the use of inert barriers such as TiW[24] or TiN.[88]

2.6 ION MIXING AND LASER ANNEALING

The previous sections were concerned with silicide formation under standard furnace annealing conditions. There are two recent developments, ion beam mixing, and laser annealing, which also have been used to promote silicide formation. Both involve the deposition of energy in the submicron region and rapid heating and cooling in the region where the energy is deposited. The advantages of such directed energy deposition techniques are that the silicide can be reacted in a localized region and that the silicides can be formed without heating the entire wafer. Beyond these generalities, the two techniques are sufficiently different so that we will discuss them separately. Although these techniques have not yet been used in integrated circuit fabrication both offer unique capabilities which may be exploited at a later time.

2.6.1 Laser annealing

We use the term laser annealing to denote both laser and electron beam annealing.[89,90] To date, there has not been any direct evidence to indicate a major difference in results achieved for the equivalent amounts of power absorbed in the sample. Both are basically short-duration, near-surface heating processes. There are two regimes: in one the energy is sufficient to melt the silicon and silicide formation occurs during the solidification of a molten, metal–Si mixture; in the other lower energy pulses are used and silicide formation occurs in the solid phase. With very short pulses of about 10^{-7} sec duration (typical of Q-switched lasers), the sample is heated for such a short time that silicides do not grow in the solid phase. In single-pulse Q-switch lasers, high energy pulses are required to form a molten layer. With longer pulses of 10^{-2} to 10^{-3} sec duration (typical of scanned CW beams), the sample is heated for a sufficiently long time so that silicides can be formed in the solid phase. Consequently, the two regimes, liquid phase and solid phase, are often associated with the type of laser, Q-switched or CW.

Well-defined silicide phases have been formed by scanned CW-laser and electron beams.[91,92] With electron beams both near-noble and refractory metals were formed. The results indicate that silicide formation with scanned CW beams is equivalent to that achieved by thermal annealing but at higher

temperatures and shorter times than one would use in conventional furnace processing.

With Q-switch laser irradiation, melting produces a mixture of metal and silicon over the melt depth.[93-99] Upon termination of the pulse, cooling occurs and the liquid–solid interface moves to the surface. In all cases where crystalline layers are formed, laterally non-uniform (cellular) structures are formed with columnar regions of silicon surrounded by thin walls of silicide. The structure is shown on the right side of Figure 2.22 (the silicide regions appear black in the micrographs). The process is shown in the left side of Figure 2.22. Upon solidification the metal is pushed away from the solid–liquid boundary and accumulates in the liquid until the solidification occurs. The cellular formation follows the classical description of segregation and constitutional super-cooling.[100]

The non-uniform structure of the solidified layer is reflected in the presence of multiple silicide phases in Q-switch laser annealed systems.[98] Laser irradiation of Pd layers on Si led to the formation of Pd_5Si, Pd_4Si, Pd_3Si, Pd_2Si and PdSi. A similar collection of phases was found in the Pt–Si system.

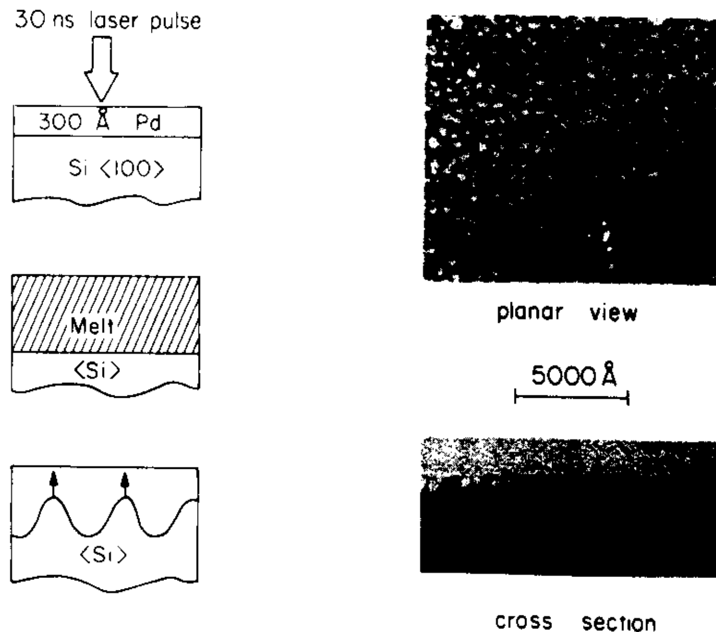

Figure 2.23. Schematic (left side) and TEM micrographs of a 300 Å Pd film on silicon irradiated with a 30 ns Nd–Yag laser. In the TEM view the dark areas are platinum. The formation of the cellular structure is attributed to constitutional supercooling of the Pt–Si molten layer

2.6.2 Ion beam induced silicide formation

The penetration of energetic ions through the metal–semiconductor interface leads to strong interfacial reactions.[101,102] In near-noble metals on Si, ion mixing leads to the same phase, M_2Si, found in thermal annealing.[102,103] For Pt–Si systems, the growth of Pt_2Si is proportional to (ion dose)$^{1/2}$ as shown in Figure 2.23. This result indicates that the mixing process is similar to radiation-enhanced-diffusion. The dependence of the silicide thickness on ion mass is correlated directly with the amount of energy deposited in atomic collisions. At higher ion doses, when all the metal film is consumed in the formation of M_2Si, ion beam mixing can lead to the formation of a more silicon-rich phase[104] or can produce an amorphous layer.[105]

With refractory metals, implantation at temperatures above room ambients is required to form well-defined, crystalline, disilicide phases.[106-108] The mixing process is temperature dependent as shown in Figure 2.24 which plots the amount, Q, of Si atoms intermixed with the Cr layer as a function of reciprocal temperature. At low temperatures, mixing is dominated by dynamic collision processes (cascade mixing) and hence is not strongly temperature sensitive. In this regime, mixing produces graded interfaces. At higher temperatures, radiation-enhanced-diffusion becomes dominant and, similar to thermal annealing, layer by layer growth of crystalline silicides are formed (Figure 2.25).

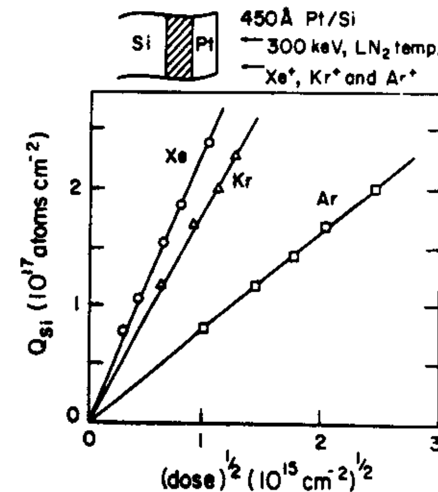

Figure 2.24 The amount of Si, Q_{Si}, in an intermixed PtSi layer versus ion (dose)$^{1/2}$ for 300 keV ions implanted through a Pt film on Si. The amount of Si increases as (dose)$^{1/2}$ (from Tsaur *et al.*[102])

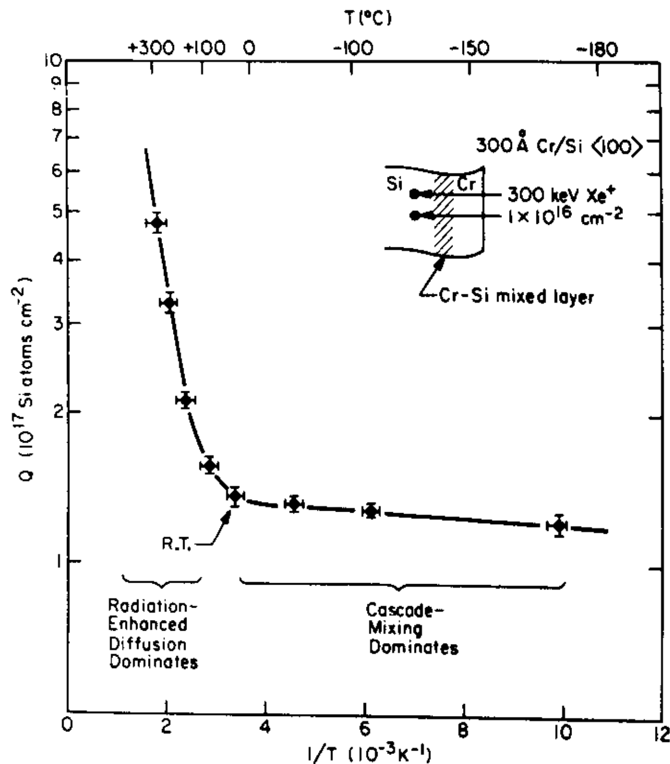

Figure 2.25 The amount of Si, Q, in an intermixed CrSi layer versus reciprocal temperature for a Cr film on Si bombarded with 300 keV Xe ions. To a dose of 1×10^{16} ions cm^{-2}. At low temperatures, cascade mixing dominates and at higher temperatures, radiation enhanced diffusion is dominant (from Tsaur[108])

It is unlikely that ion-beam mixing will be used directly in forming metal–semiconductor contacts due to the radiation damage produced in Si by the ions which penetrate the metal–semiconductor interface. However, ion mixing might be applied to the interconnect metallization to improve adhesion or to form special silicide phases.

2.7 ELECTRICAL PROPERTIES

In the previous sections we have been mainly concerned with the metallurgical properties of silicides. The importance of silicides in integrated circuits is associated with their electrical properties. The major use of silicides in device structures has been to provide a contact, either ohmic or rectifying. Due to the requirements imposed by VLSI, it has been proposed to use silicides as

interconnects.[109,110] In this usage, the resistivity rather than the barrier height of the silicide is the key feature.

2.7.1 Metal–semiconductor contacts

The most important property of a metal–semiconductor interface, from the standpoint of electronic device applications, is the potential barrier or barrier height between the Fermi level and the majority carrier band edge of the semiconductor at the interface. The barrier height plays a central role in the electrical properties of the metal–semiconductor contact because it determines the current–voltage characteristics of the structures.[111–113]

A large number of investigations on barrier heights are reported in the literature covering many silicide-forming systems. On the other hand, the theoretical understanding of metal–semiconductor contacts lags well behind experimental findings.

Recently, the availability of ultra-high vacuum systems and the development of new techniques of surface analysis allows a re-examination of the physical mechanisms involved in Schottky barriers. The most striking result is the discovery that the barrier height is already established if a few monolayers of a metal is deposited on silicon. Most of these metals produce an interfacial layer having properties different from the pure compound and the pure metal. These findings shifted the interest of researchers from bulk silicide properties to interfacial layer properties.

The barrier height is determined by the density of interface states in the energy gap of silicon, in agreement with previous models, and these states are due to the interfacial layer between silicon and silicide. The position of these interface states is determined by the metal and their density can depend upon the interfacial composition.

Figure 2.26 shows the values of the barrier height measured in a SiPt system after annealing at various times and temperatures.[114] The phases quoted here have been identified by backscattering techniques and X-ray diffraction measurements. The main feature of these results is that the barrier height does not depend significantly upon the compound which is formed. Similar results were found in the Ni-silicide systems.[115]

These results indicate that (i) platinum reacts with silicon and forms an interfacial layer even if the deposition is done on substrates held at about 85 °C; and (ii) if the composition of the interfacial layer changes, the corresponding change in the density of states is not enough to produce an appreciable effect on the position of the Fermi level.

The dependence of the barrier height measured in various silicide forming systems on n-type silicon is plotted in Figure 2.27 as a function of the 'eutectic temperature' determined from phase diagrams.[116] The eutectic temperature is used as a medium to characterize the properties of the interfacial layer. The

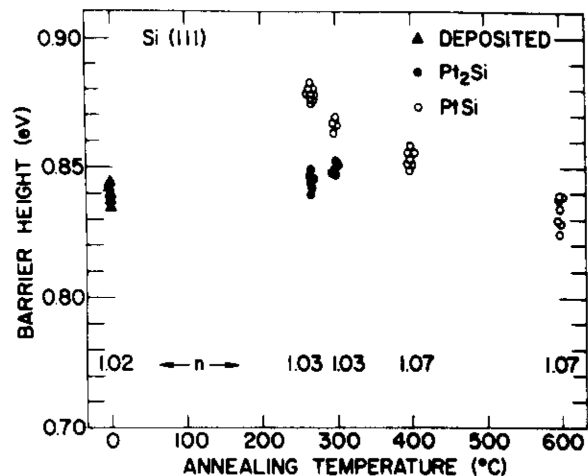

Figure 2.26. The barrier, ϕ_B, in eV versus process temperature for Pt films deposited on silicon. The phases indicated in the figure have been identified by X-ray diffraction and Rutherford backscattering (Ottaviani *et al.*[114])

correlation shown in Figure 2.26 is a further proof of the existence of the interfacial layer. The barrier height and hence the position of the surface states in the gap depends upon the kind of metal in the interfacial layer.

In Figure 2.27, we have correlated the barrier height with eutectic temperature to show the importance of the interfacial layer. Another approach, also based on the concept of an interfacial layer, is to correlate the barrier height with the geometric mean of the barrier heights of the constituents.[117] This correlation also gives a reasonable fit between measured and calculated values with the exception of PtSi and RhSi.

Actual devices are generally made in an environment which is more difficult to control than that in a laboratory where ultra-high vacuum systems and sophisticated techniques can be used to produce and characterize the device itself. Undesirable effects, as for instance non-uniform interreactions[118,119] can occur, leading to unexpected behaviour. Moreover several aspects of silicide formation, such as stress, are still under investigation. These can also affect the properties of silicon–metal contents even if the devices are prepared in the best conditions.

Other sources for non-uniform contacts come from the penetration of Al through the silicide. The non-uniform interaction produces regions in the contact area which modify the electrical properties of the whole structure. Recently the prob'ems of non-uniform interactions have been investigated.[118,119] It has been shown that by coupling I–V and C–V characteristics it could be possible to gain more insight on the uniformity in the contact area.

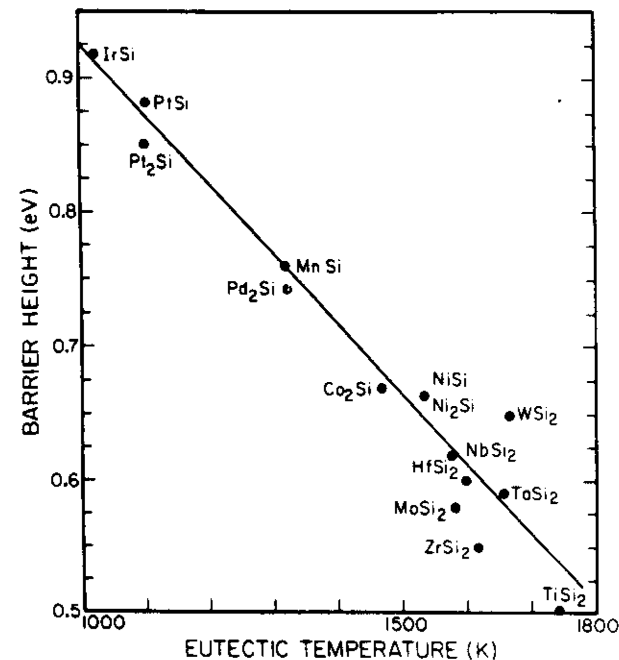

Figure 2.27. The barrier height, ϕ_B, in eV versus eutectic temperature for silicide forming systems (from Ottaviani *et al.*[116])

Moreover the results obtained can explain why barrier heights measured with C–V technique are different than the ones obtained with I–V measurements.

2.7.2 Silicide resistivity

Silicides play an increasingly important role as interconnects as device dimensions on integrated circuits are reduced. In this application the resistivity rather than barrier height becomes the important issue. The change in emphasis will lead to an increase in the number of studies dealing with electron transport properties of silicides. One may anticipate that stress and crystallite grain size as well as the silicide phase will be important parameters. It will be important to investigate the correlation between electrical and structural properties. A detailed investigation of the electrical properties of Pd_2Si has been reported.[120] Electron concentration and mobility have been measured over a wide temperature range.

Low resistivity values, about 25 $\mu\Omega$ cm, were found for $TiSi_2$ in studies of titanium on polycrystalline silicon and of cosputtered (titanium plus silicon) film on SiO_2 plus polycrystalline silicon.[121] The resistivity, stress, and surface

Table 2.4 Silicide resistivities[a,b]

Silicide	Sample preparation	Annealing temperature (°C)	Film resistivity (μΩ cm)	Bulk resistivity (μΩ cm)
$TiSi_2$	Metal on polysilicon	900	13–16	123
	Alloy	—	25	—
$ZrSi_2$	Metal on polysilicon	—	35–40	160
$HfSi_2$	Metal on polysilicon	—	45–50	—
VSi_2	Metal on polysilicon	800	50- 55	9.5
$NbSi_2$	Metal on polysilicon	800	50	6.3
$TaSi_2$	Metal on polysilicon	900–1000	30–70	8.5
	Alloy	900–1000	50–55	—
$CrSi_2$	Metal on polysilicon	700	600	1500
$MoSi_2$	Alloy	1000	50–100	20–22
WSi_2	Alloy	1000	35–100	33.4
FeSi	Metal on polysilicon	500	150–200	—
$FeSi_2$	Metal on polysilicon	700	>1000	—
RhSi	—	—	70–80	—
$CoSi_2$	Metal on Polysilicon	900	18–20	—
	Alloy	—	25	—
PtSi	Metal on polysilicon	800	28–35	—
PdSi	Metal on silicon	—	18	—

[a]Adapted from the format used by S. P Murarka.[122]
[b]Additional data from S. Zirinsky, IBM Research Center [123]

appearance had different thermal behaviour in the cosputtered (Ti + Si) and deposited (Ti) systems in the temperature range measured. Such studies are required in other silicide-forming systems. It is also important to investigate possible correlation between electrical and structure properties.

We present here in tabular form, Table 2.4, the electrical resistivity measured in thin film silicides compared with the values obtained in bulk samples.[121] The table contains also information on sample preparation and annealing conditions.

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