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THIRD COLLEGE ON MICROPROCESSOR-BASED REAL-TIME
CONTROL - PRINCIPLES AND APPLICATIONS IN PHYSICS
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GENERAL PURPOSE INTERFACE

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These are preliminary lecture notes, intended only for distribution to participants.

General Purpose Interface

(24 bit parallel digital I/O interface)

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General Purpose Interface

(24 bit parallel digital I/O interface)

Features:

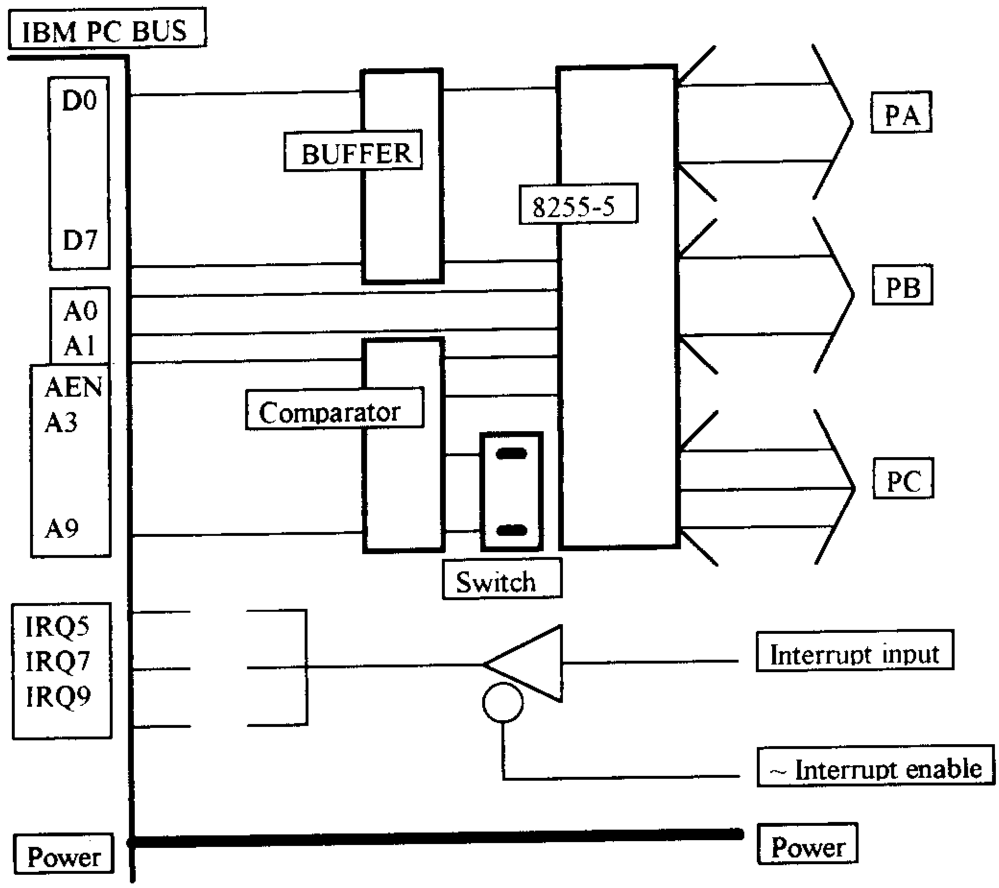
- 24 TTL digital I/O lines, organized into 8 bit ports.
- +-12 V, +5V power from connector.
- Unidirectional, bidirectional I/O options.
- Interrupt handling capability.
- Interfaces to a wide range of peripherals.
- High speed transfer rates up to 460 Kbytes/s.
  (depends on the computer and software)

Applications:

- Solid state relay boards.
- Plotter interface.
- Printer interface.
- Digital I/O control.
- Useful with ADC's and DAC's.
- BCD - compatible panel meters and test equipement.

This board turns the PC/XT/AT into a digital I/O system controller for applications in laboratory testing, production testing and industrial process monitoring and control.

Block diagram



Functional description:

24 digital I/O lines are provided through an **8255-5 Programmable Peripheral Interface** (P.P.I.) organized into three 8-bit ports (**A**,**B**, and **C**), wich can be funcionally programmed as either inputs or outputs. Ports **A** and **B** are always used for digital I/O, while port **C** can be configured for digital data I/O, control, status, or handshake signals.

The port **A**, **B** and **C** may be read as well as written to. In addition, certain other configurations are possible for unidirectional and bidirectional strobed I/O where port **C** is used for control of data transfer and interrupt generation etc.. Users are referred to the **Intel 8255-5** data sheet for a complete technical description and summary of the various operating modes of the P.P.I..

Interrupt handling is via a tristate driver with separate enable (interrupt enable - active low). This may be connected to any of the interrupt levels **5** - **7** - **9** available on the IBM PC (or compatible) bus by means of a jumper on the board.

The interrupt is controlled by the **8259** interrupt controller in the IBM PC and this is set by the BIOS on system initialization to respond to positive (**low to high**) edge trigered inputs. Users **must** program the **8259** to respond to their requirements and set up corresponding interrupt handlers.

The IBM PC Bus

Only 10 address lines (A0 to A9) are decoded fot I/O resulting in a 1024 byte I/O space. IBM assigns standard I/O locations to many devices in this 1k byte region as shown in the next table:

Table: Assigned I/O locations in the IBM PC I/O space

Component	**PC / XT**	**AT**
DMA controller (8237A-5)	000-00F	000-01F
Interrupt controller (8259A)	020-021	020-03F
Timer	040-043	040-05F
Programmable Peripheral Interface (PPI 8255A-5)	060-063	none
Keyboard (8042)	none	060-06F
Realtime clock (MC146818)	none	070-07F
DMA page register	080-083	080-09F
Interrupt controller 2 (8259A)	none	0A0-0BF
DMA controller 2 (8237A-5)	none	0C0-0DF
Math coprocessor	none	0E0-0F1
Math coprocessor	none	0E8-0EF
Hard drive controller	320-32F	1F0-1F8
Game port (joysticks)	200-20F	200-20F
Expansion unit	210-217	none
Interface for second parallel printer	none	278-27F
Second serial interface	2F8-2FF	2F8-2FF
Prototype card	**300-31F**	**300-31F**
Network card	none	360-36F
Interface for first parallel printer	378-37F	378-37F
Monochrome Display Adapter and parallel interface	3B0-3BF	3B0-3BF
Color / Graphics Adapter	3D0-3DF	3D0-3DF
Disk controller	3F0-3F7	3F0-3F7
First serial interface	3F8-3FF	3F8-3FF

At first glance, it migth appear that there is free space in the "prototype card" region, which addresses 300 through 31f hexadecimal. However, many third-party vendors use this region for peripheral boards, if so we have to look elsewhere for I/O space.

Because the IBM_PC bus have many cards attached to it, we must drive it carefully, and each card must not load it excessively. In practice this requires that we use no more than about two lower power Schottky (LSTTL) inputs per slot and "bus buffer" chips to drive the data lines.

The interface card must decode its own address, which is achieved by using a digital comparator (Ex. 74LS682) that compares the address on the bus to that of the card. The card address is determined by the settings on a dip switch.

The AEN (address enable) line should also be compared on the comparator. This will eliminate the possibility of spurious address decoding during a bus DMA cycle, when AEN is high.

Note that, although the bus buffer is activated by the board selected signal (~BS) from the decoder, the bus buffer is arranged to direct data onto the card unless a read cycle is in progress (~IOR low). This prevents the possibility of a bus collision with the output from another card, wich can occur when the buffer decodes a bus transient at its board address and activates ~BS.

Since the board does not use address line A2, eigth I/O locations are decoded, even though the 8255 has only four registers, the effects of this address ambiguity are small: a slight loss of I/O space and duplication of the registers in the upper four bytes of the decoded space.

Base address switch:

The 8255-5 P.P.I. uses 4 I/O address locations which are decoded within the I/O address space of the IBM PC.

The base address is set by an 8 position DIP switch (SW1) (see Fig. 1) and can in theory be placed anywhere in I/O address space, but base addresses below FF hex (255 decimal) should be avoided as this address range is used by the internal I/O of the computer, the 200-3FF hex (512 - 1023) address range provides extensive unused areas of I/O space. In our case we use the address of the **prototype card** (300 - 31F hex).

The address map for the P.P.I. registers is:

Base Address	**+ 0**	**Port_A**	**read/write**
	+ 1	**Port_B**	**read/write**
	+ 2	**Port_C**	**read/write**
	+ 3	**Control**	**write only**

Programming:

The P.P.I. should first be configured in the initialization section of your program by writing to the control register. On power up or reset, all ports are configured as inputs. A wide variety of configuration are possible by writing the appropriate control code.

D7	0 - bit set/reset mode
	1 - mode set actve
D6	00 - Mode 0 for PA/PC4-7
D5	01 - Mode 1 for PA/PC4-7
	10 - (or 11) - Mode 2 for PA/PC4-7
D4	0 - PA output
	1 - PA input
D3	0 - PC4-7 output
	1 - PC4-7 input
D2	0 - Mode 0 for PB/PC0-3
	1 - Mode 1 for PB/PC0-3
D1	0 - PB output
	1 - PB input
D0	0 - PC0-3 output
	1 - PC0-3 input

Note that **D7** must be high (= **1**) to set the configuration of the ports.

Mode 0 - Basic I/O , all ports are I/O ports.

Mode 1 - Strobed I/O, part of PC controls data transfer

Mode 2 - Bidirectional I/O on PA, part of PC controls data transfers

Some examples:

PA input, PB output, PC0-3 input, PC4-7 output.

Control word = 1001 0001 binary or 91 hex.

Strobed output on PB, PA output, PC0-3 control, PC4-7 input.

Control word = 1000 1100 binary or 8C hex.

To program:

1. First write to the control register to set configuration e.g. in Basic:

```
**** OUT (Base address + 3), &H91
```

2. Then we can acess the ports as required. For example to read PA:

```
**** X% = INP ( Base address + 0)
```

To write to PB:

```
**** OUT ( Base address + 1), Data
```

To read PC:

```
**** Z% = INP ( Base address + 2)
```

3. Once the configuration has been set in the initialization , the P.P.I. will remain in that configuration until a futher write to the control register.

All registers are cleared by a write to the control register.

Using Microsoft C the next program reads the status of Port A.

```
/*       Reading the status of I/O Port A          */

#include<stdio.h>
#include<conio.h>

main()
{

/*                 Declare data types              */

int port_A,control_reg,word;
unsigned int contents;

/*                 Addresses of 8255               */

port_A=768;
control_reg=771;

/*                 Initialize control register     */

word=155;
outp(control_reg,word);

/*                 Read Port A                     */

contents=inp(port_A);

printf("Port A contains %d\n",contents);
}
```

Connector pin assignments:

All digital I/O is through a standard **DB37 male connector.** The connector pin assignments are as follows:

1 - Interrupt Input
2 - ~Interrupt enable
3 - PB7
4 - PB6
5 - PB5
6 - PB4
7 - PB3
8 - PB2
9 - PB1
10 - PB0
11 - Dig. Com.
12 -
13 - Dig. Com.
14 - -12V
15 - Dig. Com.
16 - +12V
17 - Dig. Com.
18 - +5V
19 - Dig. Com.

20 - +5V
21 - Dig.Com
22 - PC7
23 - PC6
24 - PC5
25 - PC4
26 - PC3
27 - PC2
28 - PC1
29 - PC0
30 - PA7
31 - PA6
32 - PA5
33 - PA4
34 - PA3
35 - PA2
36 - PA1
37 - PA0

Specifications:

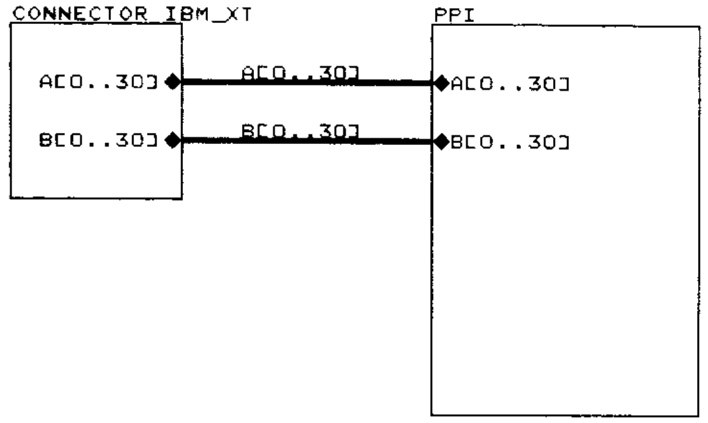
All outputs and inputs are TTL / DTL compatible and outputs will drive 1 standard TTL load (74 series) or 4 LSTTL (74LS) loads. CMOS compatibility can be obtained by connecting a 10Kohm pullup resistor from the input or output to +5V.

Logic inputs and outputs:

Level	Min	Max
Input low voltage	0,0 V	0,8 V
Input high voltage	2,0 V	5,25 V
Input low current (V_{in} = 0,8V)	-	-10 uA
Input high current (V_{in} = 2,4V)	-	+10 uA
Output low voltage		
(I_{out} = 1,7 mA)	-	0,45 V
Output high voltage		
(I_{out} = -200uA)	2,4 V	-

Darlington drive output current (Ports B & C only)

(R_{ext} = 750 Ω, V_{ext} = 1,5 V) .... -1 mA min., -4 mA max.



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MANUEL GONCALVES

Title
GENERAL PURPOSE INTERFACE

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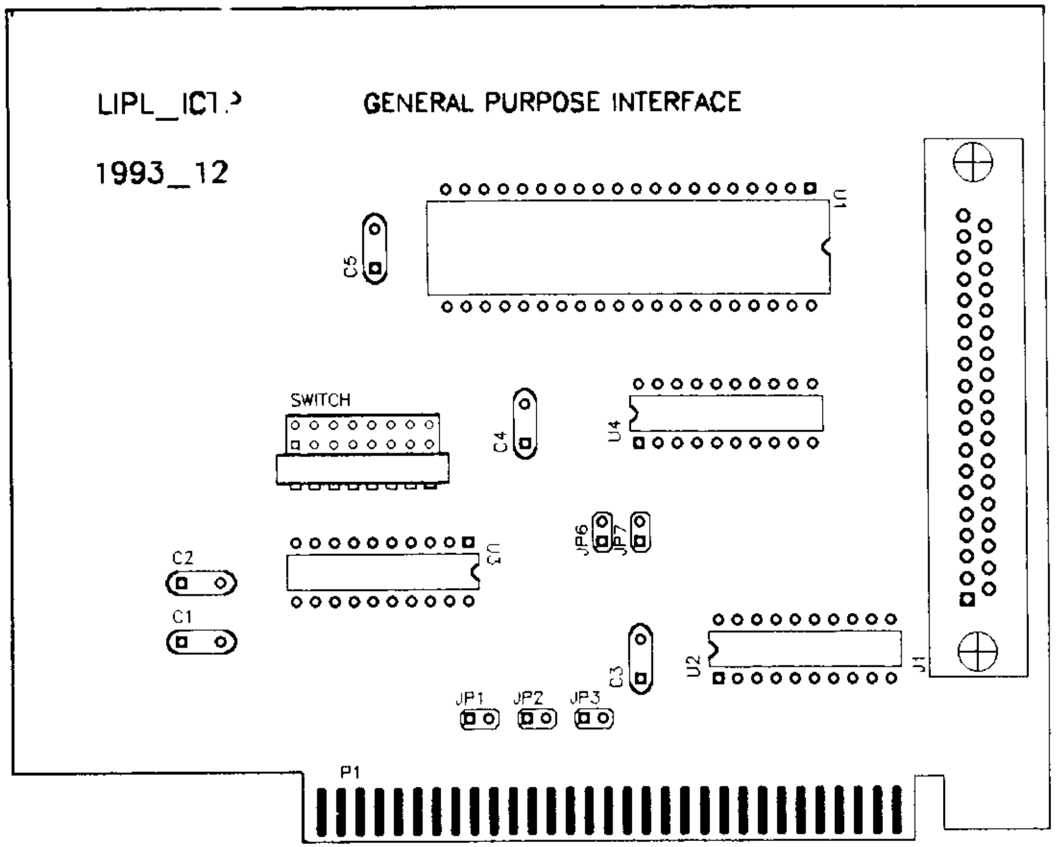

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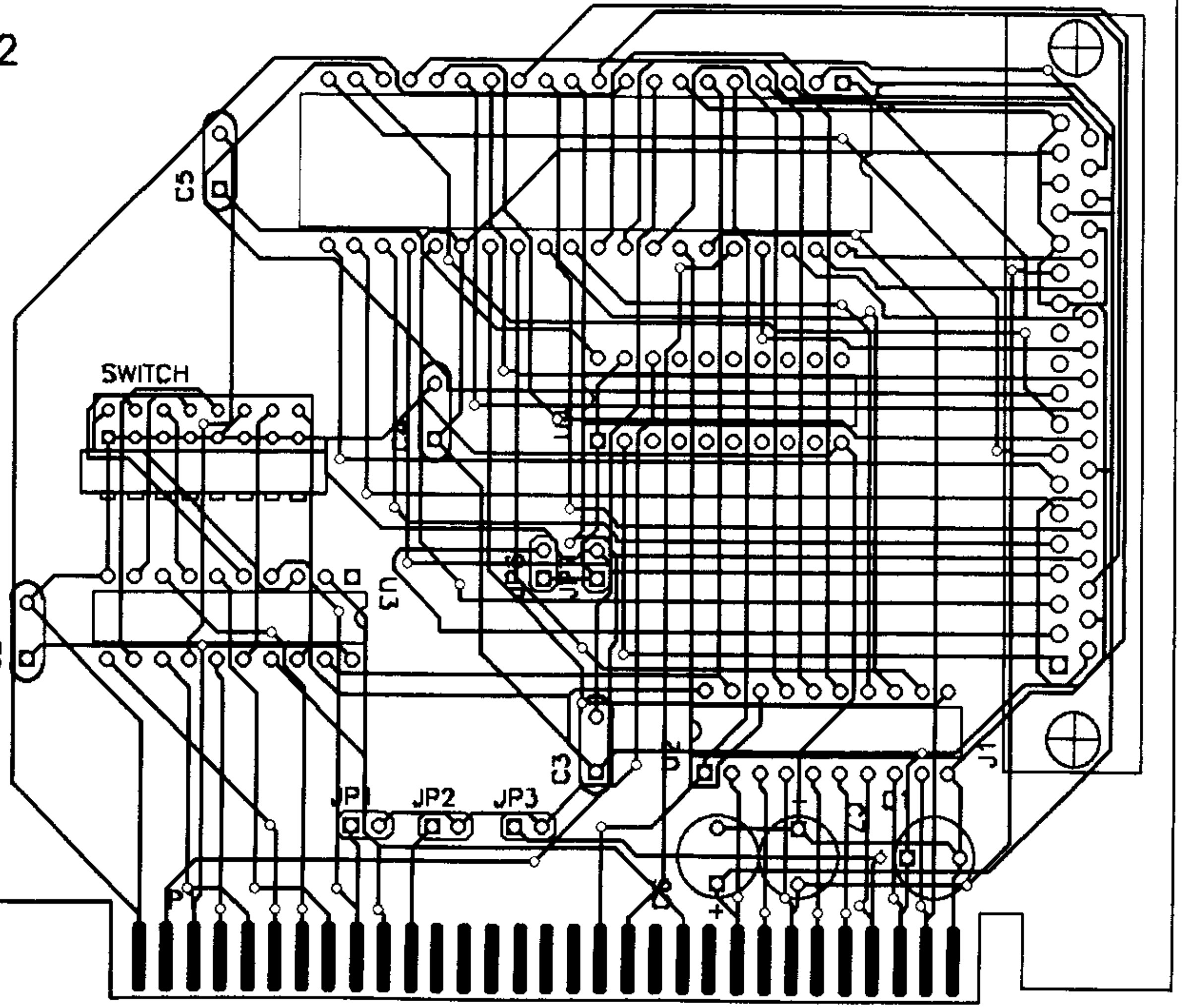
GENERAL PURPOSE INTERFACE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SWITCH
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