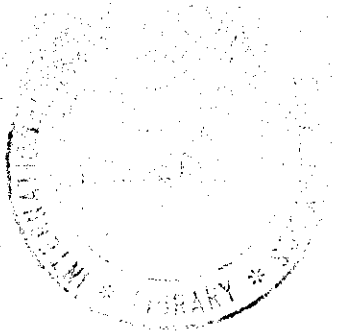




INTERNATIONAL ATOMIC ENERGY AGENCY
UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION



INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS
34100 TRIESTE (ITALY) - P.O. BOX 58 - MIRAMARE - STRADA COSTIERA 11 - TELEPHONES: 234231/234232
CABLE: CENTRATON - TELEX 460392-1

SMR/90 - 20

COLLEGE ON MICROPROCESSORS:

TECHNOLOGY AND APPLICATIONS IN PHYSICS

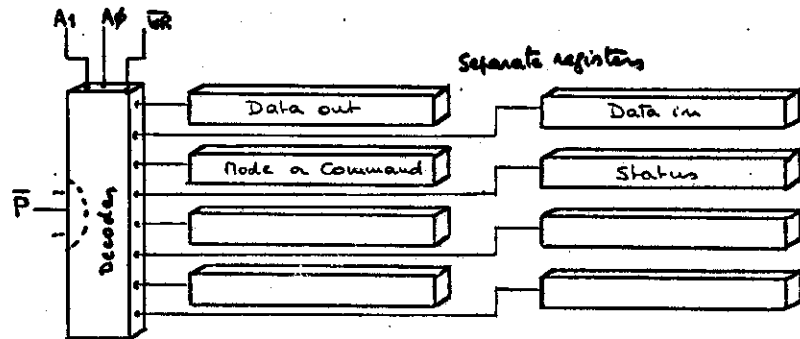
7 September - 2 October 1981

MICROPROCESSOR INTERFACING - II: Programmable interfaces

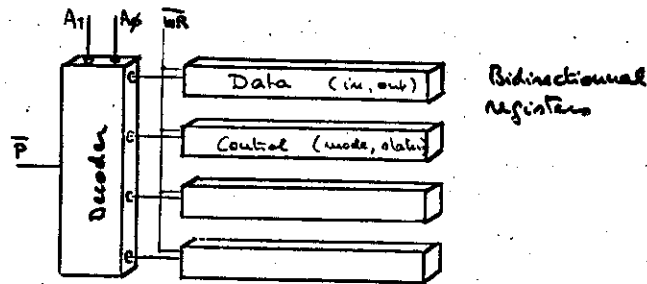
J-D. NICOUD

LAMI
Ecole Polytechnique Fédérale
de Lausanne
Chemin de Bellerive 16
CH-1007 Lausanne
Switzerland

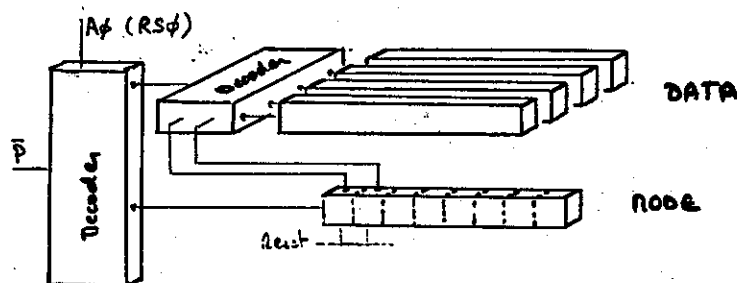
These are preliminary lecture notes, intended only for distribution to participants. Missing or extra copies are available from Room 230.



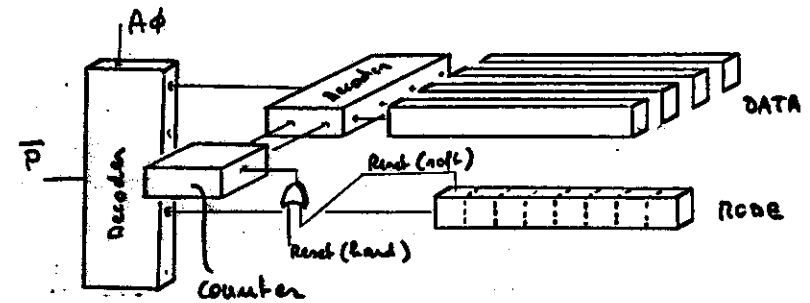
1. Simple address scheme with separate input and output registers



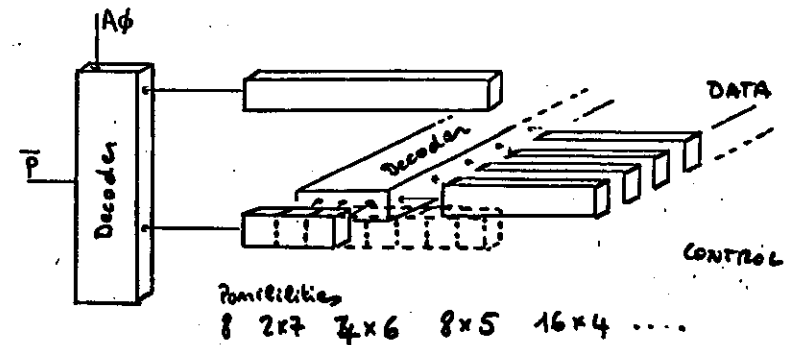
2. Simple address scheme with bidirectional registers



3. Addressing with sub-address in mode registers

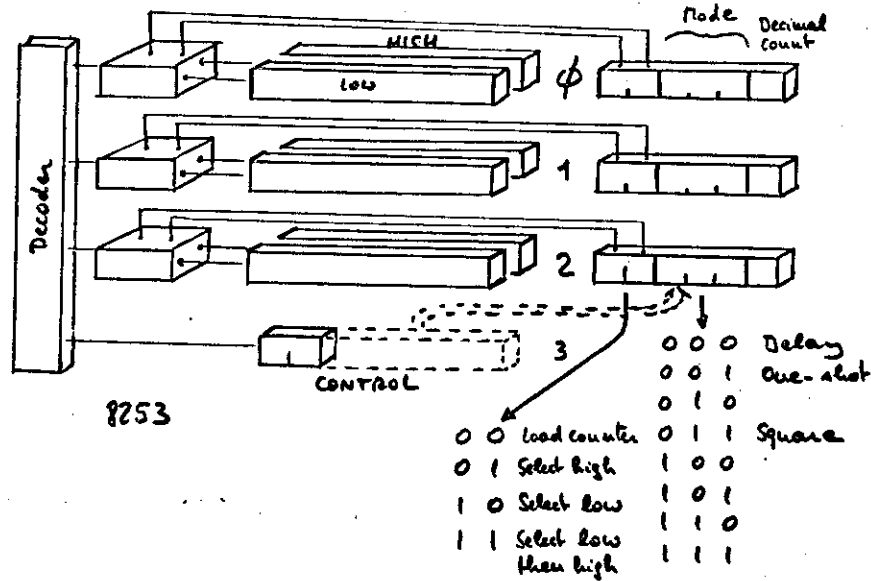


4. Subaddress in a counter

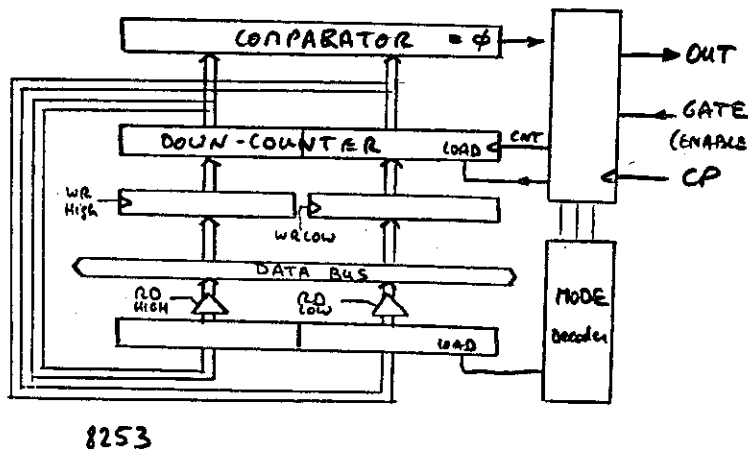


5. Subaddress in the data word itself

8253 Timer

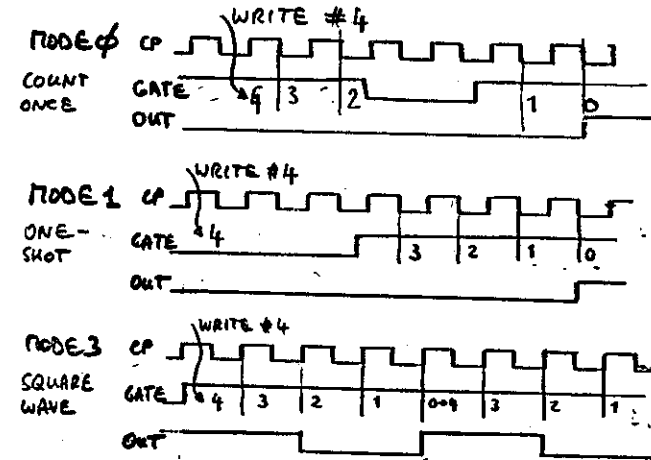


6. Addressing of 8256 register



7. Logic for each timer

-3-

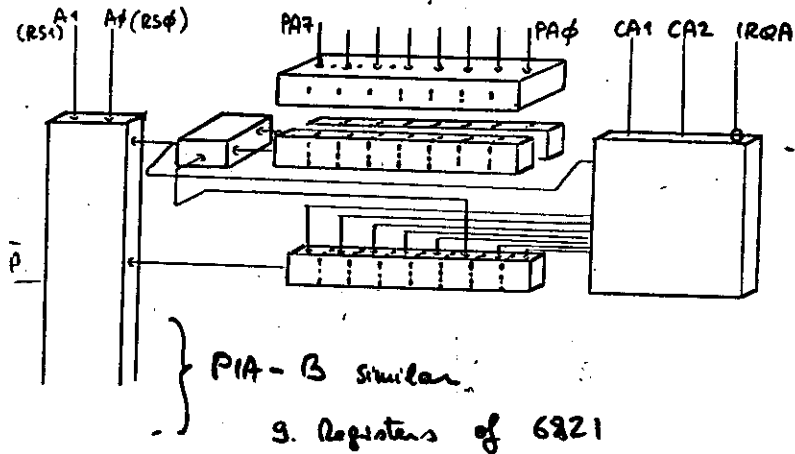


Example: Mode 3 on counter 0, divide by 20 frequency of 10 kHz

LDAA #36 Mode: select timer 0, low-high, mode 3
 STAA \$BFC3 Address of mode register
 LDAA #20
 STAA \$BFC0 Write low counter
 LDAA #0
 STAA \$BFC0 Write high counter and start

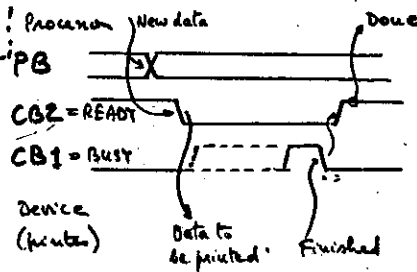
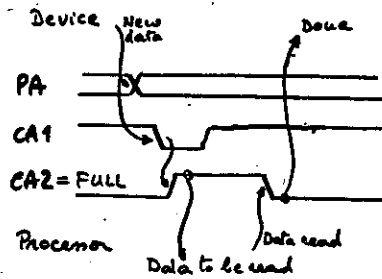
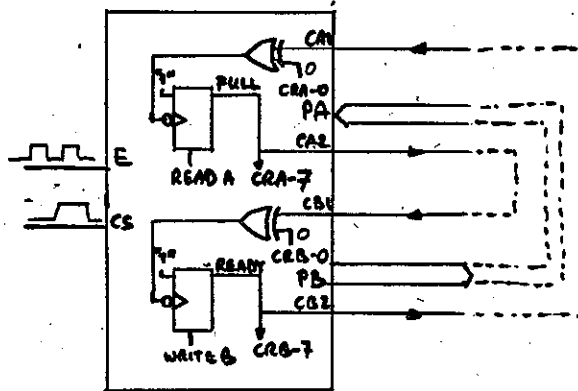
8. Major modes of the 8253

6821 PIA



3. Registers of 6821

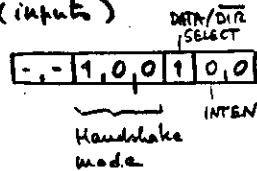
PIA Handshake mode
Read on PA Write on PB



Initialization

DIRA ← 0 (inputs)

CRA ← 24



DIRB ← FF

CRB ← 24

10 Handshake mode

