SMR/90 - 20

COLLEGE ON MICROPROCESSORS:

TECHNOLOGY AND APPLICATIONS IN PHYSICS

7 September - 2 October 1981

MICROPROCESSOR INTERFACING - II: Programmable interfaces

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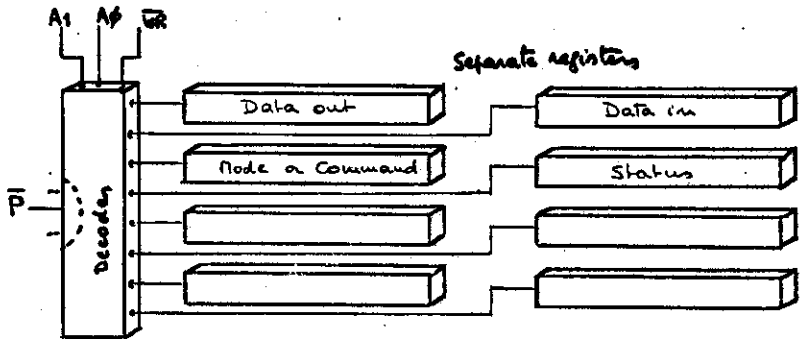
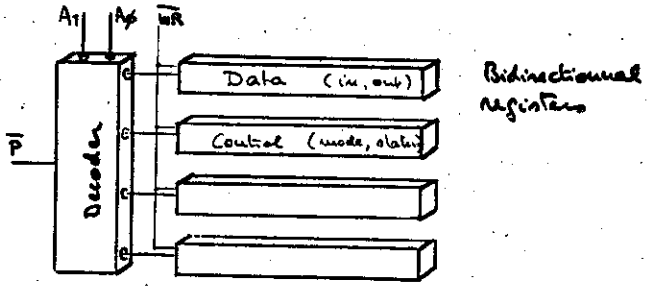
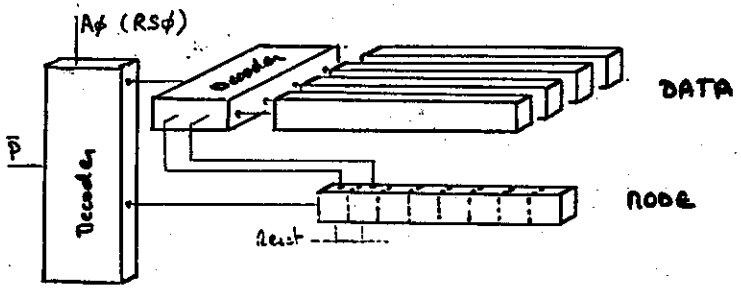


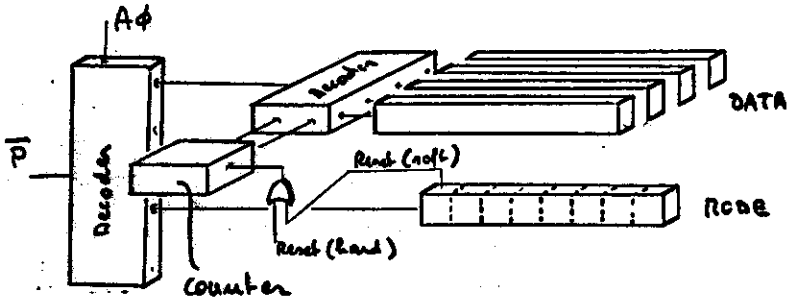
1. Simple address scheme with separate input and output registers



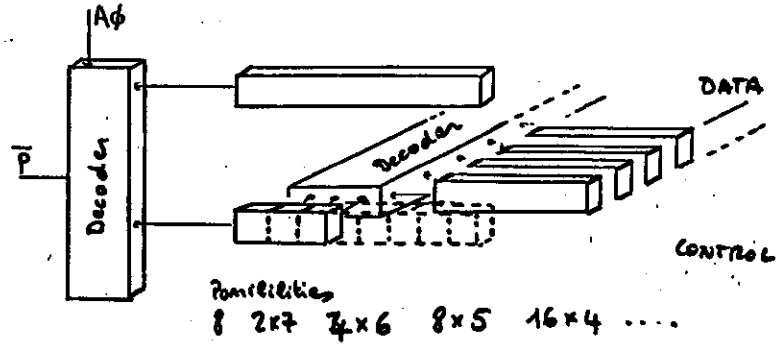
2. Simple address scheme with bidirectional registers



3. Addressing with sub-address in mode register

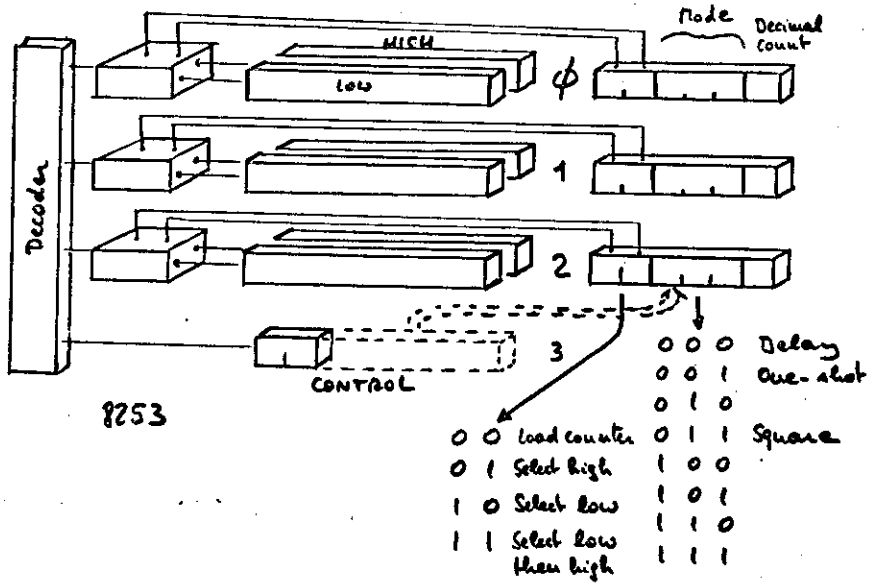


4. Subaddress in a counter

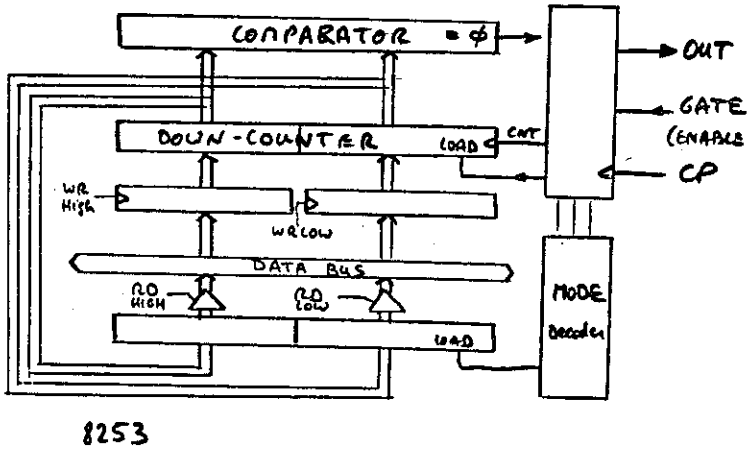


5 Subaddress in the data word itself

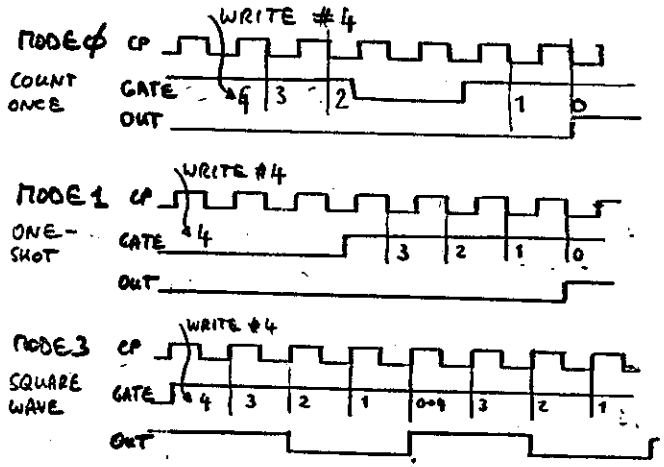
8253 Timer



6. Addressing of 8256 registers



7. Logic for each timer

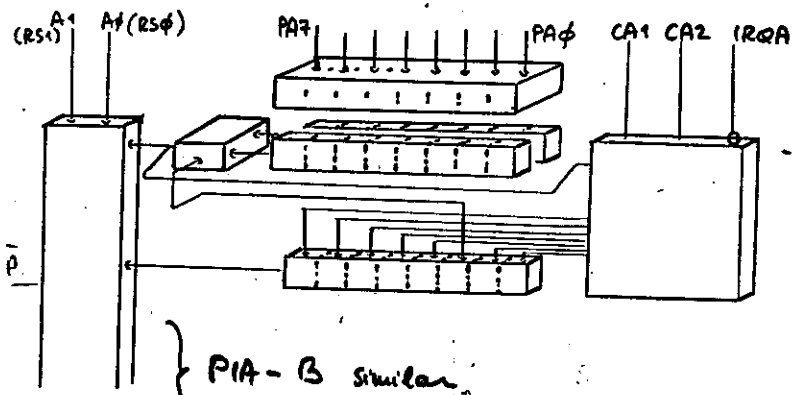


Example: Mode 3 on counter Φ, divide by 20 frequency of 10kHz

```
LDAA  #$36    Mode: select timer Φ, low-high, mode 3
STAA  $BFC3   Address of mode register
LDAA  #20
STAA  $BFC0   Write low counter
LDAA  #0
STAA  $BFC0   Write high counter and start
```

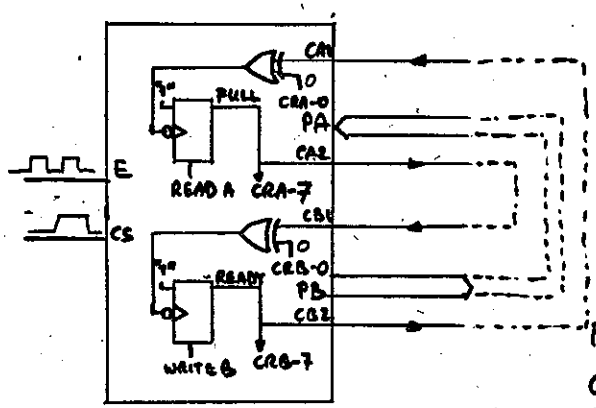
8. Major modes of the 8253

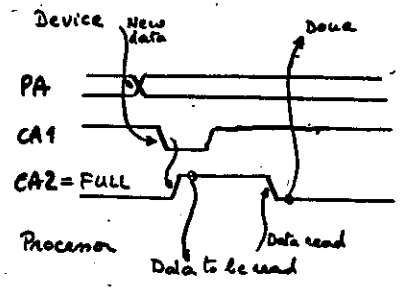
6821 PIA

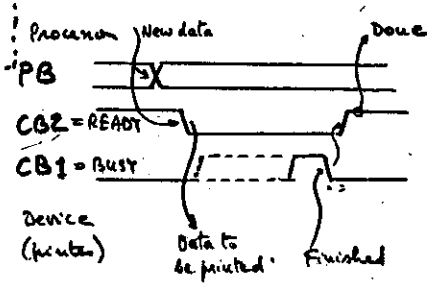


9. Registers of 6821

PIA Handshake mode
Read on PA Write on PB







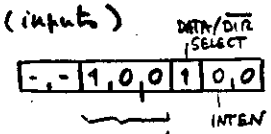
Initialization

DIRA ← 0 (inputs)

CRA ← 24

DIRB ← FF

CRB ← 24



10 Handshake mode