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COLLEGE ON MICROPROCESSORS:

TECHNOLOGY AND APPLICATIONS IN PHYSICS

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LECTURE NOTES ON LOGIDULES

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LECTURE NOTES ON LOGIDULES.
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) MICRO-PROCESSOR IS NOT A COMPUTER.

-IT'S ONLY AN ARITHMETIC UNIT WITH ADDRESSING CAPABILITY.

-IT NEEDS MEMORY, SOMEWHERE TO PUT THE INSTRUCTIONS AND DATA.

-IT NEEDS COMMUNICATION WITH THE OUTSIDE WORLD.

OTE:- THE KIT HAS A FEW OF EACH OF THESE NEEDS AND CAN BE CONSIDERED AS A MICRO-COMPUTER

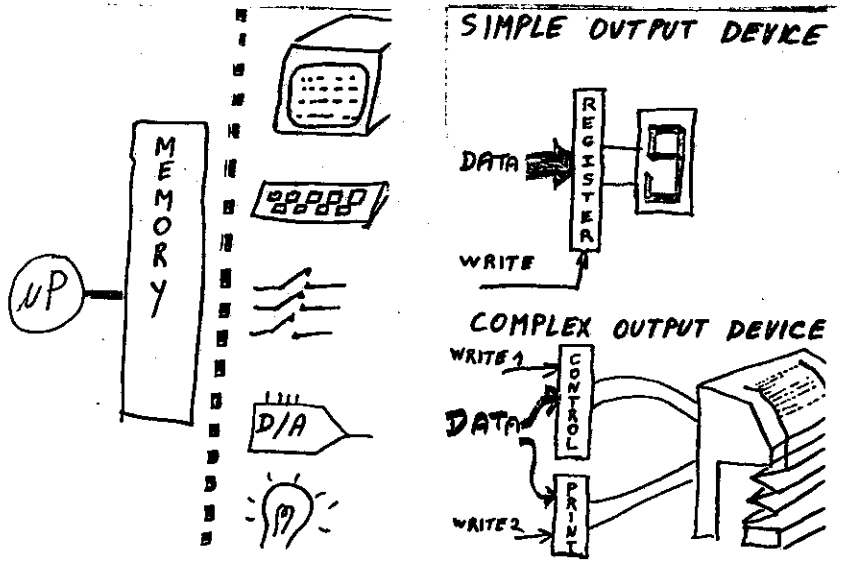
) WHAT DOES THE OUTSIDE WORLD LOOK LIKE?

-PASSIVE OUTPUT DEVICE NEEDS ONE DATA REGISTER TO CONTAIN A CHOSEN DATA WORD THAT IS CONTINUOUSLY DISPLAYED. TO CHANGE THE DISPLAY WRITE IN ANOTHER DATA WORD TO THE DATA REGISTER.

-MORE COMPLEX OUTPUT DEVICE NEEDS TWO (OR MORE) REGISTERS. ONE IS THE 'CONTROL' REGISTER (ONE BIT DECIDES THE PRINT SPEED, ONE BIT THE TYPE FACE, THREE BITS THE LINE SPACING ETC ETC). THE OTHER IS THE DATA REGISTER (THE CHARACTER TO BE PRINTED).

- DITTO FOR INPUT DEVICES

- IN GENERAL THEN INPUT OR OUTPUT DEVICES ARE, OR CAN BE MADE TO LOOK LIKE, REGISTERS, FOR BOTH CONTROL AND DATA FUNCTIONS.



HOW CAN THE MICROPROCESSOR 'SEE' A REGISTER ?

- IF WE ASSIGN AN ADDRESS TO EACH DIFFERENT REGISTER THEN THE MICROPROCESSOR CAN 'THINK' THAT IT IS ADDRESSING MEMORY (WHICH IT KNOWS HOW TO DO) RATHER THAN EXTERNAL REGISTERS (WHICH IT IS NOT AWARE OF)

- THIS WAY OF COMMUNICATING WITH THE EXTERNAL WORLD IS KNOWN AS 'MEMORY MAPPED I/O'

- READ THE KIT MANUAL FOR DETAILS OF THE MEMORY MAP

HOW DOES THIS WORK IN A BIT MORE DETAIL ?

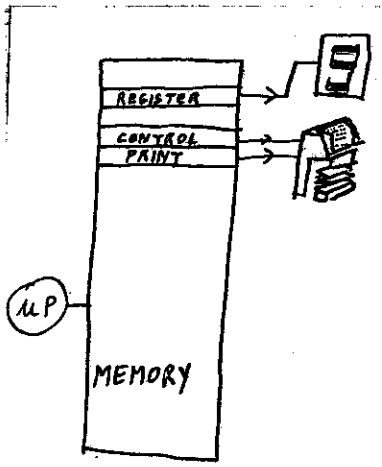
- THE MICROPROCESSOR IN ITS MINIMUM CONFIGURATION GENERATES AND HAS CONTROL OVER THREE BUSSES.

- ADDRESS BUS OF 16 LINES GIVING ACCESS TO OVER 64000 INDIVIDUAL LOCATIONS

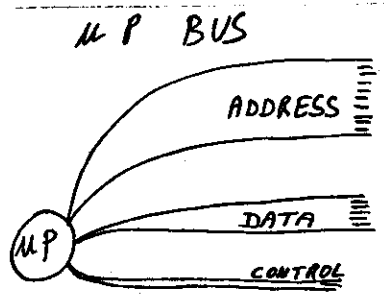
- DATA BUS OF EIGHT LINES (ONE BYTE WIDE)

- CONTROL BUS TO INDICATE WHEN THE ADDRESS IS VALID, WHEN THE DATA IS GOOD, READ/WRITE CYCLE INFORMATION ETC.

- IN THE GENERAL CASE THE OUTSIDE WORLD LOOKS AT THE ADDRESS BUS AND DECIDES IF 'IT' IS BEING TALKED TO BY THE MICRO-PROCESSOR. IF SO IT THEN DECIDES IF THE MICRO WISHES TO GIVE OR TAKE DATA. WHEN THE CONTROL LINES SAY 'DO IT NOW' THE PERIPHERAL EITHER TAKES DATA FROM, OR GIVES DATA TO THE DATA BUS. ADDRESSES NOT BEING TALKED TO IGNORE THE 'DO IT NOW' SIGNAL SO THAT THERE IS NO CONFLICT.



MEMORY MAPPED I/O



A BUS IS A WAY OF ELECTRICALLY CONNECTING TOGETHER DIFFERENT ELEMENTS SUCH THAT THEY MAY COMMUNICATE ONE WITH ANOTHER.

- A BUS MAY BE SERIAL OR PARRALELL. THERE ARE LECTURES TO COME ON THAT SUBJECT.

- A BUS MAY BE SHARED BETWEEN MANY DEVICES ON THE CONDITION THAT ONLY THE DEVICE CURRENTLY ADDRESSED MAY DRIVE THE BUS. WE NEED THEN A DRIVER ENABLE FUNCTION AND THE KIND OF ELECTRONICS THAT PERMITS THIS KIND OF SHARING.

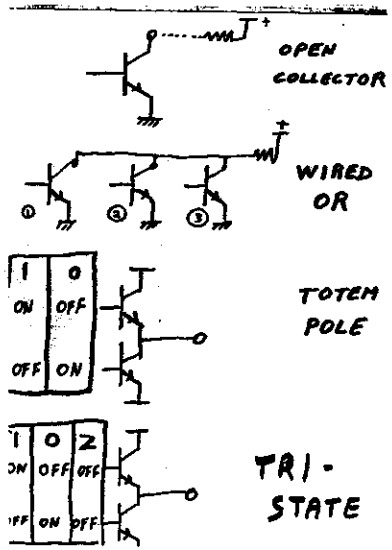
- ONE WAY TO DO IT IS TO USE THE OPEN COLLECTOR TECHNIQUE.

- IF TRANSISTOR 'ON' THE COLLECTOR IS AT A LOW VOLTAGE.
  IF TRANSISTOR IS 'OFF' THE RESISTOR PULLS UP THE COLLECTOR TO A HIGH VOLTAGE

- IF SEVERAL DEVICES ARE CONNECTED TO THE SAME WIRE AND ONLY THE ONE ADDRESSED HAS THE RIGHT TO BE 'ON' THEN THE SHARING IS POSSIBLE. THIS IS CALLED THE 'WIRED OR'. THIS TECHNIQUE IS NOT WIDELY THESE DAYS USED SINCE YOU MUST SOMEWHERE HAVE THE RESISTORS WHICH USE UP SPACE AND POWER.

- NORMAL LOGIC OUPUTS FROM TTL ARE 'TOTEM POLE' AND DEFINE A LOGICAL ONE OR ZERO DEPENDING ON THE TWO ALLOWED STATES OF THE OUTPUT TRANSISTORS. THESE CANNOT BE USED TO DRIVE A BUS BECAUSE IF ONE DEVICE IS HIGH AND ANOTHER LOW THERE WILL BE A CONFLICT AND SOME MID-LEVEL WILL RESULT.

- BY ALLOWING BOTH TRANSISTORS TO BE OFF AT THE SAME TIME THE TRI-STATE OUTPUT CAN PRESENT A HIGH IMPEDANCE TO THE OUTSIDE WORLD AS WELL AS THE LOGICAL ONE OR ZERO. THIS IS THE WAY THAT VIRTUALLY ALL MICROPROCESSOR BUSSES ARE CONSTRUCTED. EACH DEVICE IS IN TRI-STATE UNTIL IT IS A) ADDRESSED AND B) TOLD TO 'DO IT NOW'.



- WE STUDY HERE THE TWO INSTRUCTIONS COMMONLY USED IN OUR NEXT GROUP OF EXERCISES. LOAD THE 'A' ACCUMULATOR FROM MEMORY (LDAA MEMORY) AND STORE THE 'A' ACCUMULATOR IN MEMORY (STAA MEMORY)

- THESE DETAILS ARE TAKEN FROM THE KIT MANUAL.

- FOR LDAA THE PROCESSOR FETCHES THE OP-CODE, FETCHES THE DESTINATION ADDRESS, PUTS THE PERIPHERAL ADDRESS ON THE ADDRESS BUS AND VIA THE CONTROL BUS ASKS FOR THE DATA.

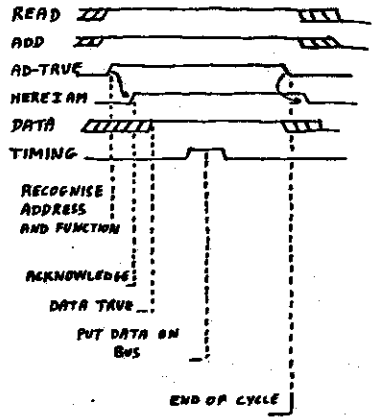
- FOR STAA THE PROCEDURE IS THE SAME EXCEPT THAT ONE MORE CYCLE IS NEEDED TO GET THE ACCUMULATOR DATA ONTO THE DATA BUS AND THE CONTROL LINES INSTRUCT THE PERIPHERAL WHEN TO TAKE THE DATA.

- EXAMINE THE TIMING OF THE LAST CYCLE OF THESE TWO OPERATIONS
- IN BOTH CASES THE PERIPHERAL FOLLOWS THE SAME STEP BY STEP PROCEDURE:-
  ....RECOGNISE ITS ADDRESS AND THE FUNCTION REQUESTED
  ....TELL THE PROCESSOR THAT IT'S ALIVE AND WAITING
  ....EXECUTE FUNCTION ON COMMAND

LDAA MEMORY

CY	ADDRESS BUS	DATA BUS	ADDRESS TRUE	READ
1	PC	OP CODE	1	1
2	PC+1	DEST ADD [H]	1	1
3	PC+2	DEST ADD [L]	1	1
4	DEST ADD	DATA	1	1

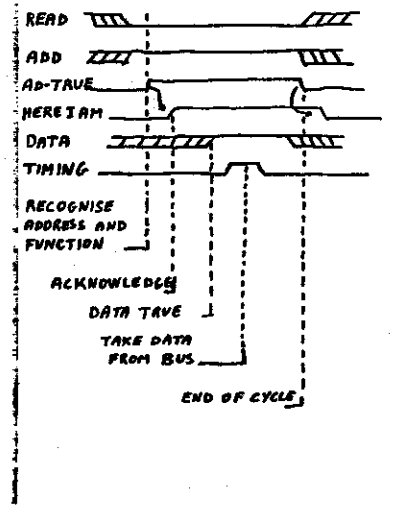
TIMING DIAGRAM (R)



STAA MEMORY

CY	ADDRESS BUS	DATA BUS	ADDRESS TRUE	READ
1	PC	OP CODE	1	1
2	PC+1	DEST ADD [H]	1	1
3	PC+2	DEST ADD [L]	1	1
4	DEST ADD	——	0	1
5	DEST ADD	DATA	1	0

TIMING DIAGRAM (W)

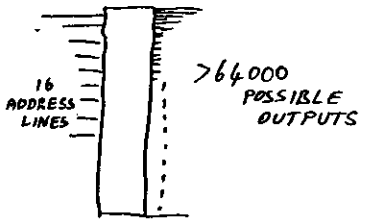


WHAT IS NEEDED PHYSICALLY TO INTERFACE TO THE BUSSES. ?

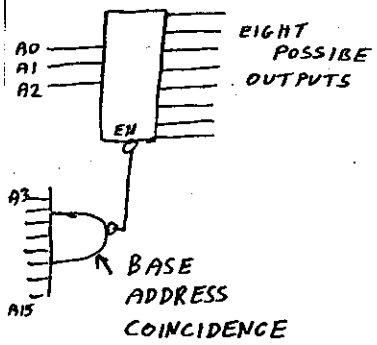
- 16 ADDRESS LINES GIVE 64000 POSSIBILITIES.
- SINCE THE DESIGNER CAN ASSIGN THE ADDRESS OR GROUP OF ADDRESSES FOR A GIVEN DEVICE IT MAKES MORE SENSE TO DECODE ONLY AS MANY ADDRESS LINES THAT ARE STRICTLY NEEDED AND ENABLE THEM WITH THE BASE ADDRESS COINCIDENCE.

  FOR EXAMPLE..... THE POLITE PERIPHERAL.
- IF THE BASE ADDRESS OF THE DEVICE IS ON THE BUS AT THE SAME TIME AS THE VALID MEMORY ADDRESS CONTROL IS TRUE. THEN WE ENABLE THE FUNCTION DECODER AND REPLY 'HERE I AM' TO THE CONTROL BUS.
- WHEN THE DECODER IS ENABLED IT OUTPUTS THE FUNCTION TO BE EXECUTED.
- WHEN THE PROCESSOR SAYS 'DO IT NOW' (THE 'E' LINE) THE FUNCTION GATES ARE STROBED TO GENERATE THE PUT OR TAKE DATA STROBES.

ONE WAY TO DO DECODING

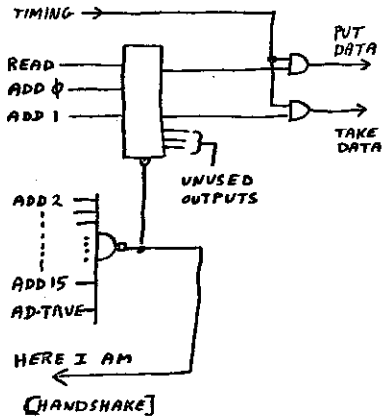


A BETTER WAY



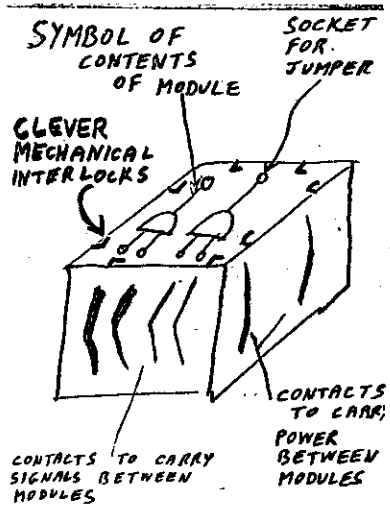
NOTE :- DECODING JUST ADDRESS IS NOT ENOUGH.
ALSO MUST DECODE THE READ OR WRITE FUNCTION

THE POLITE PERIPHERAL

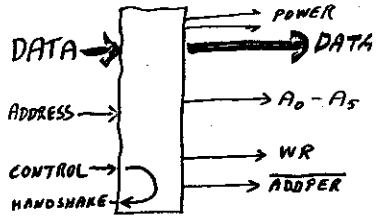


HOW CAN WE DO THIS USING LOGIDULES AND WHAT IS A LOGIDULE ANYWAY?

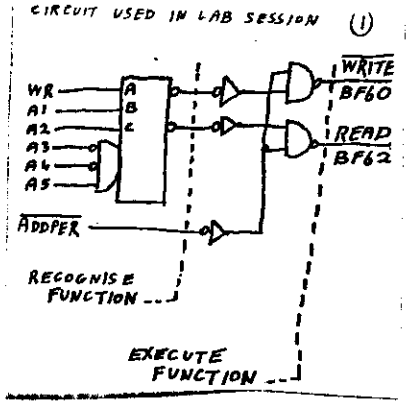
- LOGIC CHIPS ALL LOOK THE SAME AND ARE A TEACHING NIGHTMARE.
- LOGIDULES MECHANICALLY AND ELECTRICALLY INTERLOCK
- WIRED INTERCONNECTIONS ARE AT A MINIMUM
- THE MASTER MODULE INTERFACES TO THE MICROPROCESSOR BUSSES.
- A SUBSET OF THE CONTROL BUS IS AVAILABLE TO THE LOGIDULES.
- THE BASE COINCIDENCE DETECTOR IS STROBED WITH 'E'
- THE BASE ADDRESS CHOSEN IS BF40 AND THE RANGE IS UP TO BF7F. THIS IS IN THE ADDRESS SPACE OF THE KIT AVAILABLE OFF THE BOARD.
- THE MASTER MODULE DOES THE HANDSHAKING.
- USE A DECODER (74138) TO DECODE THE R/W LINE, AND A1..A5.
- THIS IGNORES A0 SO IT BECOMES A NO CARE (PARTIAL DECODING)
- THE OUTPUTS FROM THE DECODER ARE TRUE LOW SO WE INVERT THEM
- ADDPER/ IS TRUE LOW SO WE INVERT THAT TOO.
- ADDPER STROBES THE FUNCTION SINCE IT HAS THE TIMING.
- THE LEDS REGISTER CONNECT DIRECTLY TO THE DATA BUS BECAUSE THEY ARE WRITE ONLY AND THERE CAN BE NO CONFLICT
- THE SWITCHES ARE BUFFERED THROUGH THREE-STATE DRIVERS.
- THESE DRIVERS ARE KEPT IN HIGH IMPEDANCE MODE UNTIL IT IS TIME TO 'DO IT NOW' AND TRANSMIT THE STATE OF THE SWITCHES ONTO THE DATA BUS.

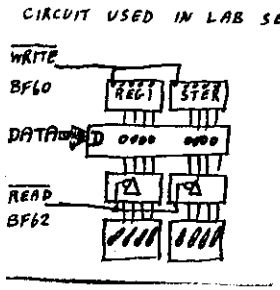


LOGIDULE TO KIT INTERFACE

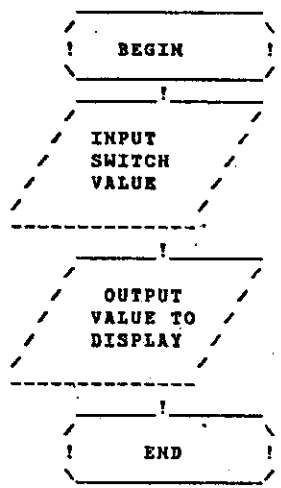


ADDPER IS THE 'AND' OF THE BASE ADDRESS COINCIDENCE AND THE TIMING STROBE 'E'.
FOR OUR EXERCISES WE WILL USE IT AS THE TIMING STROBE.





READ IN THE VALUE OF A SET OF SWITCHES AND OUTPUT THAT VALUE
THE 'LED' DISPLAY.
LN:- TO 'READ' THE VALUE OF THE SWITCHES WE LOAD THE 'A'
CUMULATOR WITH THE CONTENTS OF ADDRESS BF40. THIS IS THE 'LDA'
STRUCTION USING THE EXTENDED MODE OF ADDRESSING. SIMILARILY TO
RITE' A VALUE TO THE LED'S WE STORE THE CONTENTS OF THE 'A'
CUMULATOR IN MEMORY LOCATION BF40. THIS IS THE 'STA' INSTRUCTION
AIN USING THE EXTENDED MODE OF ADDRESSING.



USING THE MANUAL WE FIND THAT THE OP-CODES FOR THESE
STRUCTIONS ARE RESPECTIVELY
B6 <ADDRESS> LDA ADDRESS
B7 <ADDRESS> STA ADDRESS
FOR THE PURPOSES OF THESE EXERCISES WE SHALL USE THE AVAILABLE RAM
AT STARTS AT ADDRESS 0. OUR PROGRAM NOW BECOMES:-

DRESS	OP-CODE		MNEUMONIC	PSEUDO-CODE
00		START:	EQU *	BEGIN
00	B6 BF 40		LDAA SWITCH	(A) <= SWITCHVALUE
03	B7 BF 40		STAA DISPLAY	DISPLAY <= (A)
06	3F		SWI	END