INTERNATIONAL ATOMIC ENERGY AGENCY
UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION

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SMR/90 - 26

COLLEGE ON MICROPROCESSORS:

TECHNOLOGY AND APPLICATIONS IN PHYSICS

7 September - 2 October 1981

SUMMARY OF "MICROPROCESSOR ARCHITECTURE"

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	INITIAL	θ := b+c	y := a*θ	
0	a	a	a	MEMORY
1	b	b	b	
2	c	c	c	
3	y	y	(a*(b+c))	
4		(b+c)	(b+c)	

EXECUTION of y := a*(b+c) IN THREE ADDRESS MACHINE.

	INITIAL	PUSH Ay	PUSH a	PUSH b	PUSH c	+	*	POP	
0	a	a	a	a	a	a	a	a	MEMORY
1	b	b	b	b	b	b	b	b	
2	c	c	c	c	c	c	c	c	
3	y	y	y	y	y	y	y	(a*(b+c))	
4					b				
5				a	a	a			
6			3	3	3	3	3		
A		3	a	b	c	(b+c)	(a*(b+c))		MPU
SP	8	7	6	5	4	5	6	8	

EXECUTION of y := (a*(b+c)) IN STACK MACHINE.

(cf SLIDES 15 & 16)

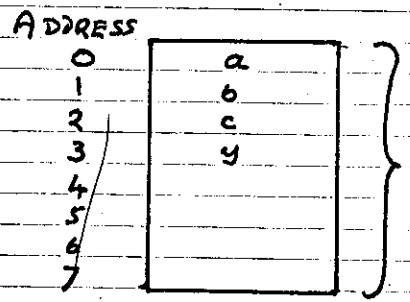
ALGORITHM of PROGRAMME

KNOWS DATA AS

- NAMED VARIABLES.

  e.g. a, b, c, y.

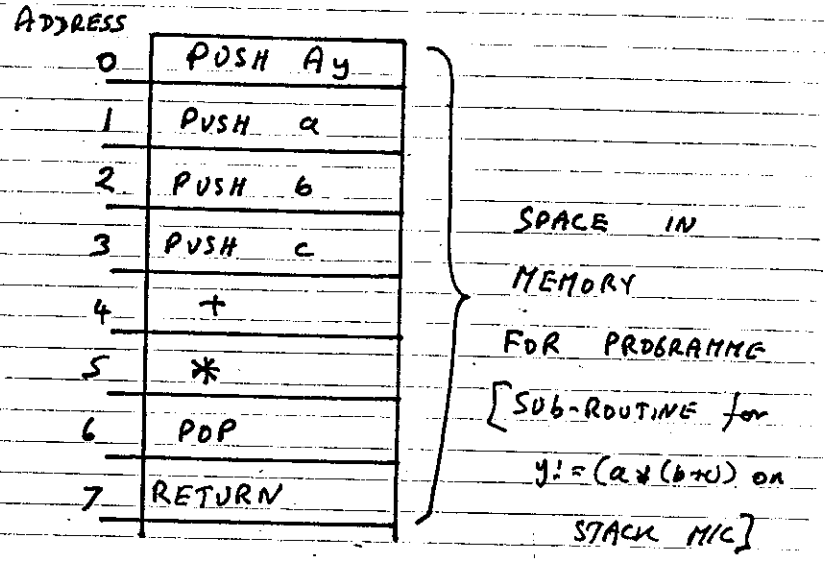
- WORKING VARIABLES.
  - 3-Address ⊖ EXPLICIT
  - STACK SPACE IMPLICIT.



PROGRAMME REFERS TO DATA OBJECT BY ITS ADDRESS IN MEMORY

THE PROGRAMME

IS LAID DOWN IN MEMORY IN CONSECUTIVE MEMORY LOCATIONS.



NAMED VARIABLES MUST BE REPLACED BY EXPLICIT ADDRESS VALUES

e.g. PUSH Ay → PUSH 3

PUSH a → PUSH M_0

PUSH b → PUSH M_1

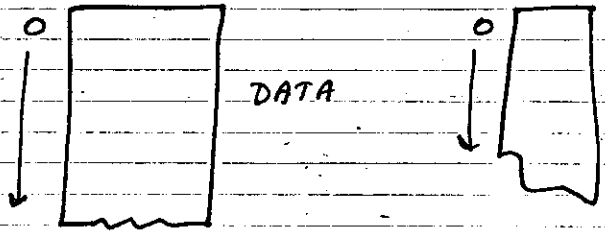
etc.

N.B. THE PROGRAMME CANNOT BE LOCATED IN MEMORY LOCATIONS 0 → 3 !!

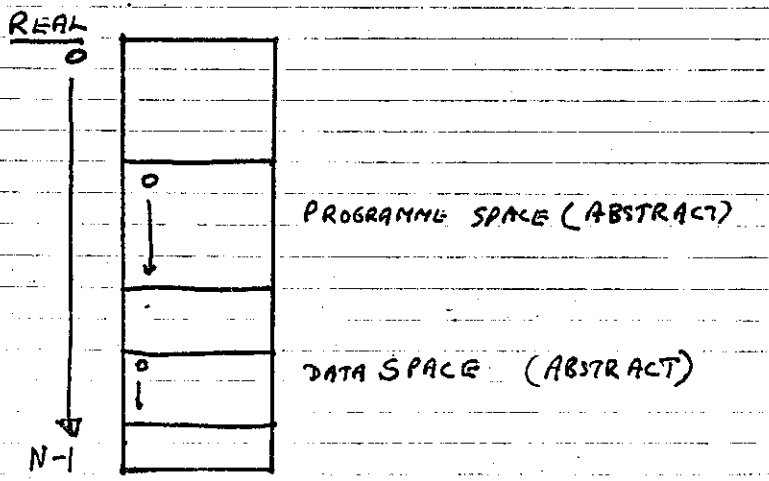
LOCATION of DATA & PROGRAMME.

WHEN DESIGNING A PROGRAMME IT IS CONVENIENT [ESSENTIAL] TO ASSUME AN ABSTRACT MEMORY SPACE FOR

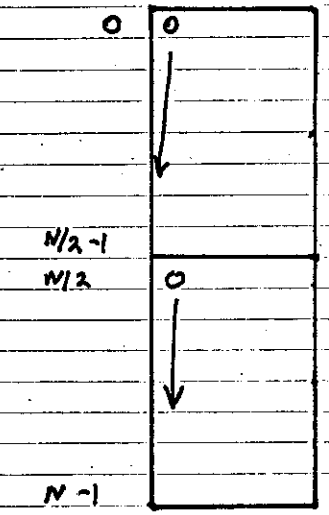
- DATA
- PROGRAMME



THESE SPACES ARE THEN LOCATED IN REAL MEMORY



SEGMENTATION of REAL MEMORY



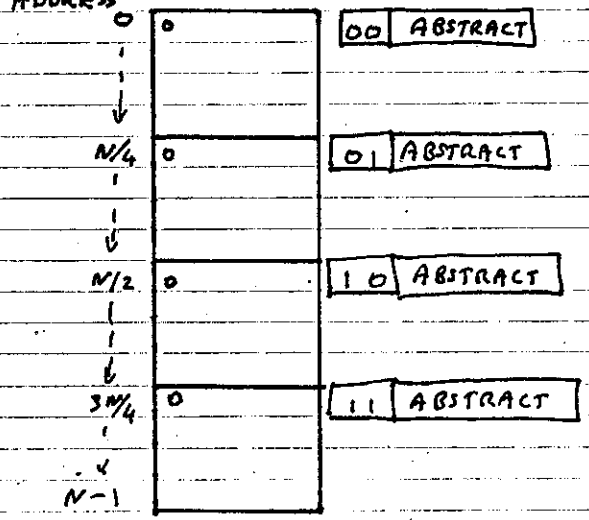
ABSTRACT DATA ADDRESS +0 = REAL DATA ADDRESS

0	ABSTRACT ADDRESS

ABSTRACT DATA ADDRESS + N/2 = REAL DATA ADDRESS

1	ABSTRACT ADDRESS

CONCATENATION.



00	ABSTRACT

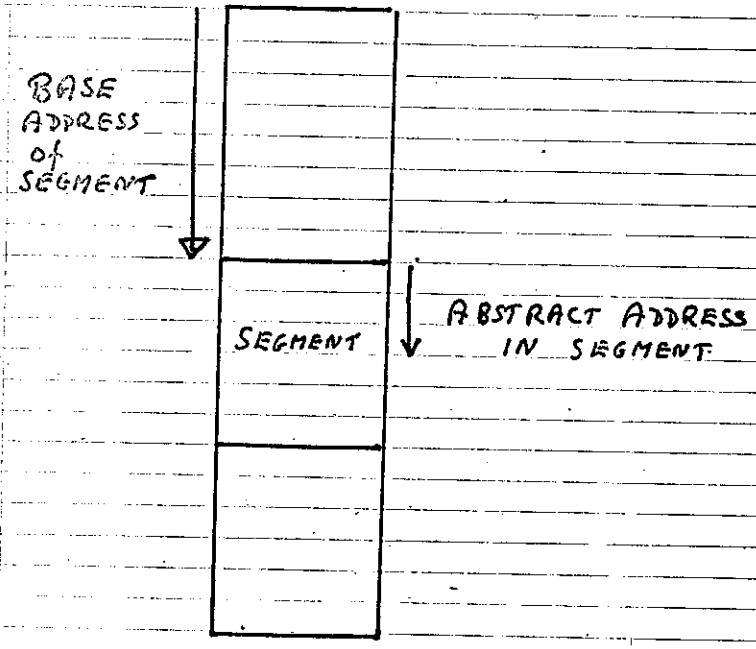
01	ABSTRACT

10	ABSTRACT

11	ABSTRACT

EQUAL SEGMENTS CAN BE MANAGED BY CONCATENATION.

General Segmentation.



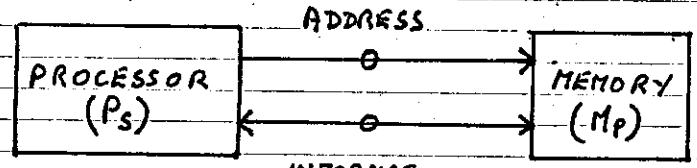
REAL ADDRESS = BASE ADDRESS
+ ABSTRACT ADDRES.

(BASE REGISTER) + LITERAL ≡ DIRECT

(BASE REGISTER) + (GENERAL REGISTER) ≡ INDIRECT

c.f. 8086
68000
Z-8000.
(SLIDES 8, 12 & 6).
also SLIDES 21 → 25.

Processor - Memory Pair



1. CLOSED SYSTEM EQUIVALENT TO A FINITE STATE MACHINE

$$S := f(S)$$

S ::= STATE VECTOR

State Transition occurs during an Instruction Cycle

$$S ::= \langle P_S \times M_P \rangle$$

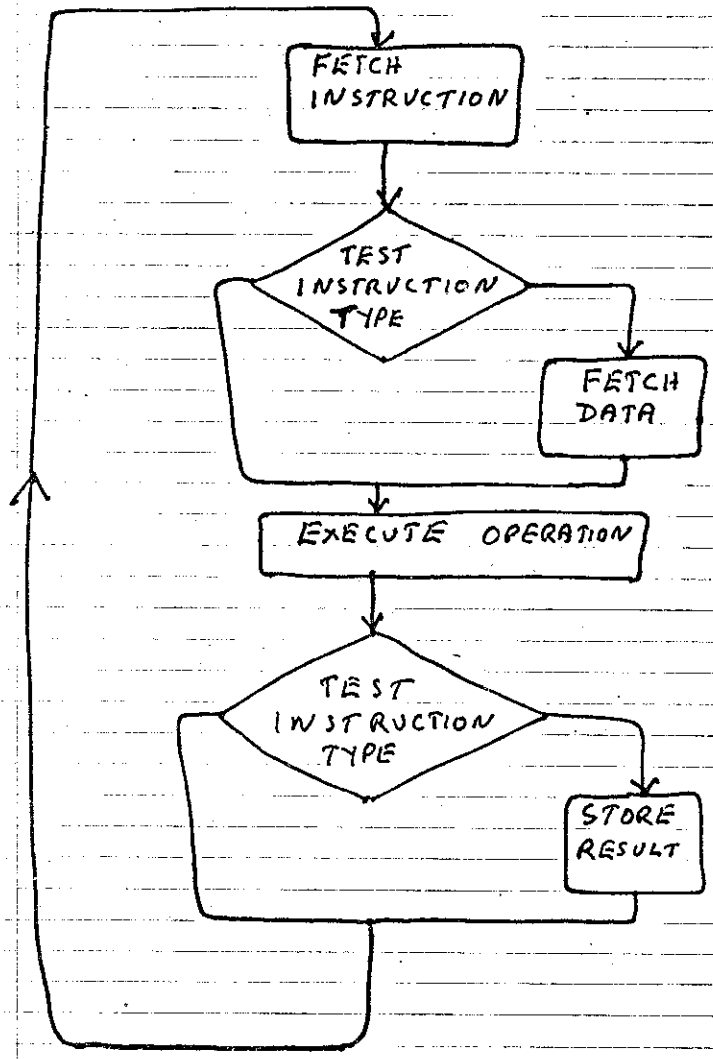
P_S ::= PROCESSOR STATE [SLIDE 35]
eg PC, A, B, IX

M_P ::= MEMORY STATE.
eg RAM, ROM, I/O Interface.

2. INFORMATION OBJECTS

- INSTRUCTIONS $P \leftarrow M$
- DATA OPERANDS $P \leftarrow M$
- RESULTS $P \rightarrow M$

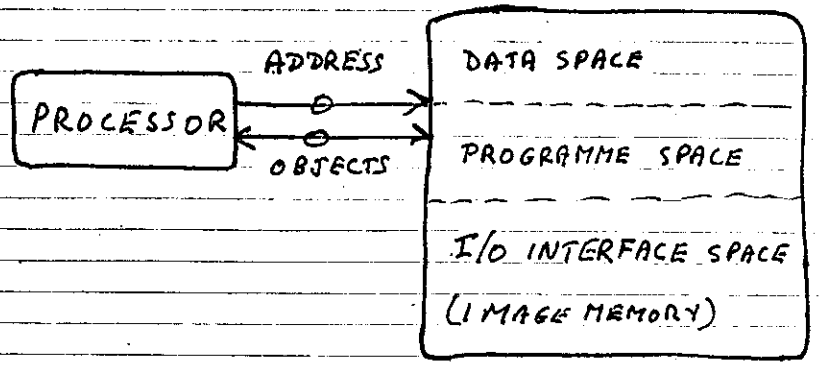
INSTRUCTION CYCLE.



CLOCK MEASURES

TIME FOR A CYCLE.

cf SLIDE 39



OCCUPANCY of ABSTRACT MEMORY SPACE.

IMAGE MEMORY

- STATIC OUTPUT
  - LAMPS
  - COMMAND REGISTER
  - OUTPUT DATA REGISTER
- STATIC INPUT
  - SWITCHES
  - STATUS REGISTER
  - INPUT DATA REGISTER.
- DYNAMIC INPUT
  - INTERRUPT FLAG.

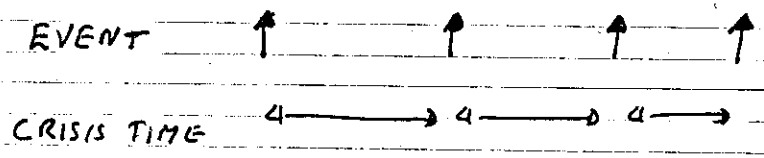
(CRISIS TIME)

OCCUPANCY of REAL IMAGE MEMORY.

CRISIS TIME.

TIME PERIOD FOLLOWING AN EVENT [Signalled by an Interrupt] DURING WHICH AN ACTION IS REQUIRED.

REGULAR OCCURANCES.

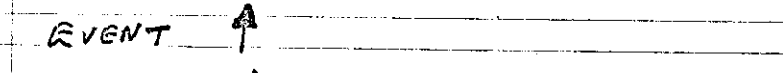


ie. BEFORE NEXT EVENT

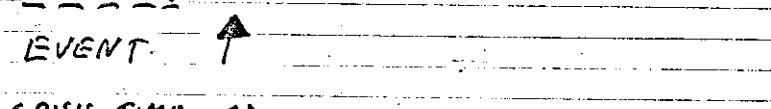
e.g. CHARACTER READ FROM A MOVING STORAGE MEDIUM such as a paper tape.

INFREQUENT OCCURANCES.

NOT URGENT



URGENT



(BEFORE THE PLANT EXPLODES).

POLLING.

PROGRAMME DESIGNED TO PAUSE AT REGULAR INTERVALS, DURING EACH PAUSE

- EXAMINE INTERRUPT FLAG
- ACT ACCORDING TO STATE of INTERRUPT FLAG.

PROGRAMMER PLANS *a priori* WHEN THE PAUSE OCCURS.

PROGRAMMER IS IN CONTROL OF EVENTS.

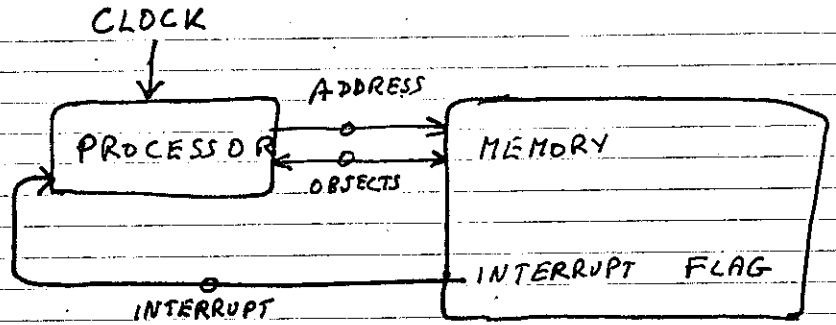
AUTOMATIC POLLING.

PROCESSOR IS DESIGNED TO EXAMINE INTERRUPT FLAG DURING EACH INSTRUCTION CYCLE

- IF SET FORCE A PAUSE
- IF NOT SET CONTINUE

PROGRAMME IS MADE TO PAUSE *a posteriori*.

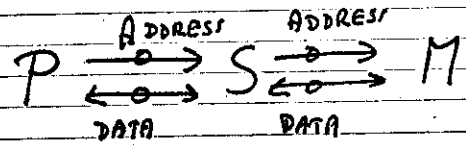
PROGRAMMER IS NOT IN CONTROL.



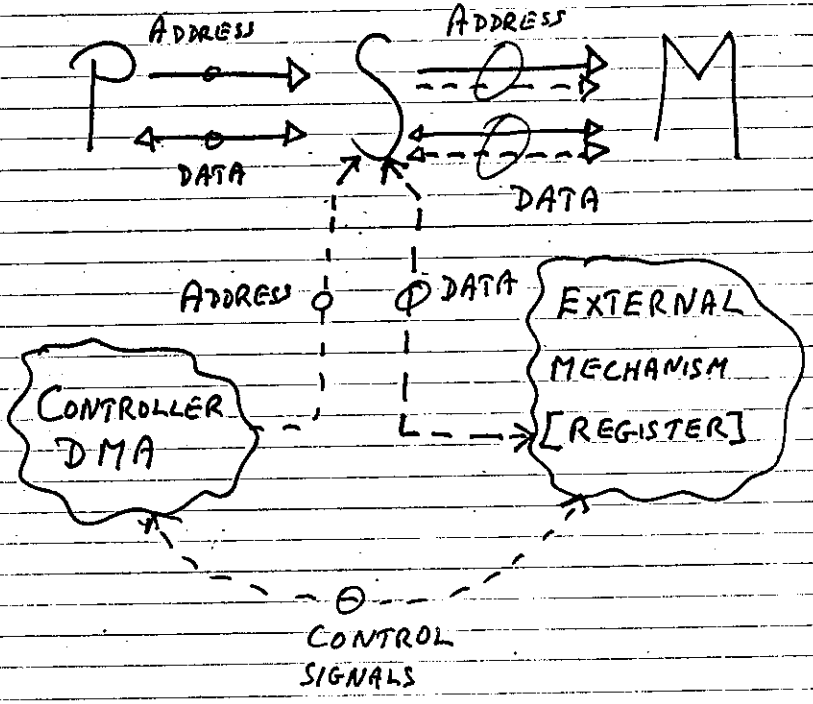
PROCESSOR - MEMORY PAIR
COMPRISE A SEQUENTIAL DOMAIN.
THE SEQUENCE IS MEASURED BY A CLOCK.

A SECOND SEQUENTIAL DOMAIN
EXISTS WITH ITS OWN CLOCK.

THESE CONCURRENT
SEQUENTIAL DOMAINS
ARE SYNCHRONISED
BY MEANS OF THE INTERRUPT
CO-OPERATION BETWEEN THEM
MANAGED BY
PROGRAMME EXECUTED IN
PROCESSOR MEMORY PAIR.



S ::= SWITCH (SUCH AS a BUS)
TO ALLOW CONSTRUCTION of
PROCESSOR - MEMORY INTERCONNECT.



SWITCH ALSO ROUTES DATA BETWEEN
MEMORY ⟷ EXTERNAL REGISTER
& ADDRESS FROM
DMA CONTROLLER → MEMORY.

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