INTERNATIONAL ATOMIC ENERGY AGENCY
UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION

INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS
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CABLE: CENTRATOM - TELEX 460392-1

SMR/90 - 27

COLLEGE ON MICROPROCESSORS:

TECHNOLOGY AND APPLICATIONS IN PHYSICS

7 September - 2 October 1981

INTEGRATED CIRCUIT TECHNOLOGY FOR THE 1980's

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SGS Technology and Service

INTRODUCTION

ESTIMATED WORLDWIDE SEMICONDUCTOR CONSUMPTION

(MILLIONS OF DOLLARS)

	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985
TOTAL SEMICONDUCTORS	5827	6846	8859	11116	14119	13763	15913	19588	23978	29093
BIPOLAR I.C.	865	1026	1315	1703	2450	2499	2890	3562	4304	5200
MOS I.C.	1239	1564	2369	3480	4921	4735	5713	7354	9412	11799
LINEAR I.C.	837	1097	1551	1943	2401	2318	2629	3205	3891	4702
TOTAL I.C.	2941	3687	5235	7126	9772	9552	11232	14121	17607	21701
TOTAL DISCRETE	2598	2850	3205	3395	3648	3537	3896	4488	5172	5922
TOTAL OPTOELECTRONICS	288	309	419	595	699	674	785	979	1199	1470

SOURCE: DATAQUEST INC.

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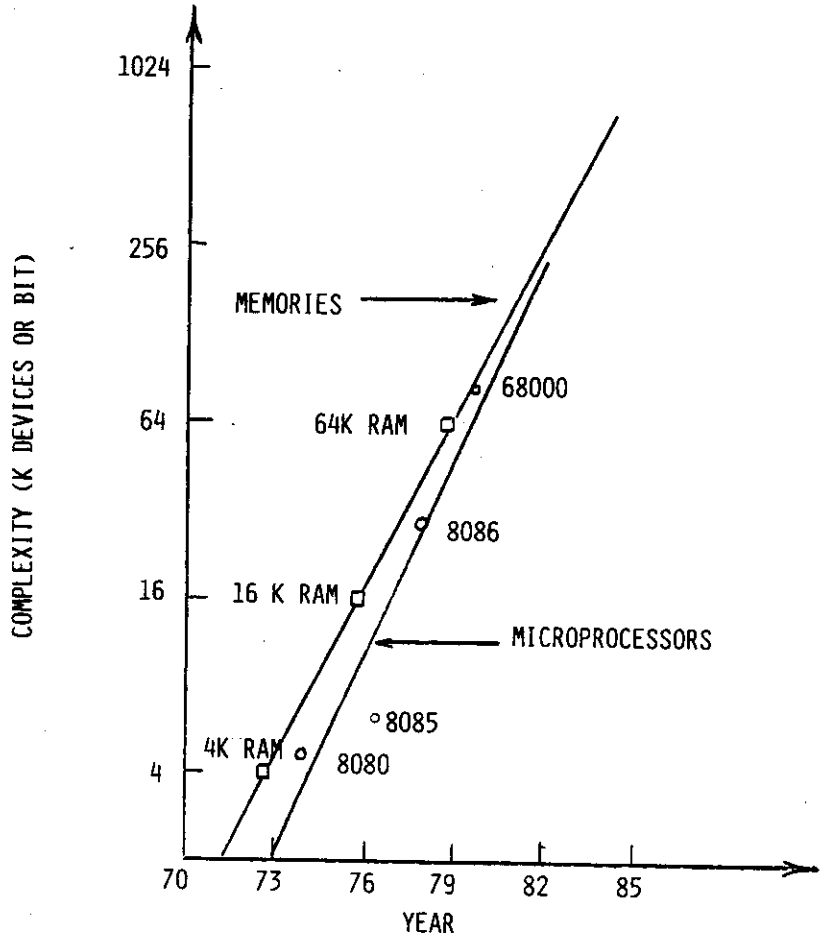
EVOLUTION IN I.C. COMPLEXITY



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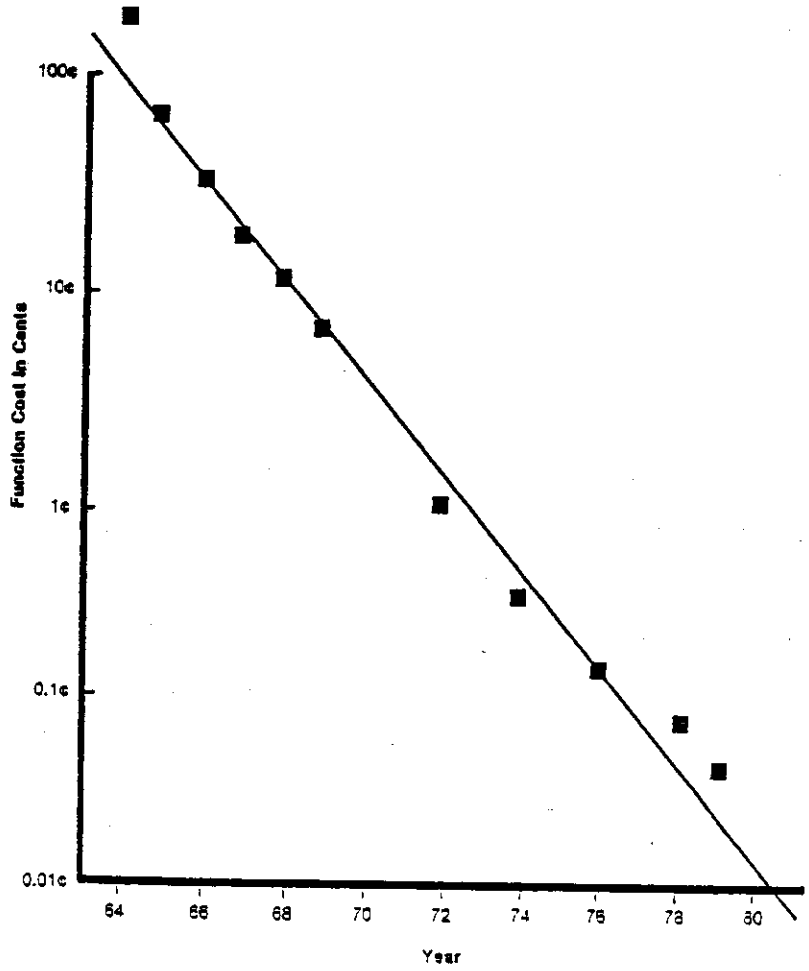
AVERAGE PRICE PER FUNCTION (ICs)



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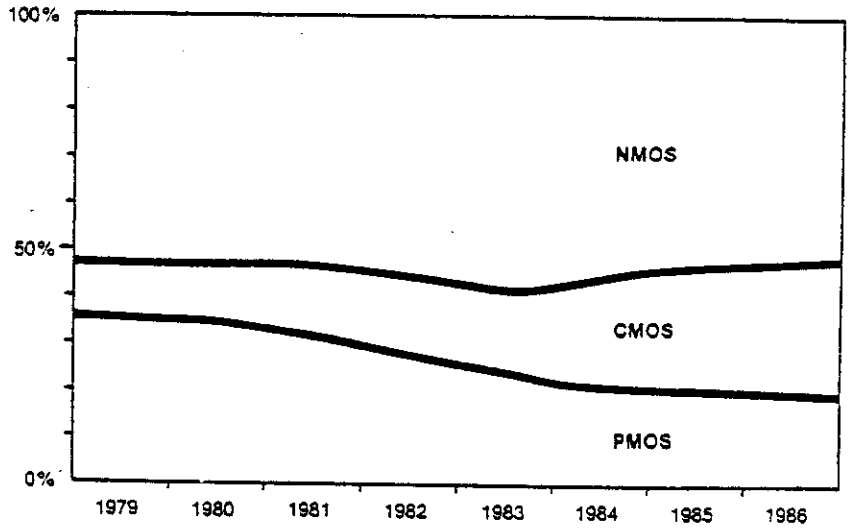
ESTIMATED MICROCOMPUTER CONSUMPTION
BY TECHNOLOGY

(DOLLARS)



FORECAST:

TOTAL 1981 : $ 690 MILLION (230 MILLION UNITS)
TOTAL 1986 : $ 2160 " (1000 " ")

SOURCE: DATAQUEST INC.

INTEGRATION TECHNOLOGIES

BIPOLAR TECHNOLOGY

PRO:

- DIGITAL AND ANALOG FUNCTIONS
- MATURE TECHNOLOGY
- LOW IMPEDANCE: CAN DRIVE LARGE CAPACITANCES AND SINK OR SOURCE LARGE CURRENTS.
- LARGE TEMPERATURE RANGE: UP TO 200°C

- HIGH GAIN

CONS:

- DEVICES ARE NOT SELF ISOLATED
- TWO LAYERS METAL IS REQUIRED
- LARGE NUMBER OF CONTACTS NEEDED
- EPITAXY DEFECTS: YIELD SENSITIVITY
- NO SELF ALIGNEMENT FEATURE

WORKHORSE BIPOLAR TECHNOLOGIES

TTL :

- GOOD DRIVE POWER
- NOT VERY DENSE

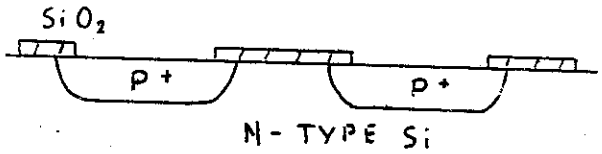
ECL (EMITTER COUPLED LOGIC):

- NON SATURATED LOGIC
- VERY FAST (SUB NANOSECOND)
- POWER DISSIPATION

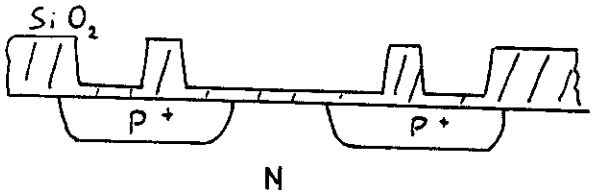
I^2L / MTL:

- VERY DENSE (2000 GATES/MM^2 AT 1.25 μM)
- VERY GOOD SPEED/POWER PRODUCT (0.3 PJ)
- DOWNSCALABLE
- HIGHER SPEED CAN BE ACHIEVED WITH SCHOTTKY ISL

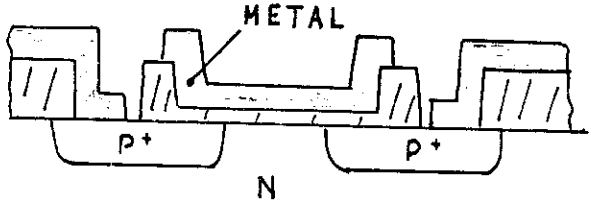
METAL GATE P CHANNEL N MOS



- N TYPE (III) MATERIAL
- 1ST MASK SOURCE AND DRAIN

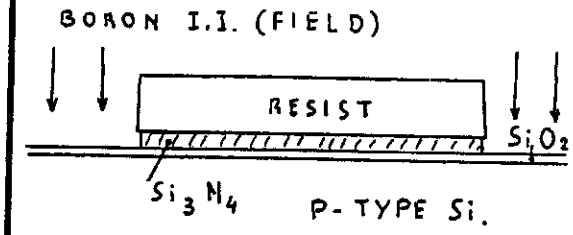


- FIELD OXIDE
- 2ND MASK
  DEV. WELL + GATE OXIDE

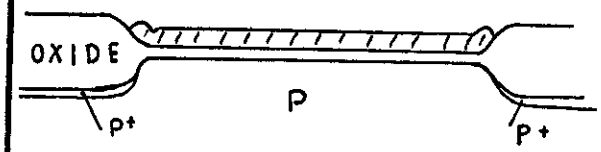


- 3RD MASK
  CONTACT OPENING
- 4TH MASK
  METAL DEFIN.
- 5TH MASK
  PROTECTION

N - CHANNEL SILICON GATE



1)



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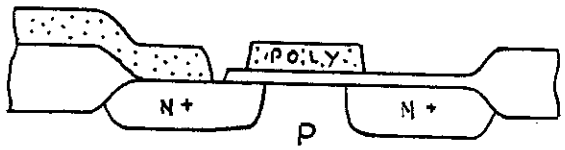
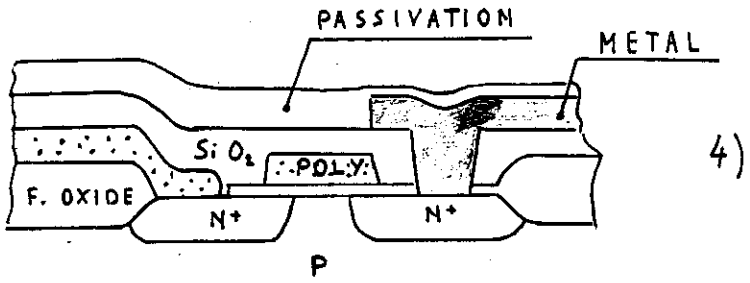


3)

N - CHANNEL SILICON GATE



4)

1) INITIAL OXIDE+NITRIDE, DEVICE WELL ETCH (1ST MASK), FIELD IMPLANT.

2) FIELD OXIDE GROWTH

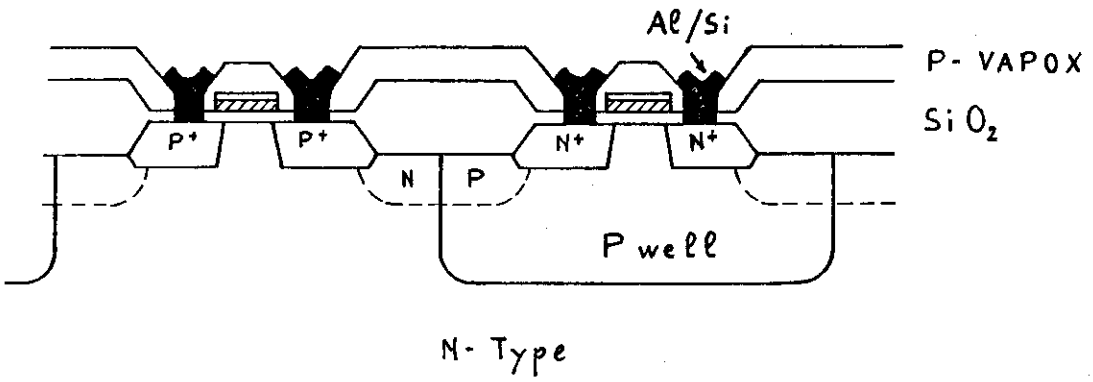
3) BURIED CONTACT (2ND MASK), POLY DEPOSITION AND DEFINITION (3RD MASK), SOURCE AND DRAIN DIFFUSION

4) SiO_2 DEPOSITION, CONTACT OPENING (4TH MASK), METAL DEPOSITION AND ETCH (5TH MASK), PASSIVATION (6TH MASK)

THE CASE FOR MOS TECHNOLOGY

- SIMPLE PROCESSING : HIGHER YIELD
- DEVICE SELF ISOLATION : HIGHER DENSITY
- INHEREN CAPACITOR : DYNAMIC CIRCUITRY
- LOW POWER CONSUMPTION : CMOS
- DOWNSCALABLE BELOW 1 /UM
- MOS TECHNOLOGY IS EVOLUTIONARY AND PREDICTABLE

C MOS SILICON GATE



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THE CASE FOR C MOS TECHNOLOGY

- C MOS TECHNOLOGY IS YOUNG COMPARED WITH N MOS.
  THERE IS PLENTY OF ROOM FOR DEVELOPMENT AND IMPROVEMENT

- C MOS HAS A WIDER SPECTRUM OF APPLICATIONS THAN N MOS (LOGIC AND ANALOG FUNCTIONS, BETTER SPEED-POWER PRODUCT, WIDER VOLTAGE RANGE, FROM FEW VOLTS TO...)

- C MOS IS DOWNSCALABLE TO 1 μM

- C MOS MAY BECOME A DOMINANT VLSI TECHNOLOGY:
  IT USES A SIGNIFICANT AMOUNT OF ENERGY ONLY WHEN SWITCHING.
  N MOS HAS A HIGHER DENSITY BUT MUST TRADE OFF SPEED FOR LOW POWER DISSIPATION

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TECHNOLOGY

PERFORMANCE AND LIMITATION

(DIGITAL CIRCUITS)

CHOICE OF TECHNOLOGY

THE CHOICE OF THE PROPER TECHNOLOGY FOR THE PROPER MARKET SEGMENT IS CRUCIAL.
THE COST OF THE WRONG DECISION IS VERY HIGH.

TECHNOLOGY PERFORMANCE:

- SPEED, POWER, SCALING POSSIBILITY

FLEXIBILITY:

- CIRCUIT AND DESIGN ADVANTAGES AND LIMITATIONS

COST:

- NUMBER OF PROCESSING STEPS, YIELDS ACHIEVABLE WITH A GIVEN DICE SIZE

MANUFACTURABILITY:

- MINIMUM NUMBER OF PROCESS STEPS
- PREVIOUS EXPERIENCE

PERFORMANCE MEASUREMENT OF I.C.'s:SPEED, COMPLEXITY AND POWER

- THE UTILITY OF A COMPLEX I.C. DEPENDS ON THE PRODUCT OF DENSITY AND SPEED: FUNCTIONAL THROUGHPUT RATE (F.T.R.)

F.T.R. - EQUIVALENT LOGIC GATES PER CHIPS X CLOCK RATE OF GATE

- PRESENT : F.T.R. $\simeq 1 \times 10^4$ TO 2×10^5 GATE - MHz
- FUTURE : F.T.R. $> 10^7$ GATE - MHz (WITH MINIMUM DIMENSIONS IN THE RANGE 0.5 - 0.8 μM)
- F.T.R. INCREASE MUST BE OBTAINED KEEPING TOTAL POWER DISSIPATED PER PACKAGE WITHIN REASONABLE LIMITS (FEW WATTS FOR CHIP)

THREE WAYS TO INCREASE F.T.R. (UTILITY OF A VLSI CIRCUIT)

1. INCREASE OF CHIP AREA
   - THIS WAY IS LIMITED IN POTENTIAL DUE TO THE COUPLING BETWEEN CHIP AREA AND PROBE YIELD. F.T.R. COULD INCREASE OF A FACTOR TWO (DOUBLING OF CHIP AREA).

2. DEVICE/CIRCUIT CLEVERNESS
   - HAS CONTRIBUTED SUBSTANTIALLY F.T.R. INCREASE IN THE PAST (E.G. A SIX-TRANSISTOR MEMORY CELL HAS EVOLVED INTO ONE-TRANSISTOR CELL).
   - HOWEVER IT IS DIFFICULT TO INVENT TO SCHEDULE AND FUTURE CONTRIBUTION DUE TO CLEVERNESS ARE NOT PREDICTABLE. ALTHOUGH WORTH ADDRESSING STEP FUNCTION IMPROVEMENTS (ONE ORDER OF MAGNITUDE) ARE NOT IN SIGHT.

3. SCALING

. SCALING OFFERS THE GREATEST POTENTIAL FOR F.T.R. INCREASE

. IN THE EVOLUTION OF THE MOS DINAMIC RAM FROM 1 K TO 64 K. INCREASE IN CHIP AREA, CLEVERNESS AND SCALING HAVE ACCOUNTED AS FOLLOW:

CHIP AREA	: 1.65
CLEVERNESS	: $\simeq 3$
SCALING	: < 10

. SCALING OF THE MINIMUM DIMENSIONS IN AN EVOLUTIONARY PROCESS AND IT IS LARGELY PREDICTABLE.

HOW TO INCREASE DIE AREA

YIELD AND POWER DISSIPATION ARE THE PROBLEMS.

ENPHASYS SHOULD BE ON:

. REDUCED DEFECTS IN PROCESSING

. SELF DIAGNOSTIC AND CORRECTING CIRCUITS

. ON CHIP REDUNDANCY

. LOW POWER DISSIPATION TECHNOLOGY SUCH AS CMOS

SCALING

. FOR SCALING FACTOR S > 1 PARAMETERS BECOME:

PARAMETER	SCALING FACTOR
OXIDE THICKNESS	1/S
LATERAL DIMENS.	1/S
SUBSTRATE DOPING	S
VOLTAGE	1/S
CURRENT	1/S

ADVANTAGES (LOCAL DEVICE)		LIMITATIONS (LOCAL DEVICE)	
DEVICE DENSITY	S^2	LINE RESISTANCE	$S \div S^2$
DEVICE SPEED	S	CONTACT RESISTANCE	S^2
DEVICE POWER	$1/S^2$	METAL MIGRATION	S^4
DEVICE COST	$1/S^2$	CURRENT DENSITY	S

SCALING LIMITATIONS

SCALING IS AN EFFECTIVE WAY TO INCREASE CHIP CAPACITY WITH EXISTING TECHNOLOGIES

MAJOR LIMITATIONS ARE:

MAXIMUM POWER:

- LOWER VOLTAGES ARE NEEDED *
- CMOS TECHNOLOGY HAS ADVANTAGES

INTERNAL WIRE DELAY:

- NEW INTERCONNECT MATERIALS (SILICIDES)
- CAREFUL SYSTEM PARTITIONING

MANUFACTURABILITY:

- BETTER MATERIALS
- IMPROVED PROCESS CONTROL
- PROCESS SIMULATION TOOLS (CAD)

LIMITS TO SCALING (NEAR FUTURE)

ALTHOUGH CHANNEL LENGTH DOWN TO $< 1/4$ μM HAS BEEN SHOWN FEASABLE, PRACTICAL CONSIDERATIONS WILL KEEP CHANNEL LENGTH $\simeq 1$ μM AND GATE OXIDE $\simeq 150$ A°

* DISSIPATION AND HOT ELECTRONS

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FACTORS CONTRIBUTING TO INCREASED DENSITY

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MAJOR PROCESS AND MANUFACTURING TRENDS

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PROCESS AND EQUIPMENT EVOLUTION

YEAR	PROCESS	PRODUCT	MAJOR EQUIPMENT
1962	METAL GATE PMOS	-	-
1969	SI GATE PMOS	256 BIT RAM	·CVD POLY ·CVD OXIDE
1971	SI GATE NMOS	1 K RAM	
1974	SI GATE NMOS	4 K RAM	·CVD NITRIDE ·ION IMPLANT
1976	SI GATE NMOS	16 K RAM	
1979	SI GATE NMOS	64 K RAM	:PARALLEL PLATE PLASMA ETCHER ·WAFER STEPPER

. NEW TYPE OF EQUIPMENT HAS BEEN INTRODUCED EVERY SECOND GENERATION OF DYNAMIC RAM's

. ENPHASYS HAS SHIFTED FROM DEPOSITION / DOPING TO PRINTING AND PATTERNING

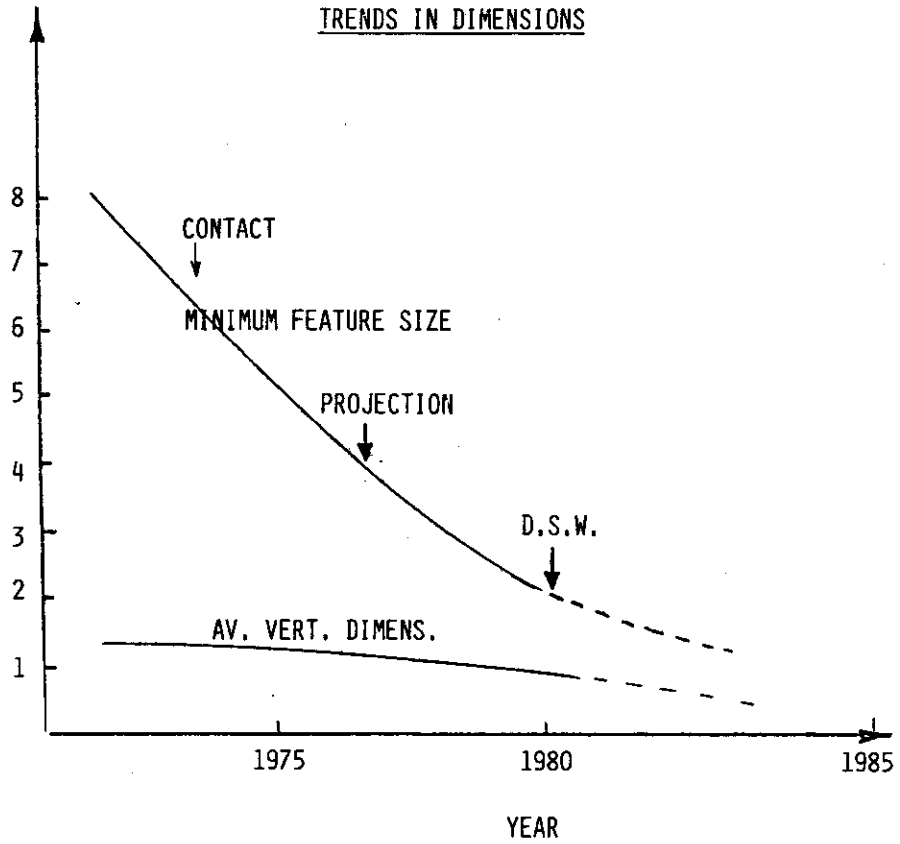
MAJOR PROCESS TRENDS IN THE 1980'S

INCREASED DIE SIZE AND SCALING OF HORIZONTAL AND VERTICAL DIMENSIONS CALL FOR IMPROVEMENTS IN THE FOLLOWING AREAS:

- PHOTOLITHOGRAPHY (ALIGNEMENT AND EXPOSURE)
- PATTERNING (FINE LINE DEFINITION BY ANISOTHROPIC ETCHING)
- LOW TEMPERATURE PROCESSING
- CONTACT AND INTERCONNECT TECHNOLOGY

CAPITAL COSTS AND EQUIPMENT AVAILABILITY WILL CONDITION THE RATE OF IMPROVEMENT.

TRENDS IN DIMENSIONS



PHOTOLITHOGRAPHY

- PRODUCTION FEATURE SIZE HAS SHRANK ≃ 1 /uM EVERY TWO YEARS FROM 20 MICROMETER IN 1965 TO 3 MICROMETER IN 1980.
- THE 1 MICRON BARRIER CROSSING IS EXPECTED IN THE MID 1980-s
- REPRODUCIBILITY AND REGISTRATION WILL BE MORE IMPORTANT THAN RESOLUTION.
- DIRECT STEP ON WAFER WITH LOCAL ALIGNEMENT WILL DOMINATE, IN THE 80's
- ELECTRON BEAM SYSTEMS WILL BE MAINLY USED FOR MASK MAKING, QUICK TURNAROUND CIRCUITS AND DEVELOPMENT

PHOTOLITHOGRAFY EQUIPMENT

	CONTACT-PROXIMITY	PROJECTION	DIRECT-STEP	E-BEAM
COST	100 K $	280 K $	600 K $	2000 K $
WAFERS/HR	60	40	30(1)	5-10
RESOLUTION	3 /uM	3 /uM	< 2 /uM	0.5 /uM

(1) DEPENDING ON DICE SIZE

SUMMARY

INTEGRATED CIRCUIT (VLSI) TECHNOLOGIES FOR THE 1980'S

- SCALING THEORY PREDICTS THE POTENTIAL FOR MORE THEN TWO ORDER OF MAGNITUDE INCREASE IN FTR (FUNCTIONAL THROUGHPUT RATE).
- SCALING WILL CALL FOR LOWER SUPPLY VOLTAGE. A NEW STANDARD IS NEEDED AFTER THE 5 VOLT ERA.
- CHIP CAPACITY WILL INCREASE MORE IN THE NUMBER OF ELEMENTS PER CHIP THAN IN SPEED.
  SYSTEMS WITH HIGHER DEGREE OF PARALLELISM WILL BE PRODUCED
- MOS AND BIPOLAR TECHNOLOGIES TEND TO CONVERGE AT THE 1 MICRON LEVEL IN THERMS OF BOTH PERFORMANCE (F.T.R.) AND PROCESSES.
- C MOS TECHNOLOGY IS LESS RESTRICTED IN THERMS OF POWER DISSIPATION THAN BIPOLAR AND NMOS TECHNOLOGIES.
  IT MAY BECOME THE DOMINANT TECHNOLOGY
- PRINTING PATTERNING AND INTERCONNECT TECHNOLOGIES WILL DOMINATE

- PROCESS AUTOMATION AND MANUFACTURING CONTROL WILL BE OF PARAMOUNT IMPORTANCE.

- THE RATE OF IMPROVEMENT WILL BE LIMITED BY CAPITAL COSTS AND SHORTAGE OF SUPERIOR TECHNICAL SKILL