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COLLEGE ON MICROPROCESSORS:

TECHNOLOGY AND APPLICATIONS IN PHYSICS

7 September - 2 October 1981

APPLICATIONS OF MICROPROCESSOR PERIPHERALS

1) Digital to analog converter
2) Programmable timer

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APPLICATIONS

of MICROPROCESSOR PERIPHERALS

1) Digital to Analog Converter.

2) Programmable Timer.

Digital To Analog Converter (D/A)

- Signals which may assume any value in a continuous range are called analog signals.

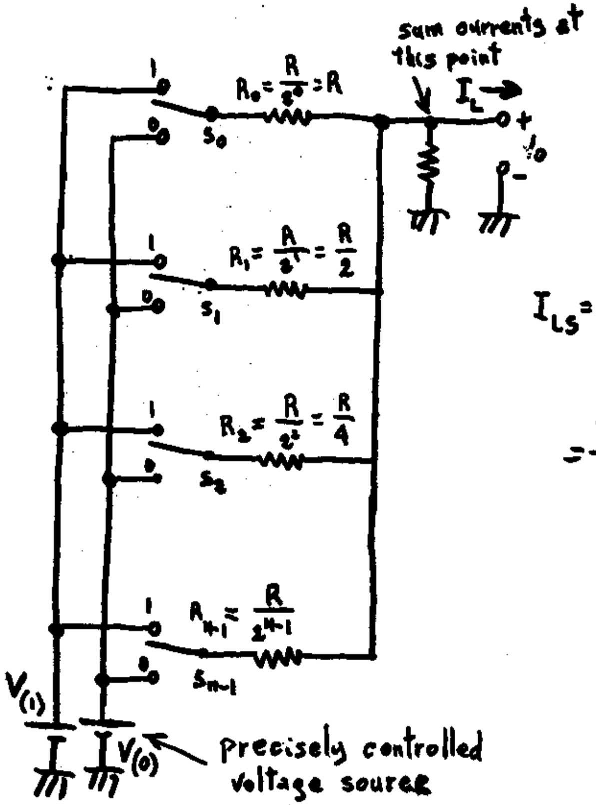
- When analog signals must be processed, there is often a great advantage in converting the signal to digital form so that the processing can be done digitally.

- A most effective way of suppressing noise is to transmit the signal digitally. A communication system which operates in this way, i.e. converts the analog signal to digital form and then reconstitutes the analog signal, is called a "pulse-code modulation system".

- The D/A converters are rather simpler than the A/D converters. A D/A converter is frequently used within the structure of D/A converters. For these reasons we shall consider D/A converters first.

Example of a circuit converting digital representation to analog form.

THE WEIGHTED-RESISTOR D/A Converter



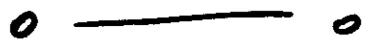
$$I_{LS} = V_R\left(\frac{S_{N-1}}{R_{N-1}} + \frac{S_{N-2}}{R_{N-2}} + \cdots \frac{S_0}{R_0}\right)$$

$$= \frac{V_R}{R}\left(S_{N-1}2^{N-1} + S_{N-2}2^{N-2} + \cdots + S_0 2^0\right)$$

-Let us assume that $V_{(1)} = V_R$, a fixed reference voltage, that $V_{(0)} = 0$, that is, all 0 switch positions are grounded and that the load $R_L = 0$ (in which case $V = 0$). Then the output current I_L is readily calculated in terms of the switch positions.

Other circuits converting digital representation to analog form

- The R-2R LADDER D/A Converter.
- The Inverted LADDER D/A Converter.



SWITCHES FOR D/A Converters

- Bipolar transistors
- FETs

CURRENT AND VOLTAGE DRIVEN D/A

- The current-driven converter has a potential merit in comparison with the voltage-driven converter.

- The voltage driven converter requires transistor switches which are driven to saturation. The time delay associated with bringing a transistor out of the saturation often establishes an upper limit to the speed with which such voltage-driven converters can operate.

- In current driven converters it is feasible to use a switching arrangement in which transistors are not driven into and out of saturation.

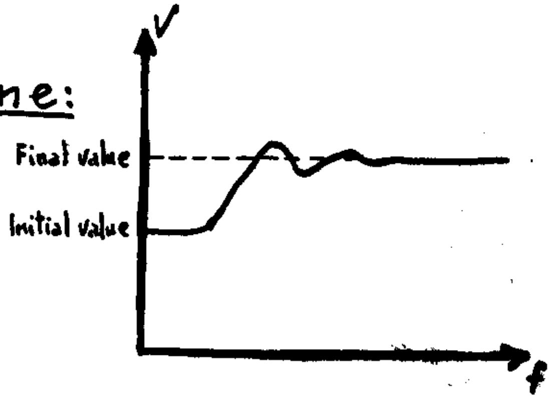
SPECIFICATIONS for a D/A converter

Resolution: This term specifies the number of bits the converter can accommodate and correspondingly the number of output voltage (or currents). i.e. the number of possible output voltages of a converter which can accept 10 input bits is $2^{10} = 1{,}024$. The smallest possible output change in output voltage is $\frac{1}{1024}$ of full scale output range. ~ resolution 1 part in 1000 or 0.1 percent.

Linearity: In an ideal D/A converter equal increments in the numerical significance of the digital-input should yield equal increments in the analog output.

Accuracy : The accuracy of a converter is a measure of the difference between the actual analog output voltage and what the output should be in the ideal case. Lack of linearity contributes to inaccuracy.

Settling time:



When the digital input to a converter changes, switches open and close and abrupt voltage changes appear.
Not only there is a finite time required to reach the new output level, but also an oscillation may occur.

The interval that elapses from the input change to the time when the output has come close enough to its final value is called the settling time. The settling time depends, among other things, on how we define "close enough". Typically a general purpose converter might have a settling time given as "500 ns to 0.2% full scale"

Temperature sensitivity: At any fixed digital input, the analog output will vary with temperature.

ANALOG TO DIGITAL Converter (A/D)

- There is a very large number of A/D converters described in the literature (a good number of which are available comercially)

Comparison of converter Types:

Converters whose speed of operation lies in three different ranges:

1) Fastest is the comparator converter.

In principle, except for the delay through the comparators, this converter makes available a digital output at the moment the analog input is applied. Hence, this converter is the system of choice where maximum speed is required. If the hardware requirements of a straightforward comparator converter become excessive, a cascade arrangement can be used with some sacrifice in speed and accuracy.

2) Next in order of speed is the successive-approximation converter

Where a relatively fast converter of good quality is required, this converter is by far the most popular.

3) Counter converters are the slowest.

The time required to process a conversion increases linearly with the power of the number of bits, requiring about as many clock pulses as the largest number. This type of converter is widely used in instruments such as digital voltmeters, where conversion speed is not important.

Beyond these comparators which are the most popular, there are almost limitless other types, some differing in principle and some only in detail. A list of some which have the merit of simplicity and economy, could be this:

- A Converter using Voltage-To-Frequency Conversion operates by counting the cycles of a variable frequency source for a fixed period
- A Converter using Voltage-To-Time Conversion operates on the principle of counting the cycles of a fixed-frequency source for a variable period.

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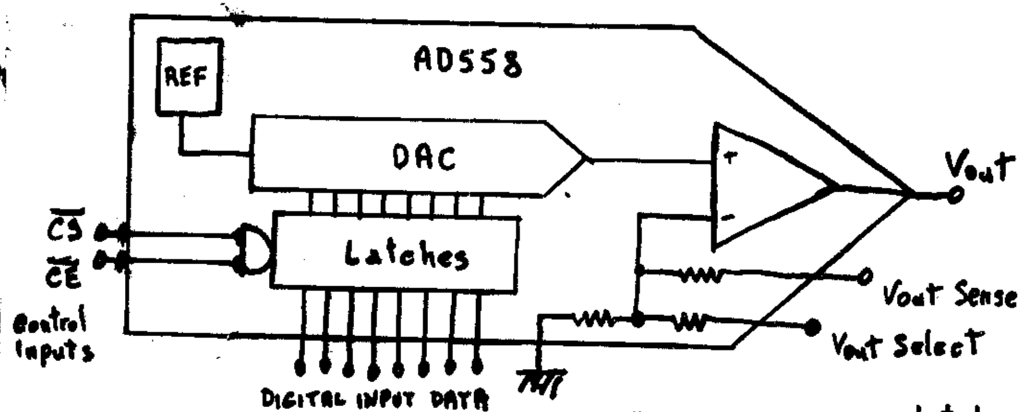
Digital-To-Analog Converter AD558J

Dacport - Lowcost μP-compatible 8-Bit DAC

Product Highlights:

- 8 Bit input register microprocessor compatible. The latch may be desabled for direct DAC interfacing.
- Power supply: >+4,5Volt → 0Volt to 2.56 Volt or 11,4V To 16,5V → 0 Volt to 10 Volt output ranges by pin-strapping.
- Settling time: 700 nsec to 0,2% full scale (2,56Volt)
- Accuracy @ 25°C ±1.5LSB (±0,6% max) full scale



The $\overline{CS}$ and $\overline{CE}$ inputs are interchangeable.

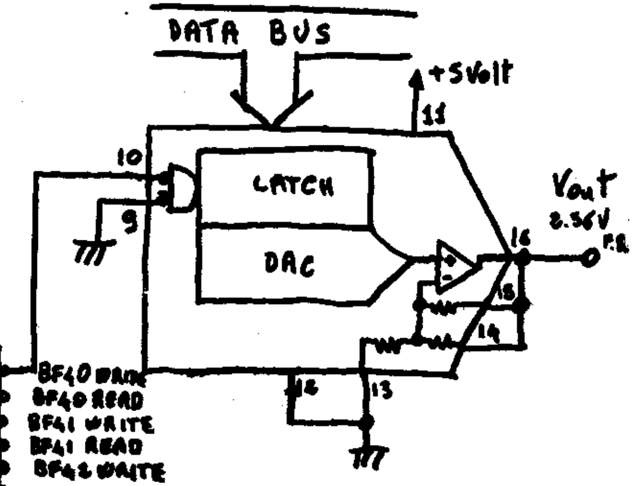
Input data	$\overline{CE}$	$\overline{CS}$	DAC data	Latch Condition
0	0	0	0	Transparent
1	0	0	1	Transparent
0	↑	0	0	latching
1	↑	0	1	latching
0	0	↑	0	latching
1	0	↑	1	latching
X	1	X	prev. data	latched
X	X	1	prev. data	latched

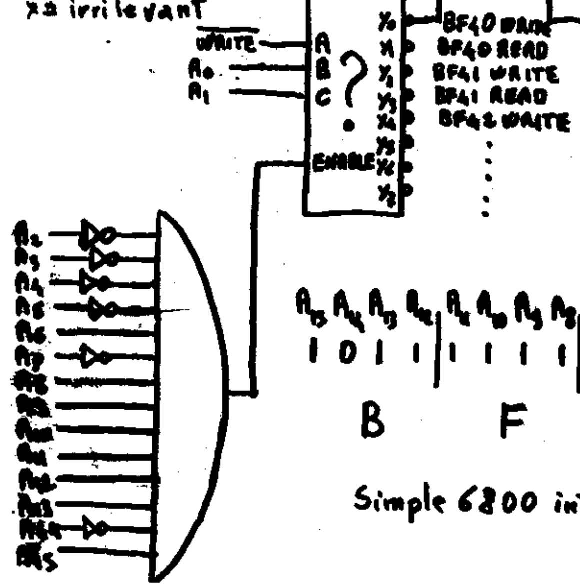
X = does not matter
↑ = Positive going transition.

Connecting the D/A AD558

ENABLE	Select			Outputs							
E	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L	x	x	x	H	H	H	H	H	H	H	H
H	L	L	L	L	H	H	H	H	H	H	H
H	L	L	H	H	L	H	H	H	H	H	H
H	L	H	L	H	H	L	H	H	H	H	H
H	L	H	H	H	H	H	L	H	H	H	H
H	H	L	L	H	H	H	H	L	H	H	H
H	H	L	H	H	H	H	H	H	L	H	H
H	H	H	L	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	H	L

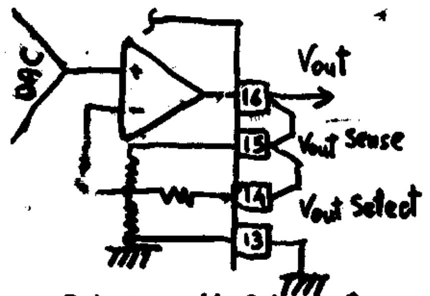
H = high level
L = low level
x = irrilevant



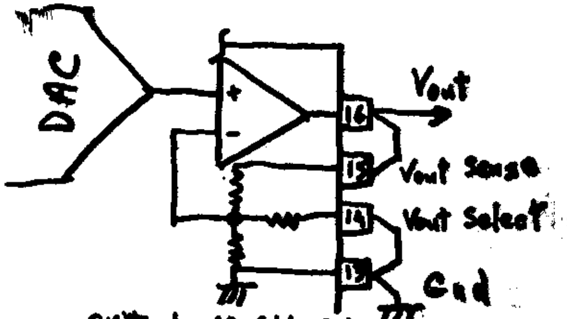


A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0
B				F				4				0			

Simple 6800 interface. Functional scheme



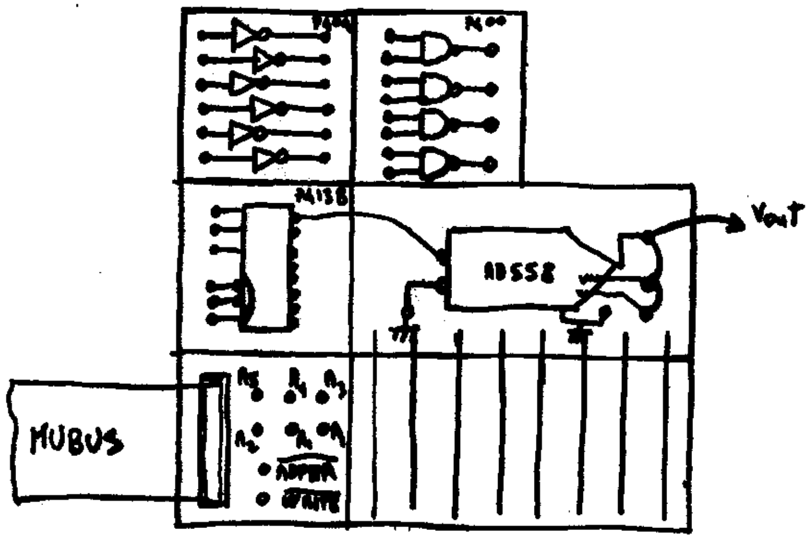
0 to 2,56 Volt Output Range
10 mVolt = 1 LSB



0 Volt to 10 Volt Output Range
40mV = 1 LSB

The functional diagram in the previous tranparency, can be implemented using the following circuits:

DECODER	$\overline{ADPER}$	REFERENCES	– partial decoding – Rosy circuit board W. VONRAVEDEN –
	74LS138		– TTL Texas Data Book p. 7-135
	AD558		– ANALOG DEVICE Data sheet



Wiring diagram. DAC mode (0-2,56 Volt)

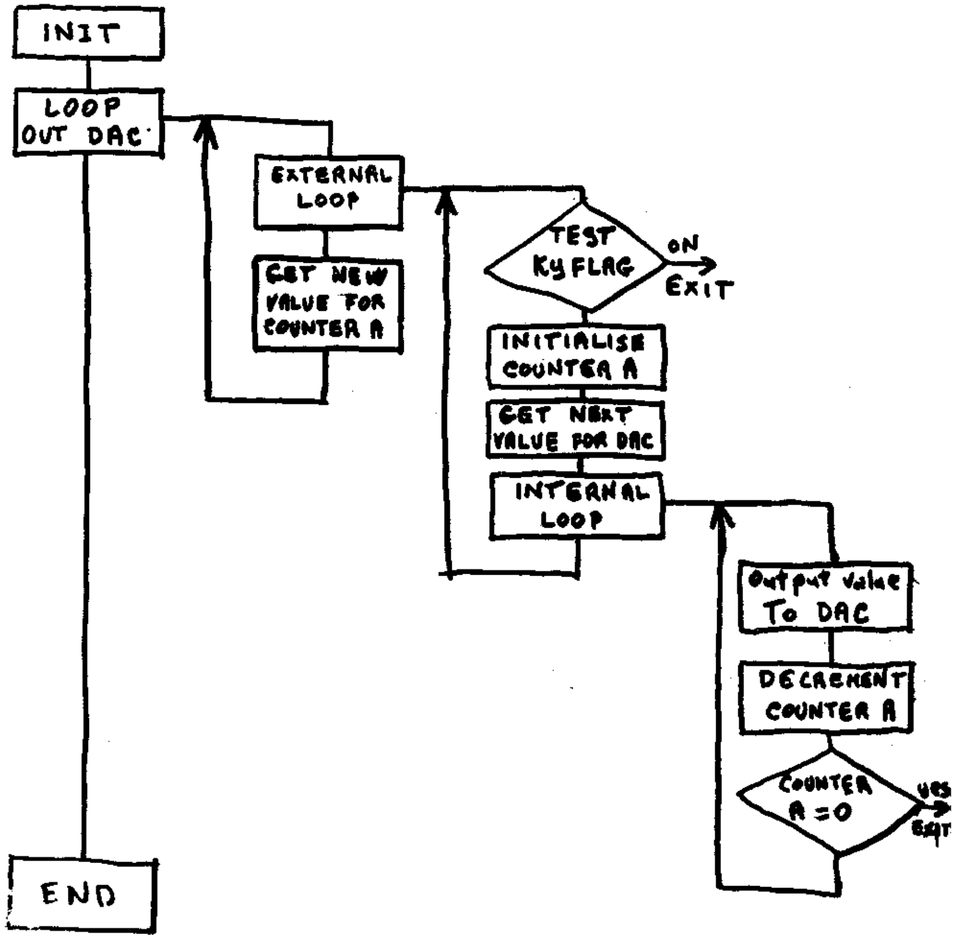
The switch is open in DAC mod (Down)

Exercise N° 8.1

The purpose of this experiment is to test the Digital to Analog converter interface.

Write a program which generate a sawtooth voltage waveform on an oscilloscope.

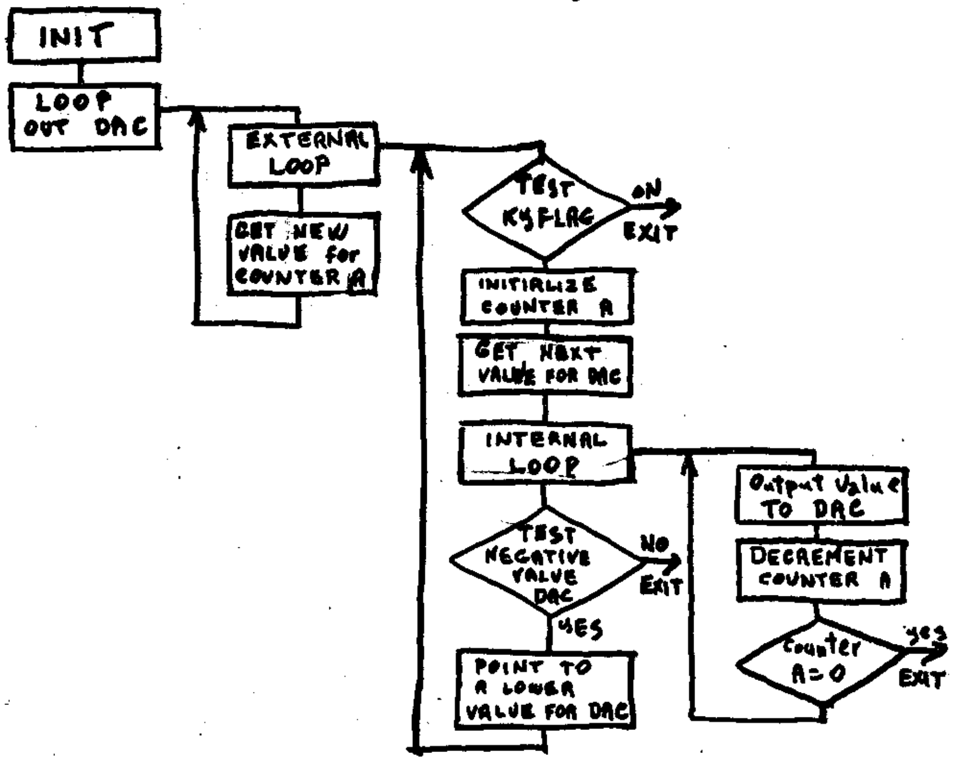
The frequency of the waveform can be selected by pressing the Key from 0 To F on the Keyboard of the Kit.



Exercise N° 8.2

Write a program to generate a triangular voltage waveform on an oscilloscope.

The frequency of the waveform can be selected by pressing the Key from "0" to "F" on the Keyboard of the Kit.

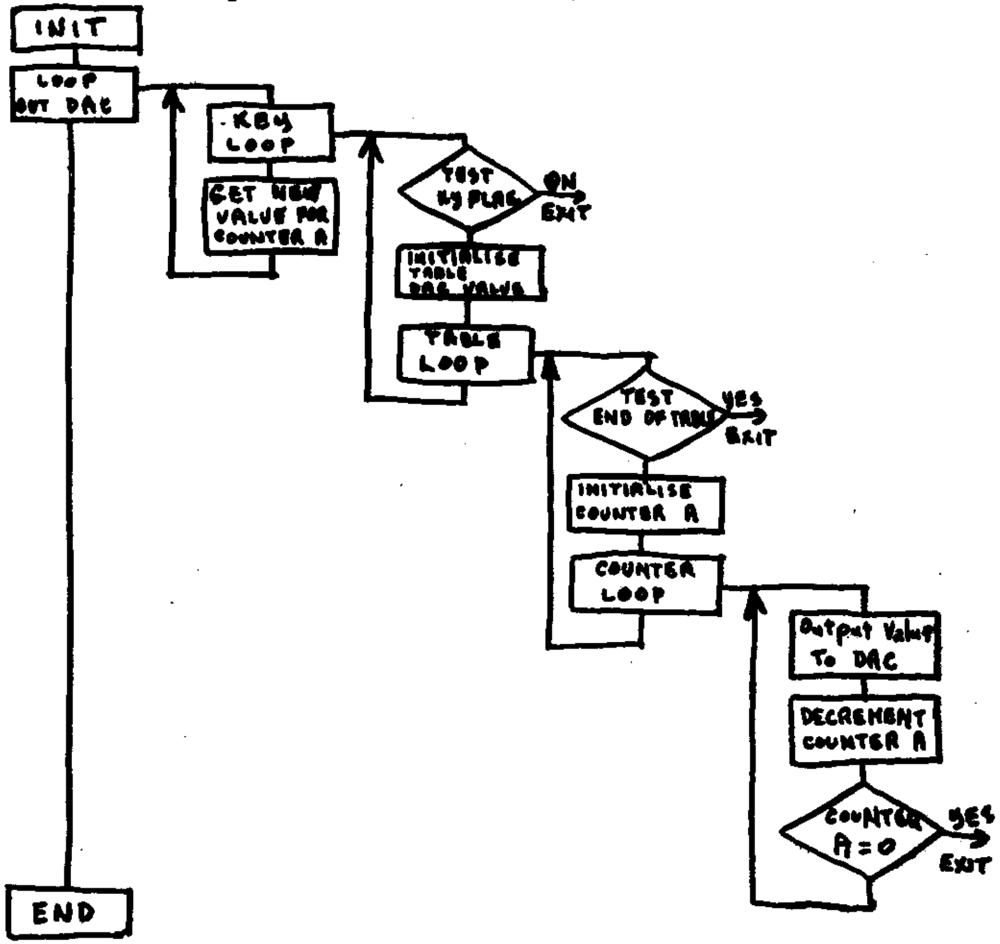


Exercise N° 8.3

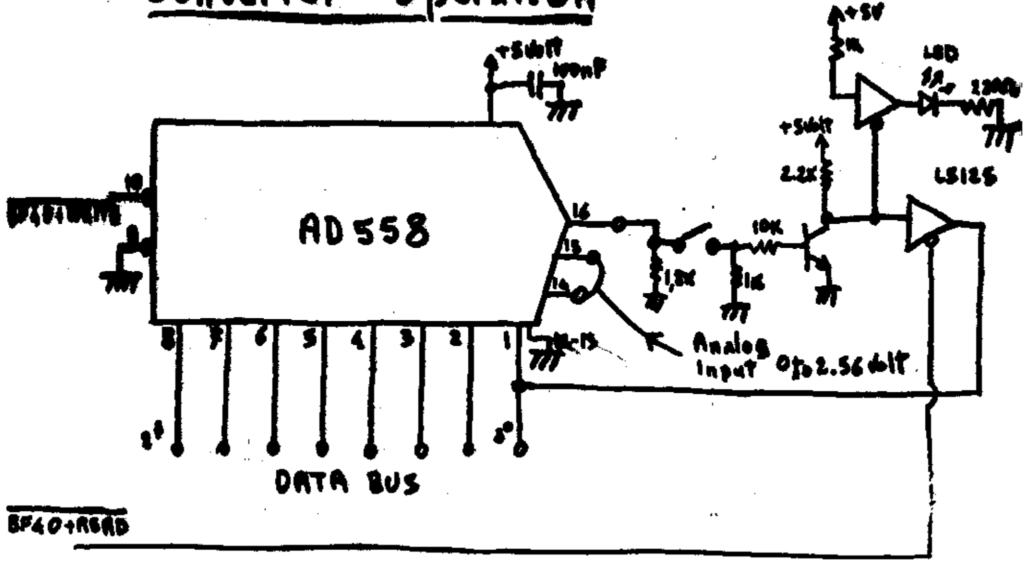
Write a program which generate a sinusoidal voltage waveform on an oscilloscope.

The frequency of the waveform can be selected by pressing the Key from "0" to "F" of the Kit.

Make use of a look-up table. The values (sin x) corresponding to a sinusoidal waveform has being stored previously in a table in memory.



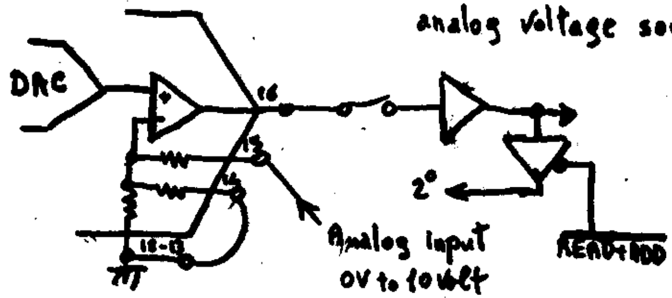
Connecting the D/A (AD558) in A/D Converter Operation



Simple 6800 interface (0 Volt to 2.56 Volt)

The switch is closed in A/D mode (UP)

Make use of the potentiometer on the logidule motor module as analog voltage source.



Connections 0 Volt to 10 Volt

Exercise Nº 8.4

- Write a program which determine the digital value of an unknown analog voltage.

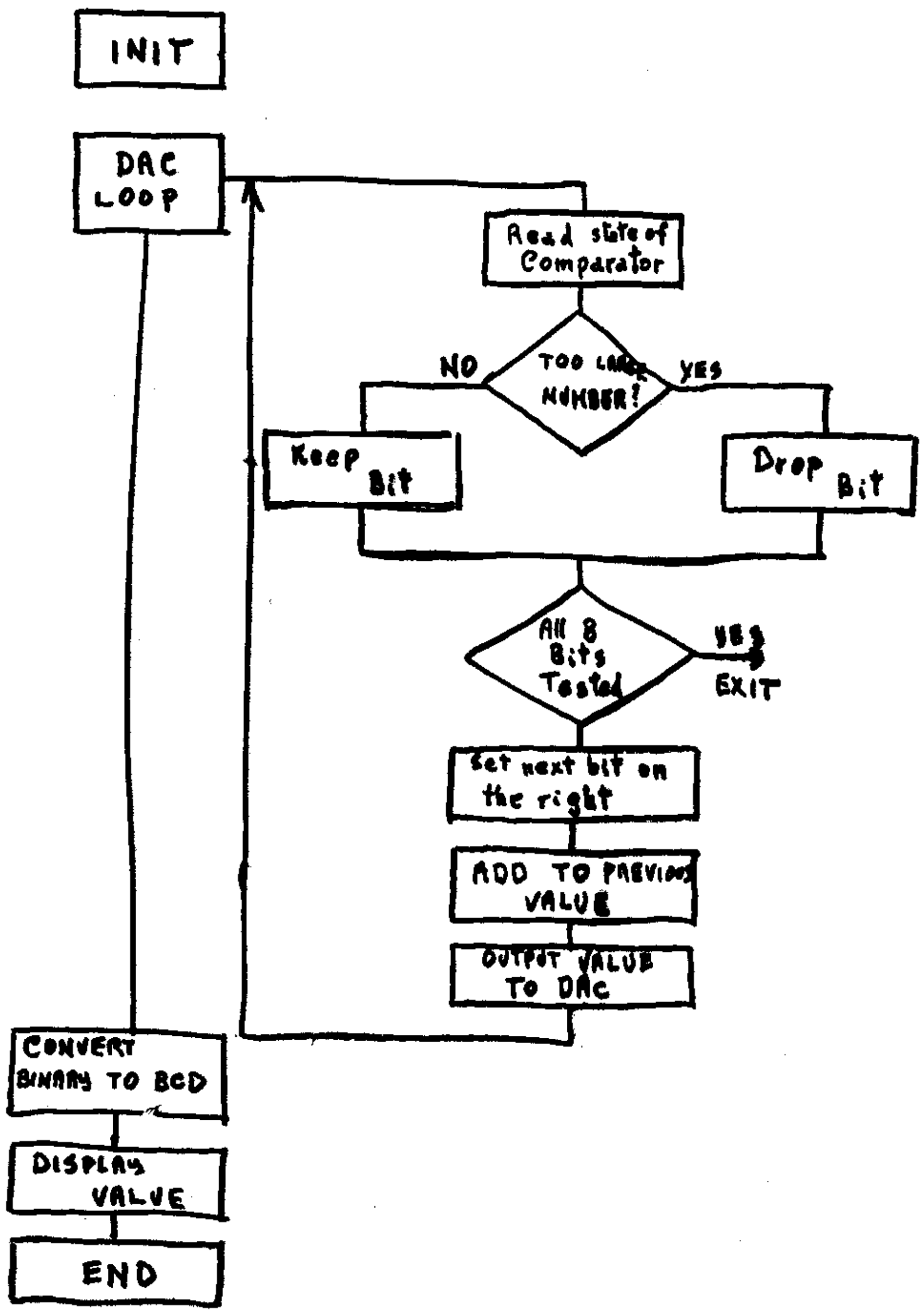
- Make use of the successive approximation techique.
- The result should be in binary form in a memory location.
- Display the value on a seven segment display of the logidule (Make use of the routine CBCDB in the library M68LIB The routine CBCDB converts a binary value in ACC A in BCD. The result is given in ACC B (+100; ACC A).

The successive-approximation algorithm has the advantages of fixed conversion time regardless of analog input signal magnitude and reasonably fast conversion times.

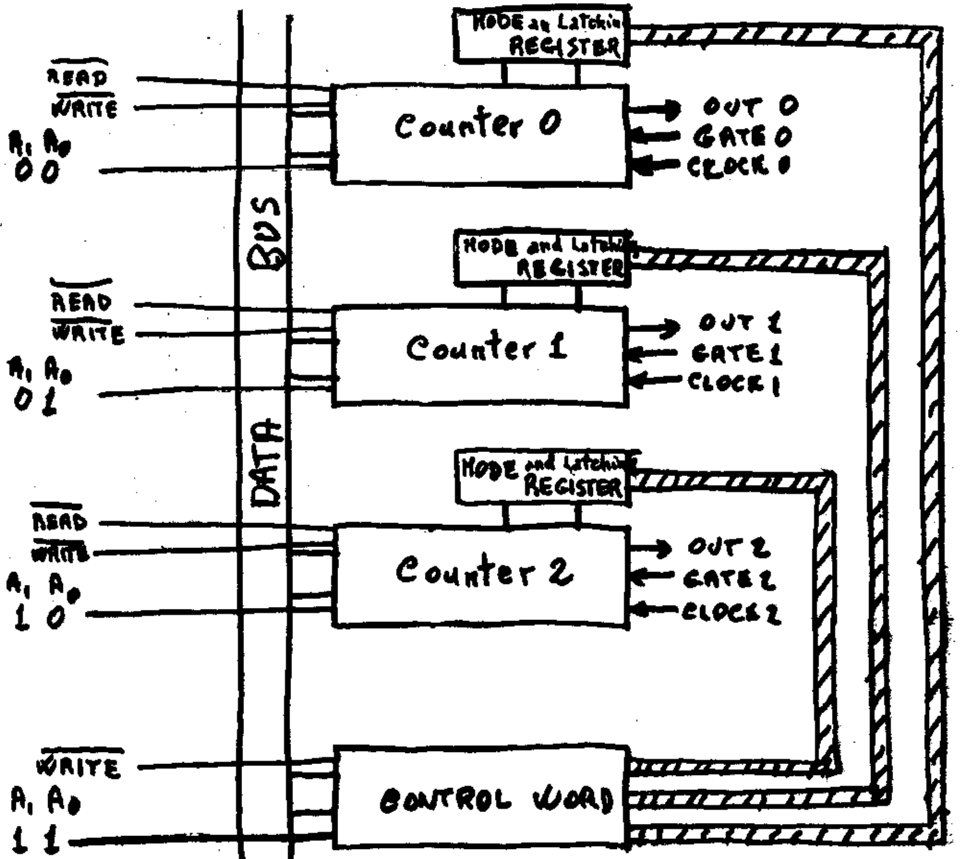
The algorithm consists of testing the MSB (most-significant bit), to determine whether the signal resides above or below middle. The result of this test determines whether the MSB should be Kept or dropped. If it is Kept, the next test is whether the signal is above or below 3/4 of full scale; if the MSB was dropped, the test is done at 1/4 full scale.

This process repeats until all eight bits have been exercised.

Exercise Nº 8.4



PROGRAMMABLE TIMER 8253



$\overline{RD}$	$\overline{WR}$	A_1	A_0	
1	0	0	0	Load counter 0
1	0	0	1	Load counter 1
1	0	1	0	Load counter 2
1	0	1	1	Write Control Word
0	1	0	0	Read counter 0
0	1	0	1	Read counter 1
0	1	1	0	Read counter 2

	SC1	SC0	RL1	RL0	Mode 3 →			BCD
CWTIMØ =	0	0	1	1	1	1	1	1

OPERATIONAL DESCRIPTION

General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the 8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. (A0, A1 = 11)

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition of Control

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL — Read/Load:

RL1	RL0	
0	0	Counter Latching operation (see READ/WRITE Procedure Section)
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

MODE Definition

MODE 0: Interrupt on Terminal Count. The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

(1) Write 1st byte stops the current counting.
(2) Write 2nd byte starts the new count.

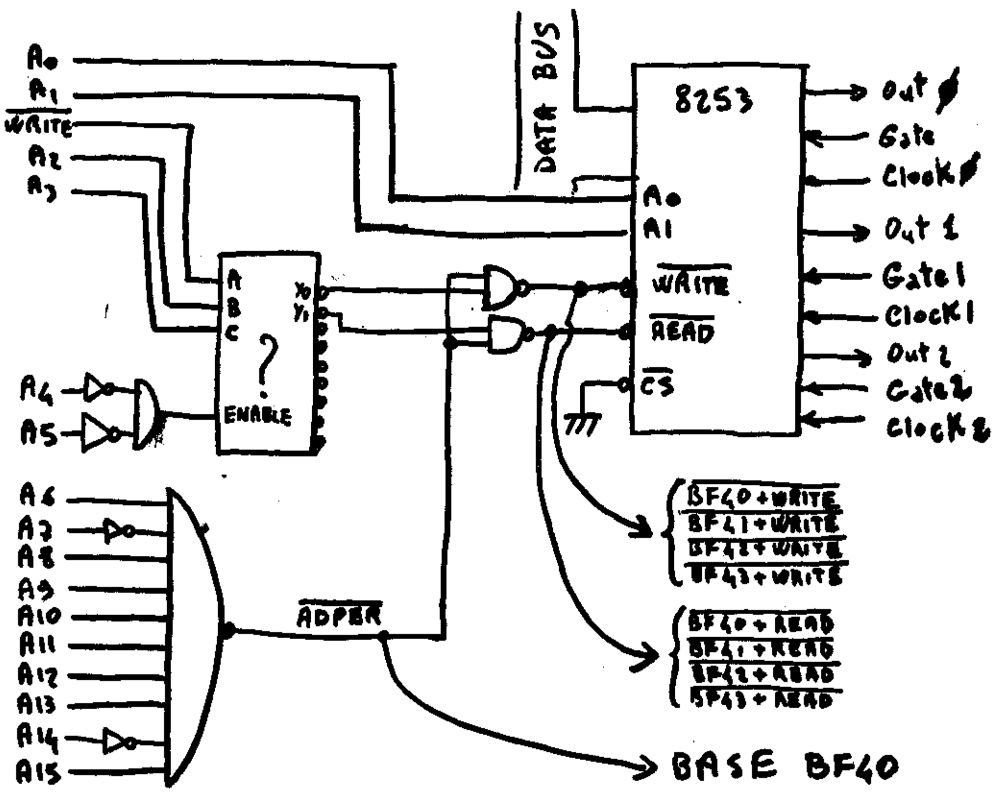
MODE 1: Programmable One-Shot. The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

```
INIT LDAA #CWTIMØ   ;INITIALISE MODE
     STAA TIMW      ;and latch Timer Ø
     LDAA #CWTIM1   ;INITIALISE MODE
     STAA TIMW      ;and latch Timer 1
     LDAA #CWTIM2   ;INITIALISE MODE
     STAA TIMW      ;and latch Timer 2
```

Connecting the programmable Timer 8253



6800 interface to logidule modules using the M))BUS signals

IF The gates of the timers are not used, use a pull-up resistor or an output of an inverter.

Exercise Nº 9.1

GOAL:

- To gain experience with the microprocessor programmable peripheral INTEL 8253

Use of the Keyboard on the microprocessor Kit as a musical instrument Keyboard.

Problem description:

Write a program to perform the following tasks:

1) Assign a frequency to each Key (from "0" to "F" only) of the microprocessor Kit.
2) Enter music pressing the Keys, echo each note entered on the speaker, memorise the note into the memory.
3) Exit the enter music mode if the "GO" Key is pressed and start executing what has been recorded in memory.

Insert a delay of 400 msec. between notes.

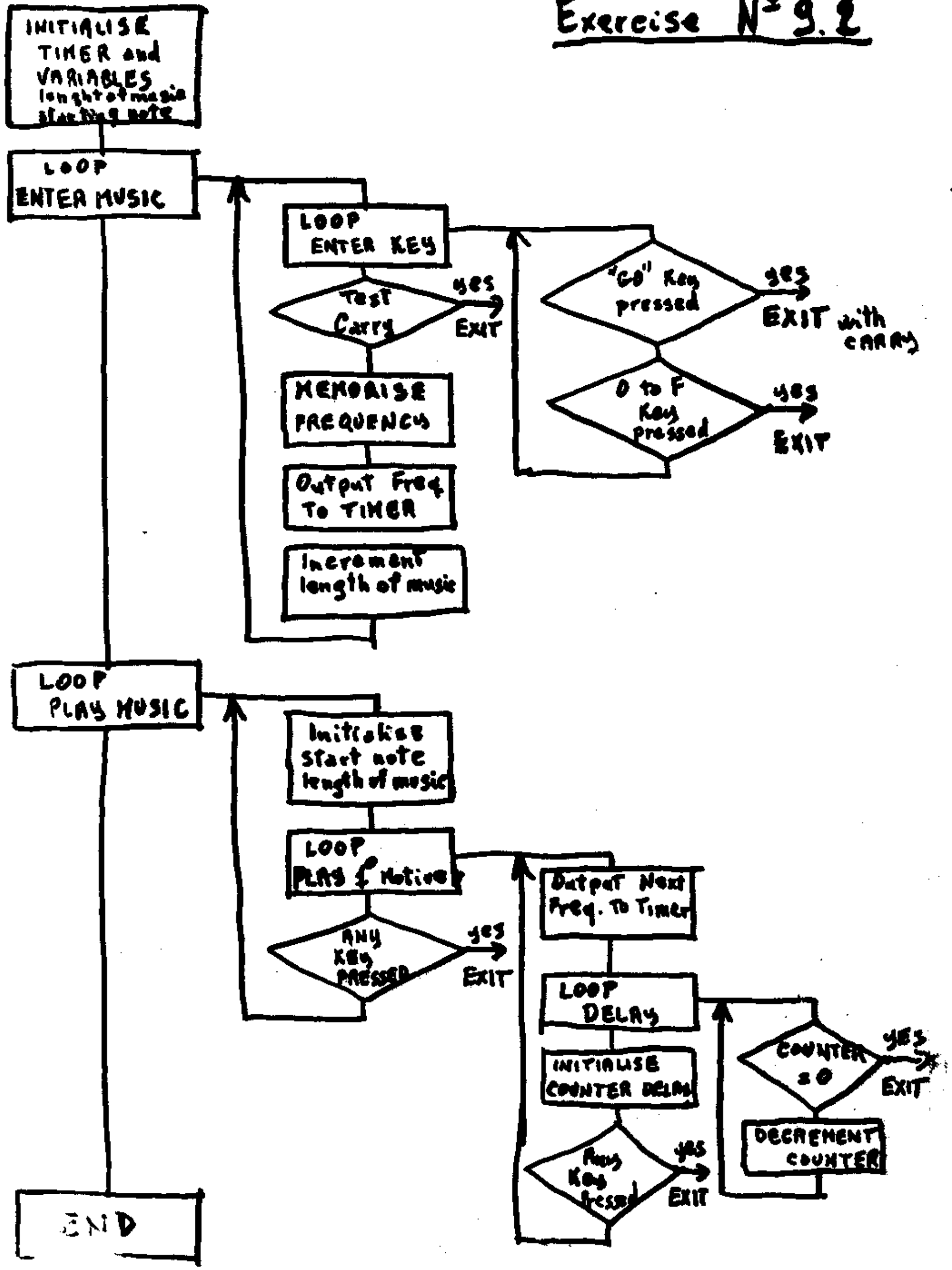
USE THE FOLLOWING TABLE FOR THE NOTES:

THE BASE FREQUENCY IS: 300'000 Hz

LA = 440 Hz
: 12 TONE
LA = 880 Hz
: 12 TONE
LA = 1760 H

NOTE	Frequency	Counter Divide by
DO		
DO#	.	
RE	.	
RE#	.	
MI	.	
FA#	.	
SOL		763
SOL#	440-(1/12 440)	
LA	440 Hz	681
LA#	440+(1/12 440Hz)	
SI	.	607
DO	.	
RE	.	
RE#	.	
MI	.	
FA	.	
F#	.	

Exercise N° 9.1



Exercise N° 9.2

GOAL:

To gain experience with microprocessor programmable peripheral INTEL 8253
- Hardware interrupts
- look-up table

Problem description:

- Write a program to play a single tone music
- Use one counter as square wave rate generator mode
- Use another counter in interrupt on terminal count mode
- Connect the output of the timer working on interrupt on terminal count mode to the $\overline{IRQ}$ line on the $\overline{MUBUS}$
- Load the starting address of the interrupt routine in the interrupt vector:

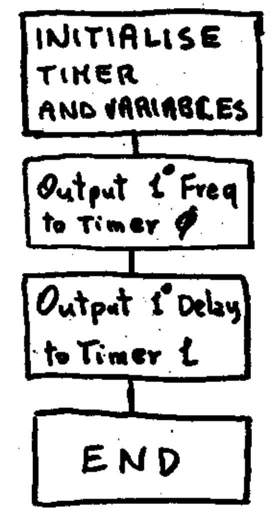
using the Kit monitor	E43C	05 HByte
	E43D	00 LByte
using the Rosy monitor	E000	05 HByte
	E001	00 LByte

i.e. 0500 = Starting address of your interrupt program

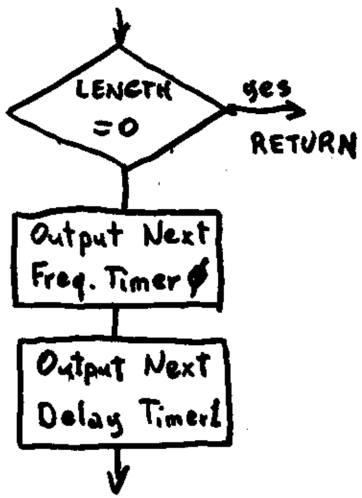
Since the program works on interrupt, most of the microprocessor time is available for other calculations.

Exercise N° 9.2

Main program



interrupt routine



Exercise 9.3

Goal:

- To gain experience with the microprocessor programmable peripheral Intel 8253
- look-up table
- assembler and linker

Problem description:

Write a program to play three tone music.

Make use of a macro for entering the text of the music.

The text of the music can be written in this form:

```
       FCB   PIANO
NOTE   DO3,MI4,SOL5,T8,DO3,MI4,NO,T1
```

i.e. DO3 = BASS, MI4 = VIOLA, SOL5 = 1° violino, T8 = Delay, DO3 = BASS, MI4 = VIOLA, NO = 1° violino, T1 = Delay

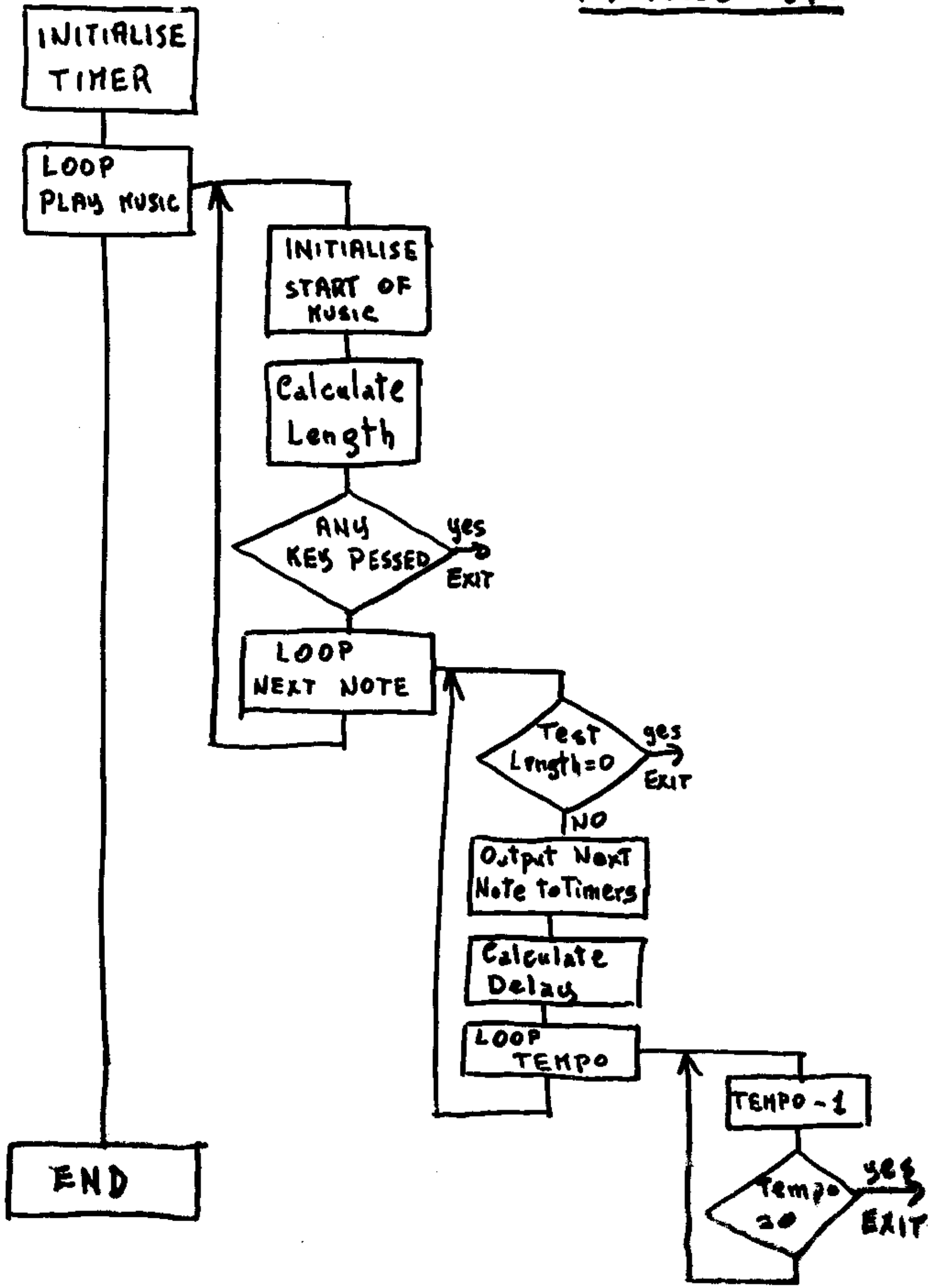
```
NOTE   MACR
       FDB  \0,\1,\2
       FCB  \3
       FDB  \4,\5,\6
       FCB  \7
       ENDM
```

You may insert in your program a table of equates for generating tuned notes on a programmable Timer which has a frequency = 300.000Hz as clock input   GET, NOTE/UN=MPCROSE

```
         DO3   EQU  $2301      (3 = OCTAVE)
DO Sharp DOS3  EQU  $2168
         RE3   EQU  $2042
         RES3  EQU  $1930
```

T64 = semibreve
T32 = minima
T8 = croma
NO = SILENT
ENT = END of Text

Exercise 9.1



~~DO = 1,0000 = 0 c~~

RE = 1,12246 = 200 c

$\sqrt[12]{2} = 1,059463 = 100c$

QUADRO GENERALE DELLE SCALE MUSICALI ANTICHE E MODERNE

[illegible]