INTERNATIONAL ATOMIC ENERGY AGENCY
UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION

INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS
34100 TRIESTE (ITALY) - P.O.B. 586 - MIRAMARE - STRADA COSTIERA 11 - TELEPHONES: 224281/2/3/4/5/6
CABLE: CENTRATOM - TELEX 460392-I

SMR/90 - 43

COLLEGE ON MICROPROCESSORS:

TECHNOLOGY AND APPLICATIONS IN PHYSICS

7 September - 2 October 1981

STANDARD BUSES

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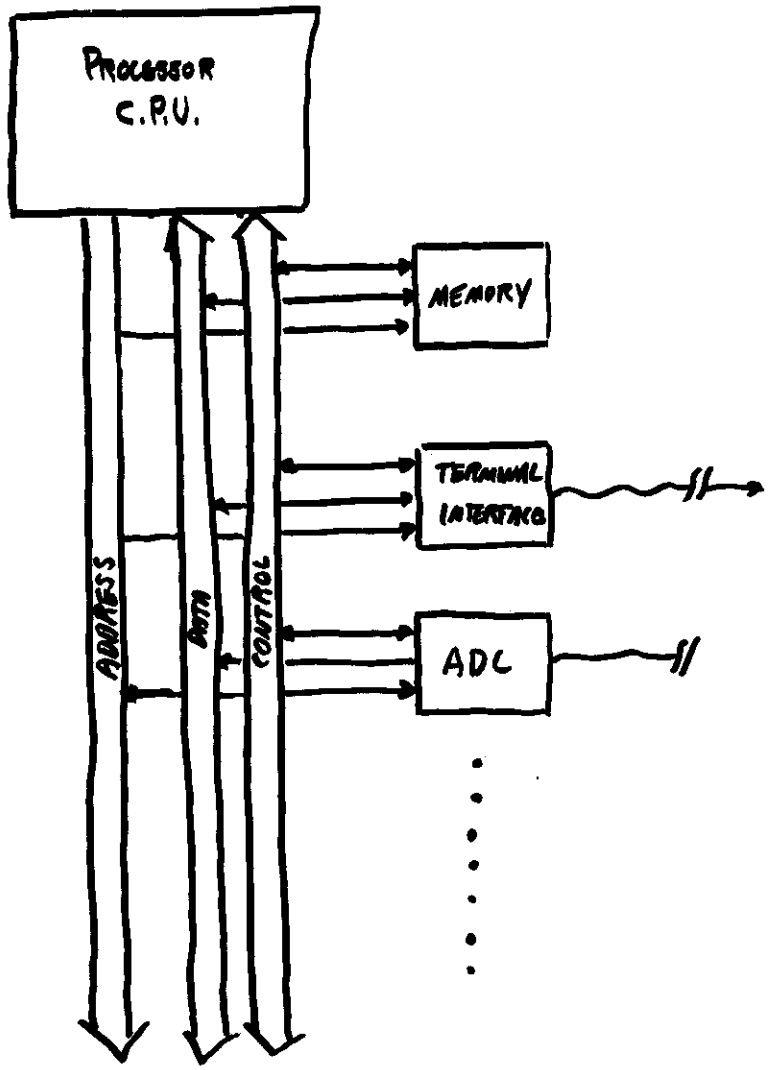
A MICRO-PROCESSOR SYSTEM

- PROCESSOR(S)
- MEMORY
  - RAM
  - PROM
- INPUT/OUTPUT DEVICES

COMPUTER-LIKE
- TERMINAL
- DISK
- PRINTER
- READER
- ⋮

LABORATORY-LIKE
- ADC
- DAC
- DIGITAL INPUT REG.
- DIGITAL OUTPUT REG.
- ⋮

PROCESSORS WORK ON BUSES



IF

- APPLICATION IS SMALL
- AND ALL COMPONENTS ON ONE BOARD

THEN

- NO PROBLEM, USE IT, FORGET ABOUT EXTERNAL BUSES AND...

  ... GO TO LUNCH BEFORE THE LINE

BUT

IF

APPLICATION IS LARGER, SO NEED MANY BOARDS

THEN

MAYBE STANDARD BUS IS GOOD

STAY AND LISTEN

HISTORY OF STANDARD BUSES

EARLY 1970's 1ST TRULY STANDARDS EMERGED

- UNIBUS FOR PROCESSOR PDP-11 FAMILY
- HP-IB FOR DESK TOP LABORATORY
- CAMAC FOR LARGE SCALE EXPERIMENTS & CONTROL

(LATER) • (S-100) FOR MICRO'S

EACH OPTIMIZED FOR APPLICATION

BUS BECOMES STANDARD BY...

... COMMITTEE

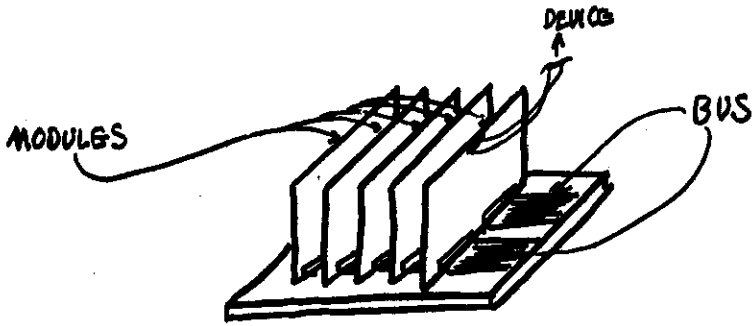
... DEFAULT

1 VENDOR VERY STRONG

1 MARKET VERY STRONG

BUSES: 2 FORMS OF MECHANICAL STRUCTURE

① BACKPLANE



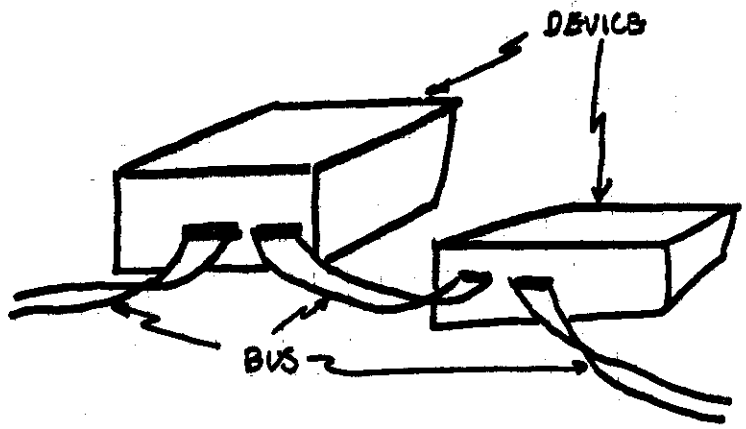
PLUG-IN MODULES TO BUS BACKPLANE

+ MODULARITY OF FUNCTION
+ CONVENIENCE OF DESIGN

- STILL NEEDS CABLES TO PHYSICAL DEVICE
- LIMITED LENGTH

BUSES: 2 FORMS OF MECHANICAL STRUCTURE

① CABLE



PLUG-IN CABLE TO PHYSICAL DEVICES

+ BUS ACCESS TO LARGE FUNCTIONAL UNITS
+ MORE SPACE FOR SPECIAL UNITS

- CABLES GET MESSY
- LENGTH INTRODUCES BUS PROBLEMS

BUSES: 2 MAIN USES

USE EMPHASIZES CERTAIN CHARACTERISTICS...

① PROCESSOR BUS

- ADDRESS SPACE
- DATA PATH
- INTERRUPT
- ARBITRATION

} ALL OPTIMIZED FOR PERFORMANCE

② LABORATORY BUS

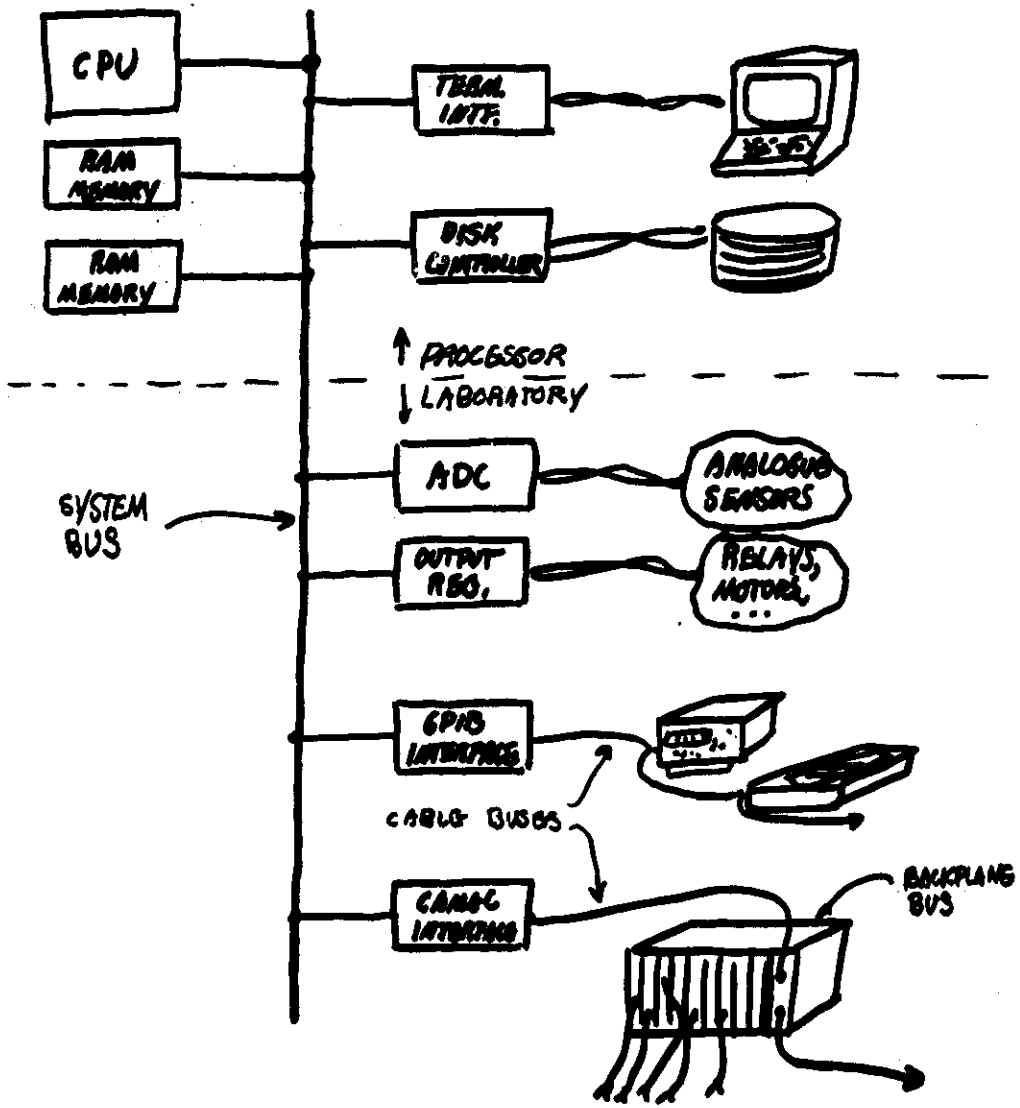
- MECHANICS
- CABLE

} OPTIMIZED FOR CONVENCE

AVAILABLE STANDARD BUSES

	PROCESSOR	LABORATORY
BACKPLANE	UNIBUS Q-BUS S-100 (IEEE 696) MULTIBUS (IEEE 796) VERSABUS STD BUS EUROBUS MUBUS ⋮	CAMAC (IEEE 583) FASTBUS
CABLE	UNIBUS	GP-IB (IEEE 488) CAMAC (IEEE 596, 595) FASTBUS

SYSTEM STRUCTURE WITH BUSES



COULD BE CAVIAR

FUNDAMENTAL ASPECTS OF STANDARD [redacted] BUSES

- DATA TRANSFER
  - DEVICE SELECTION
  - DATA PATH
  - SYNCHRONIZATION
- INTERRUPTS
  - PRIORITY
  - DEVICE SELECTION
- BUS MASTERSHIP
  - PRIORITY
  - BUS EXCHANGE
- MECHANICS
- POWER

MASTER – SLAVE RELATIONSHIP

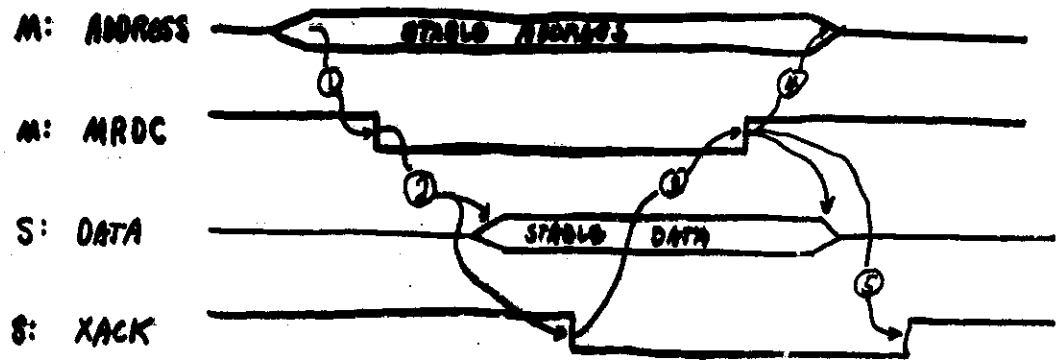
MASTER

- CONTROLS BUS OPERATION
  - GENERATES ADDRESS
  - GENERATES SYNCHRONIZATION SIGNAL
  - GENERATE DATA IF WRITE
- USUALLY CPU
- MAYBE INTELLIGENT DEVICE

SLAVE

- RESPONDES TO BUS OPERATION
  - RECOGNIZES ADDRESS
  - GENERATES ACKNOWLEDGE
  - GENERATES DATA IF READ
- USUALLY MEMORY
- MAYBE DEVICE

EXAMPLE MULTIBUS READ OPERATION



① ADDRESS STABLE 50 ns MIN THEN MRDC ↓

② SLAVE RESPONDS NO MIN. BUT XACK NO SOONER THAN DATA

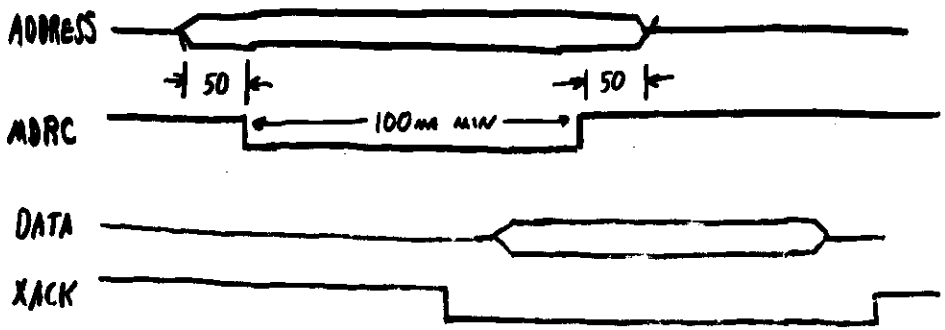
③ MASTER REMOVES MRDC NO MIN.

④ MASTER REMOVES ADDR 50 ns MIN. LATER

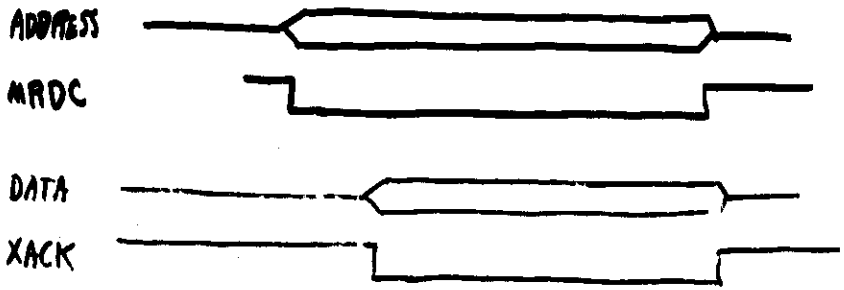
⑤ SLAVE REMOVES DATA & XACK 65 ns MAX LATER

MULTIBUS READ SEEN FROM BOTH ENDS

SEEN AT MASTER:



SEEN AT SLAVE:



ASYNCHRONOUS - HAND SHAKE BUSES

+/A

- MOST STANDARD BUSES
- ALLOWS DIFFERENT SPEED DEVICES
- ON CABLE ALLOWS VARIABLE LENGTH
- VERIFIES ADDRESS EXISTS

-

- SLOWER
- - TIME WASTED TO GET OFF BUS
  - TIME WASTED DURING ACCESS
- HANG-UP IF NO ACKNOWLEDGE

VARIATIONS on BASIC READ/WRITE OPERATION

MULTIBUS — Good for 8080, 8086 style micro

MRDC	Memory Read & Strobe
MWTC	Memory Write & Strobe
IORC	I/O Read & Strobe
IOWC	I/O Write & Strobe

UNIBUS — Good for 6800, LSI-11 style micro

C1	=0 Read
	=1 Write
MSYNC	Strobe

Addresses $000\,000_8 - 757777_8$ Memory

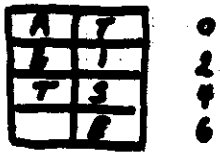
$760\,000_8 - 777\,777_8$ I/O

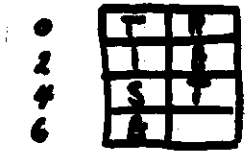
WORD/BYTE ADDRESSING

2 Styles of Processors

8080/Z80	6800/6502
PDP-11/8086	Z8000/68000

Least Significant Byte @ A (even)	Most Significant Byte @ A (even)
Most Sign Byte @ A+1 (odd)	Least Significant Byte @ A+1 (odd)

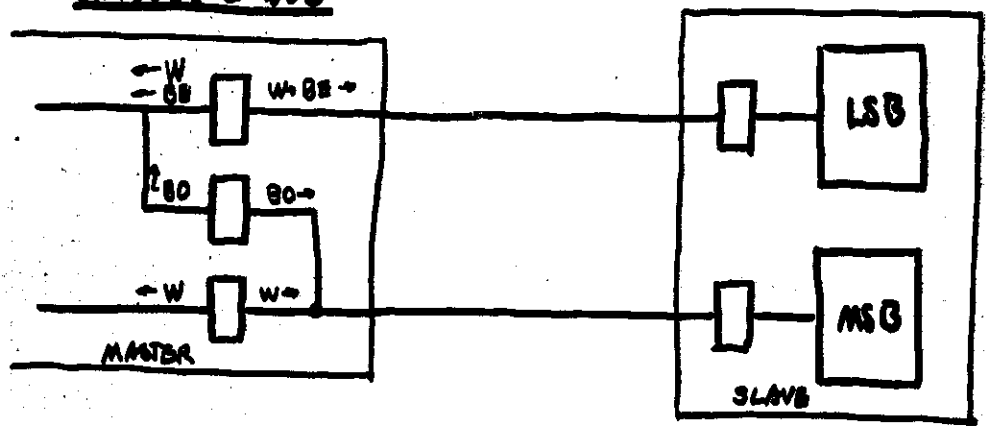




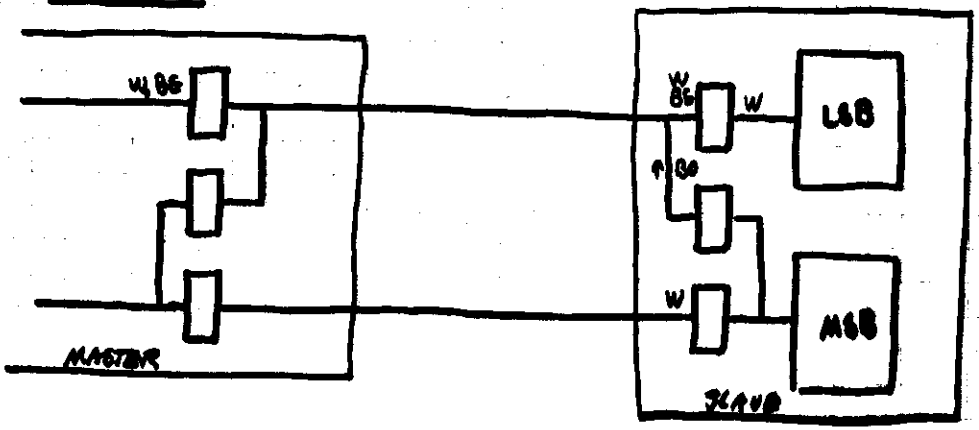
WORD/BYTE ADDRESSING

2 STYLES OF BUSSING

UNIBUS, Q-BUS



MULTIBUS



SO TRANSITION 8 BITS to 16 BITS COULD BE HARD

BUS MASTERSHIP

IF (1 CPU) THEN NO PROBLEM

MASTER ASSERTS

- ADDRESS LINES
- MOST CONTROL & TIMING
- DATA LINES FOR WRITE COMMANDS

SLAVE DEVICES

- ACKNOWLEDGE LINE(S)
- DATA LINES FOR READ COMMANDS

OTHER MASTERS

- DMA [DIRECT MEMORY ACCESS] DEVICE
  - DISK
  - PRINTER
  - USER DATA INTERFACE
- 2ND CPU
- INTERRUPTS (SOME BUSES)

WHAT'S NEEDED FOR BUS MASTERSHIP RESOLUTION

SOMETIMES CALLED
- BUS EXCHANGE
- BUS ARBITRATION
- PRIORITY RESOLUTION
- ⋮

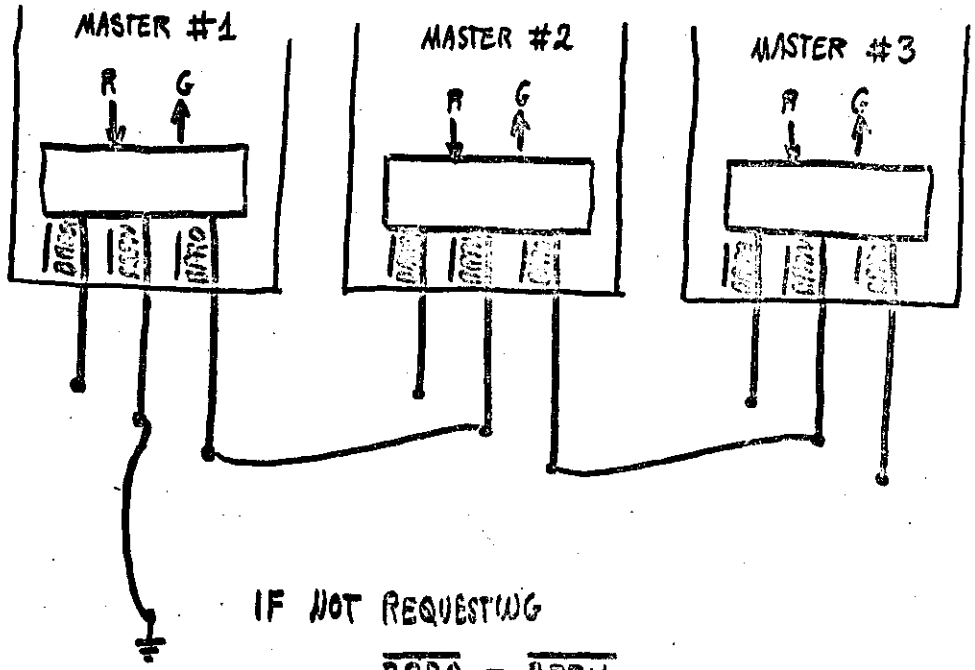
1) SET PRIORITY - USER DEFINED
   - SERIAL SCHEMES
   - PARALLEL SCHEMES

2) SYNCHRONIZE TRANSFER

SERIAL PRIORITY SCHEMES

UNIBUS, Q-BUS, MULTIBUS, CAMAC

MULTIBUS EXAMPLE



IF NOT REQUESTING

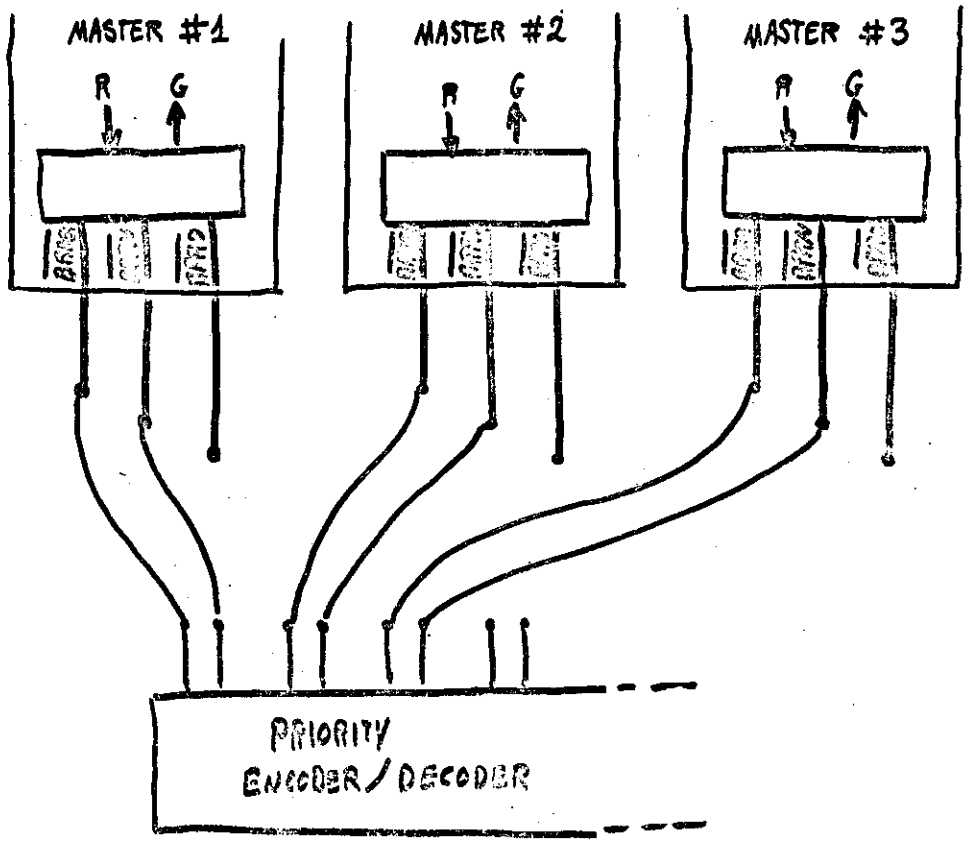
$\overline{BPRO} = \overline{BPRN}$

IF REQUESTING

$\overline{BPRO} = H$

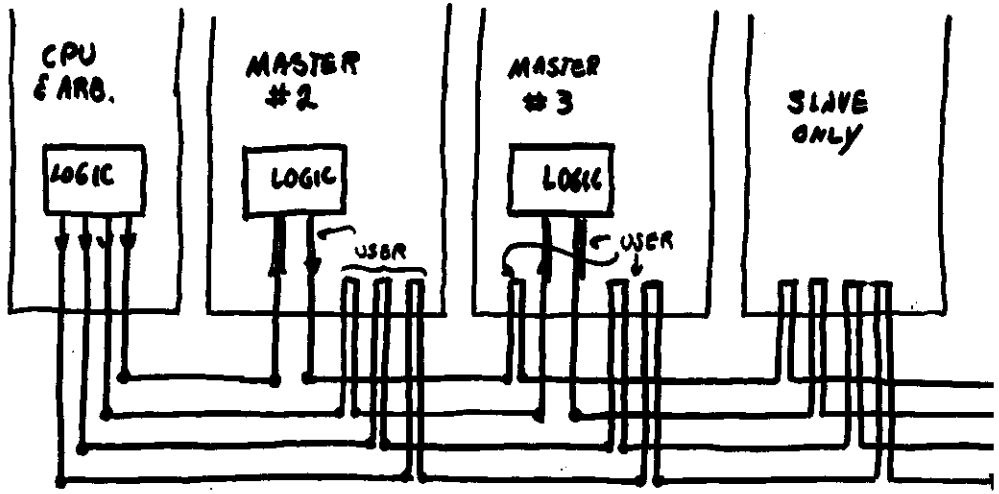
PARALLEL PRIORITY SCHEME

MULTIBUS EXAMPLE



SERIAL BUS PRIORITY SCHEME

UNIBUS EXAMPLE: GRANT LOOK ONLY



UNIBOS

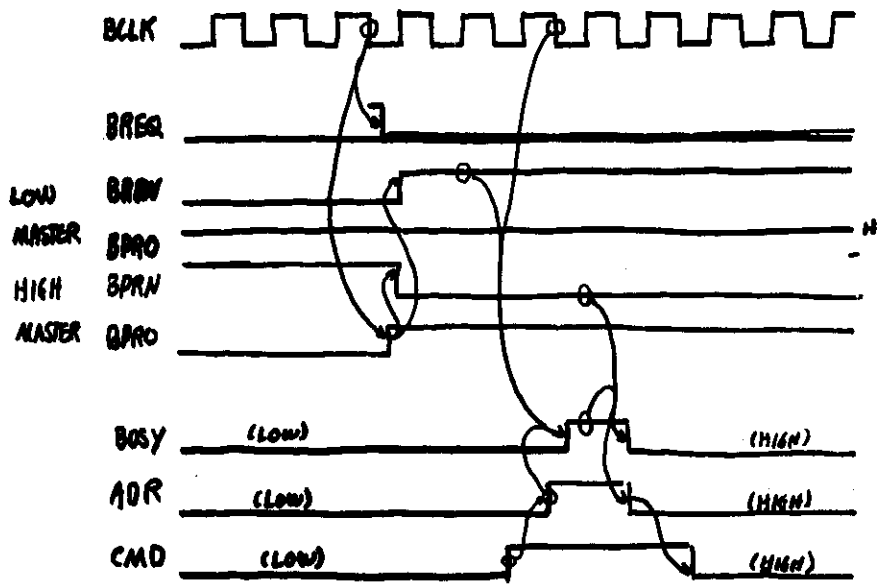
REQUEST-GRANT PAIRS

NPR / NPG	NON INTERRUPT
BR7 / BG7	} FOR INTERRUPTS
BR6 / BG6	
BR5 / BG5	
BR4 / BG4	

SERIAL BUS PRIORITY SCHEMES

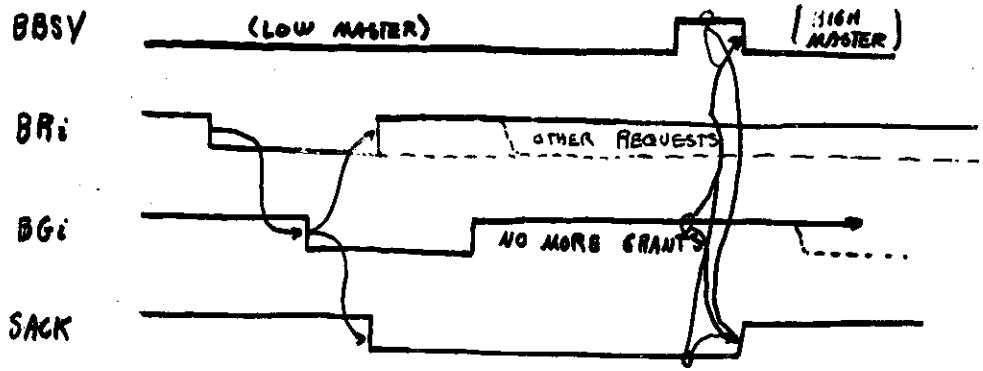
- ALLOWS (IN PRINCIPAL) ANY NUMBER OF MASTERS
  - ↙ SOMETHING ELSE MAY LIMIT
- TIME: GRANT SIGNAL MUST BE PASSED
- UNIBUS
  - STRICTLY POSITION DEPENDANT ON EACH LINE
  - MULTIPLE GRANT LINES
  - HAND WIRE ON MODULES
- MULTIBUS
  - BACKPLANE WIRED DEPENDANT
  - ALLOWS PARALLEL SCHEME

BUS EXCHANGE TIMING : MULTIBUS



[redacted]
SYNCHRONOUS TO BCLK

BUS EXCHANGE TIMING : UNIBUS



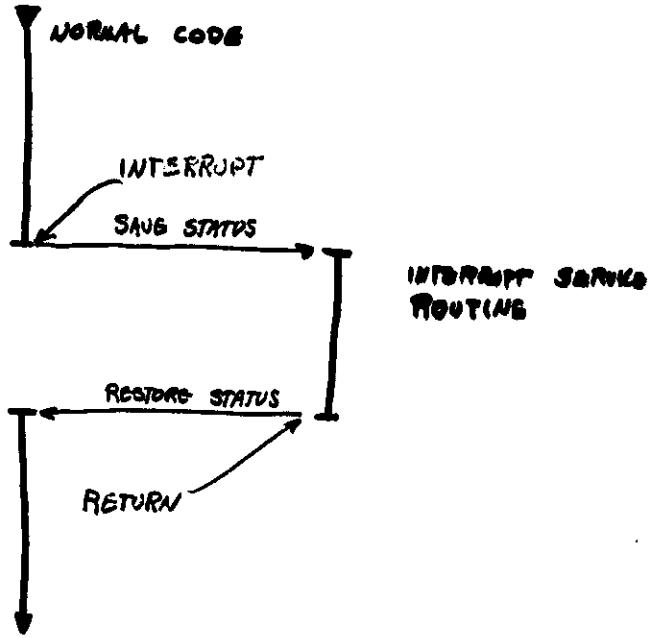
COMPLETE ASYNCHRONOUS

INTERRUPTS

FUNDAMENTAL IMPORTANCE TO SMOOTH SYSTEM

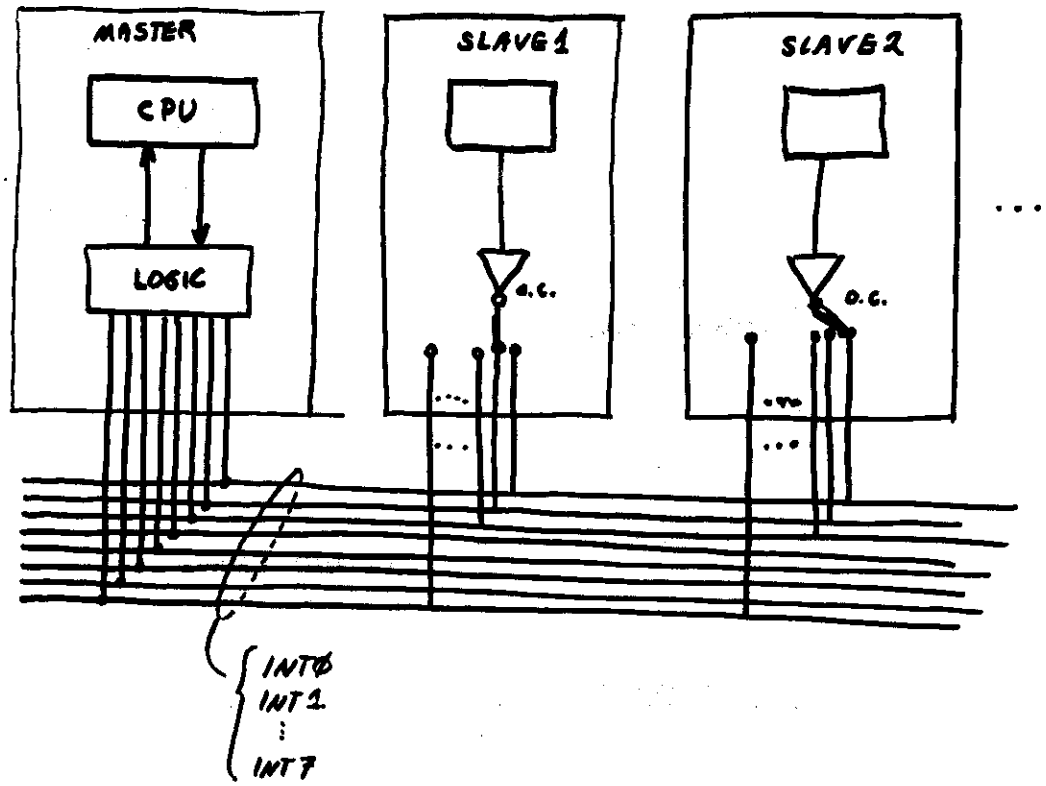
GREAT DEAL OF VARIATION

- PROCESSOR TO PROCESSOR
- BUS TO BUS



NON BUS VECTORED INTERRUPTS

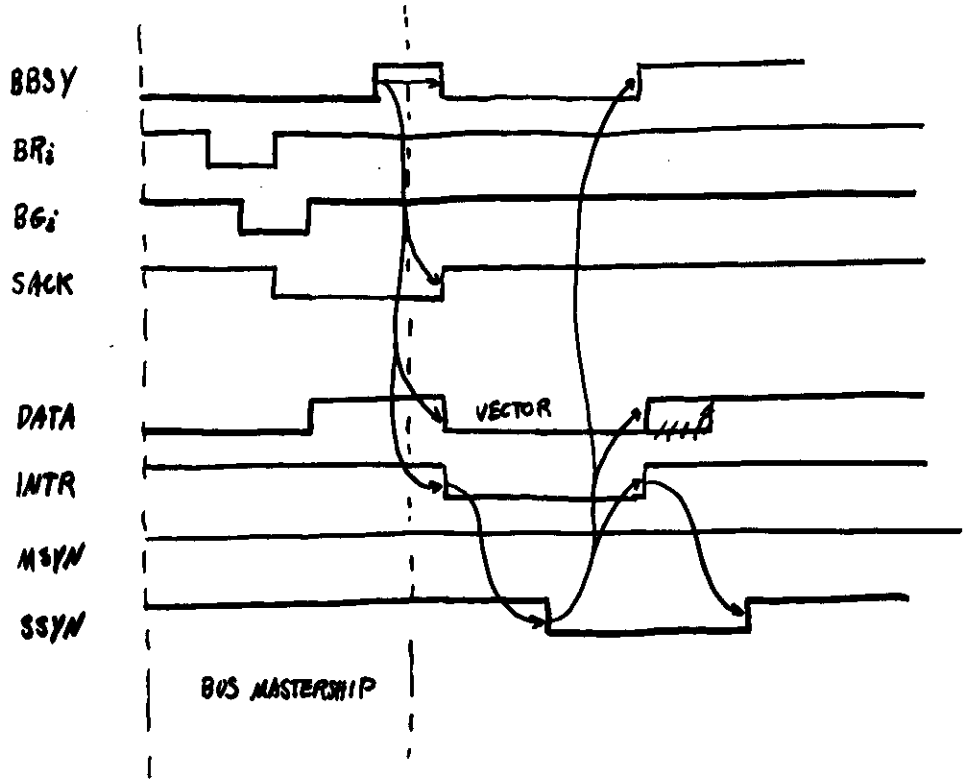
EXAMPLE : MULTIBUS



NON BUS-VECTORED INTERRUPTS MULTIBUS EXAMPLE

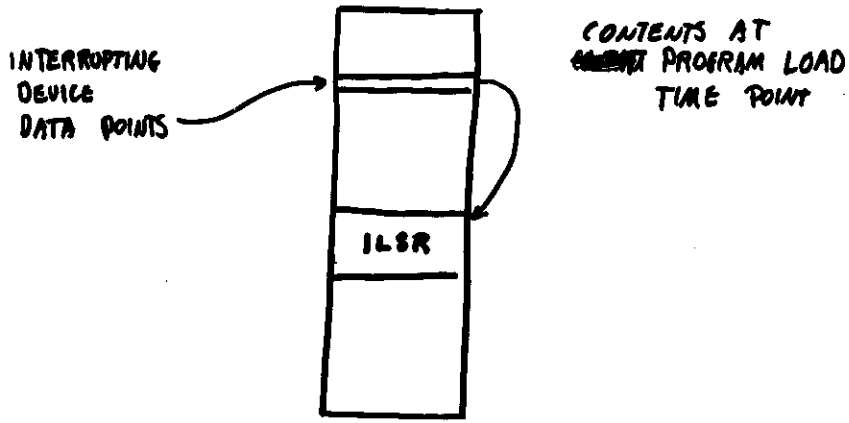
- ALLOW 8 INTERRUPT SOURCES
  - PLUS THOSE INTERNAL TO CPU BOARD
- ONLY 1 LEVEL/PRIORITY PER SOURCE
- EASY TO CONFIGURE
  i.e. 1 JUMPER PER SOURCE
- INTERRUPT SERVICE ROUTINE ADDRESS KNOWN TO MASTER
  COORDINATE JUMPER WITH LOGIC IN MASTER

BUS VECTORED INTERRUPT : UNIBUS TIMING



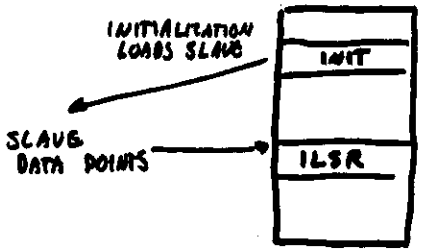
BUS VECTORED INTERRUPTS : UNIBUS DATA

- INTERRUPTING DEVICE IS BUS MASTER
- SPECIAL WRITE COMMAND TO CPU
  - ONLY 1 CPU ALLOWED
  - DATA LINES CONTAIN VECTOR ADDRESS
- SETUP
  - HAND WIRE ADRESS OF VECTOR ADDRESS
  - LOAD VECTOR ADDRESS WITH PROGRAM



BOS VECTORED INTERRUPTS : MULTIBUS

- INTERRUPTING DEVICE IS SLAVE
- SPECIAL COMMAND SEQUENCE TO SLAVE
- SLAVE RETURNS VECTOR ADDRESS
- SETUP
  - HARDWIRE SLAVE TO INTi LINE
  - CPU INIT RETURN TO LOAD SLAVE



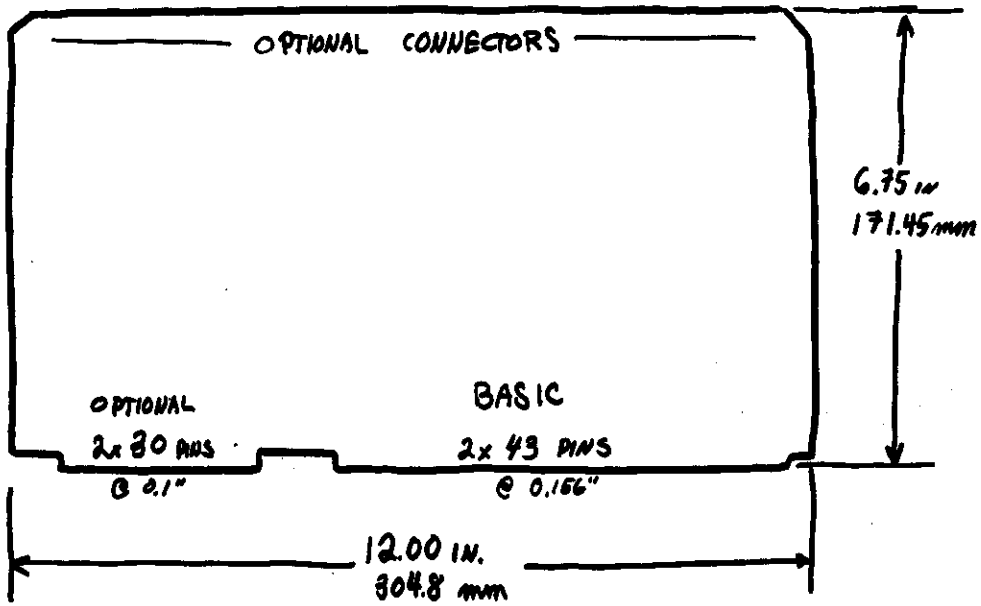
⇒ 8 INTERRUPT SOURCES

EACH WITH MULTIPLE POSSIBLE INTERRUPTS

⇒ MULTIPLE MASTER DO-ABLE

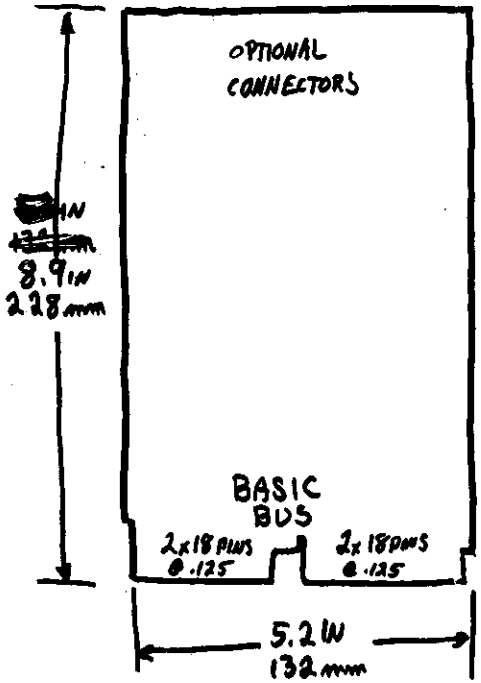
MULTIBUS CARD SIZE

1/2 ACTUAL SIZE



Q-BUS, UNIBUS CARDS

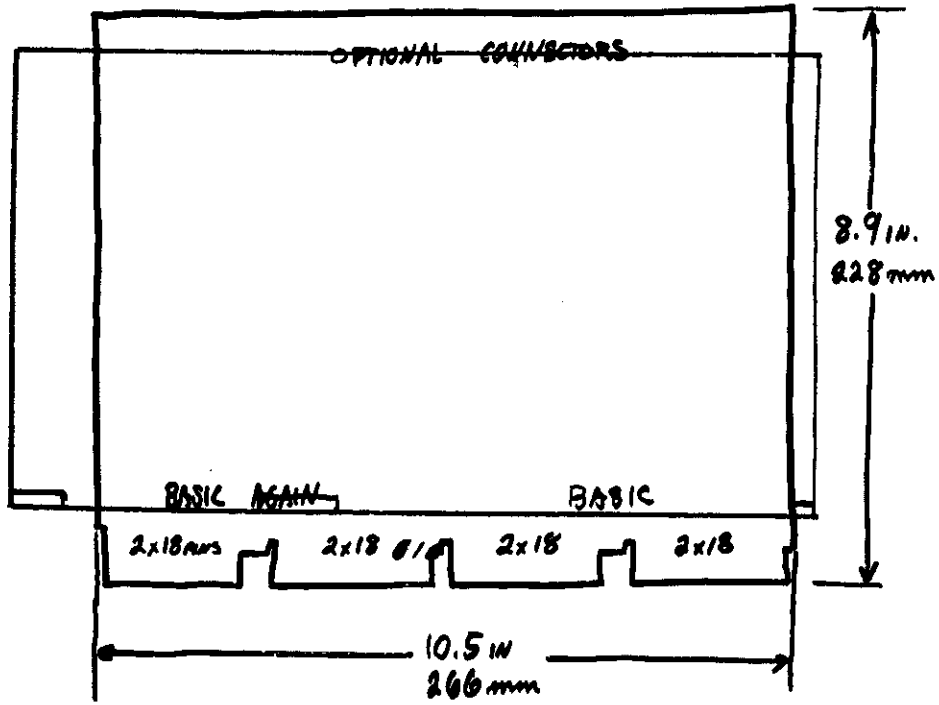
½ ACTUAL SIZE



Q-BUS, UNIBUS CARDS

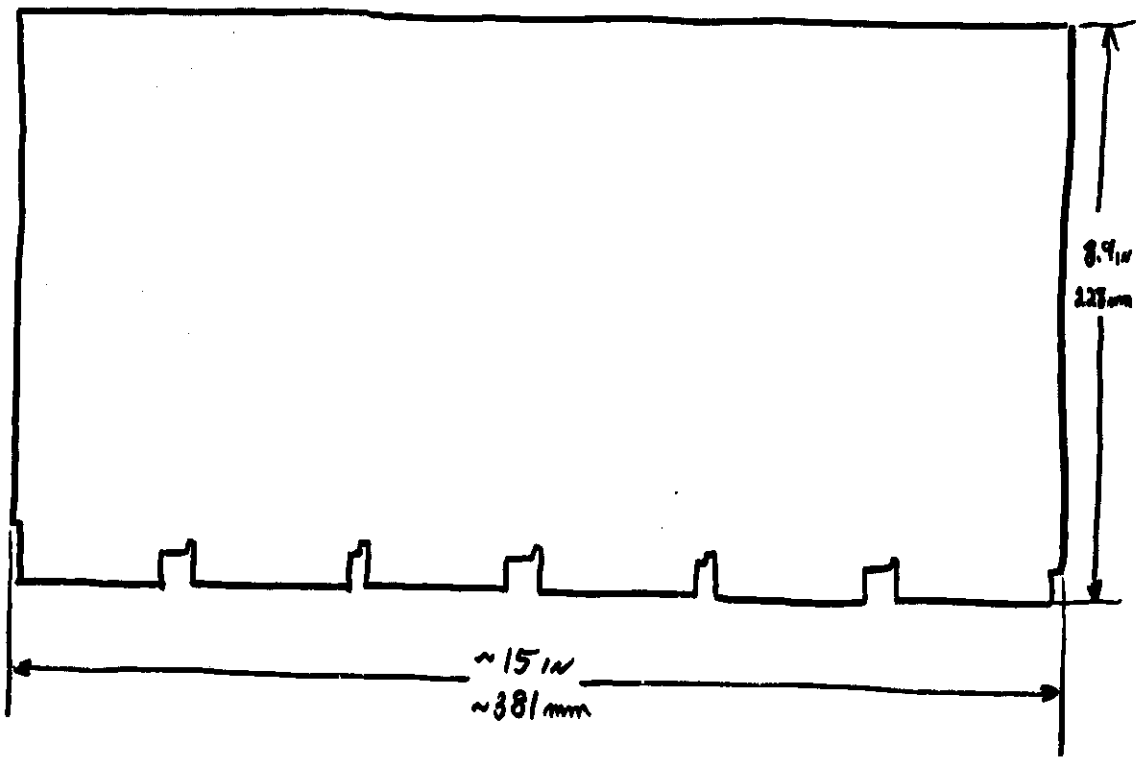
½ ACTUAL SIZE

QUAD BOARD



UNIBUS CARDS

'HEX' BOARD



STANDARD BUS MECHANICS

- ALL HAVE BACKPLANES COMMERICALLY AVAILABLE
  - MULTIPLE SOURCES
- SOME HAVE OPTIONAL CONNECTORS EXPOSED
- SOME HAVE CAGE INSIDE BOX
- SOME USE PIN AND SOCKET
  AVOID TOO MUCH GOLD

STANDARD BUSES POWER

	MULTIBUS	Q-BUS
MAIN		
+5	✓	✓
-5	✓	
+12	✓	✓
-12	✓	✓
BATTERY		
+5	✓	✓
-5	✓	
+12	✓	✓
-12	✓	
ANALOGUE		
+15	✓	
-15	✓	
SPARES		
USER DEF	✓	✓
POWER FAIL LOGIC	✓ (OPTIONAL)	✓ (STD)

OVERVIEW OF STANDARD PROCESSOR BUSES

NAME	ORIGIN	MAIN CPU	COMMENTS
UNIBUS	DEC	PDP-11	BACKPLANE, CABLE
Q-BUS	DEC	LSI-11	
MULTIBUS	INTEL	8080/8086	IEEE 796
S-100 BUS	HOBBIST	8080, Z80	IEEE 696
STD BUS	PRO LOG	8080, Z80	
VERSABUS	MOTOROLA	6800, 68000	
⋮	⋮	⋮	⋮

A Laboratory Cable Bus : IEEE-488

OFFICIAL STANDARD:

IEEE-488-1978 } IDENTICAL
ANSI MC1.1
IEC 625-1

NAMES:

HP-IB
GPIB
IEEE BUS
ASCII BUS
PLUS BUS
IEC BUS

IEEE 488 BUS

PURPOSE : CONNECT LABORATORY INSTRUMENTS TOGETHER
TO AUTOMATE EXPERIMENTS & TESTS

THEREFORE

- CABLE OF SOME LENGTH
- MANY SPECIAL FEATURES
- MINIMUM NUMBER OF LINES IN CABLE

↑ THEORY: LINE IN BUS MORE EXPENSIVE THAN LOGIC CIRCUIT.

SUCCESS

- 170 MANUFACTURERS
- 14 COUNTRIES
- > 1000 PRODUCTS

[illegible] NEW WORDS

Processor Bus

- MASTER /SLAVE
- READ /WRITE WRT MASTER

IEEE 488 BUS

① • LISTENER

- RECEIVES DATA
- EXAMPLES: PRINTERS
  DISPLAYS
  POWER SUPPLIES
  SIGNAL SOURCES
- UP TO 14 ACTIVE AT 1 TIME

IEEE 488 BUS

② TALKER

- TRANSMITS DATA onto BUS
- EXAMPLES: VOLTMETER
  COUNTERS
- ONLY 1 ACTIVE AT A TIME

THUS ONE CAN SAY 'ONLY WRITES EXIST'

③ CONTROLLER

- SPECFIES TALKER & LISTENER
- EXAMPLE COMPUTER
  PROGRAMMABLE CALCULATOR
- ONLY 1 ACTIVE AT A TIME
- ONLY 1 MASTER CONTROLLER IN SYSTEM

THE 24 LINES OF THE IEEE 488 BUS

DATA LINES

8 LINES BIDIRECTIONAL DIO1 - DIO8

HANDSHAKE

DAV DATA VALID

NRFD NOT READY FOR DATA

NDAC NOT DATA ACCEPTED

MANAGEMENT

ATN ATTENTION

IFC INTERFACE CLEAR

SRQ SERVICE REQUEST

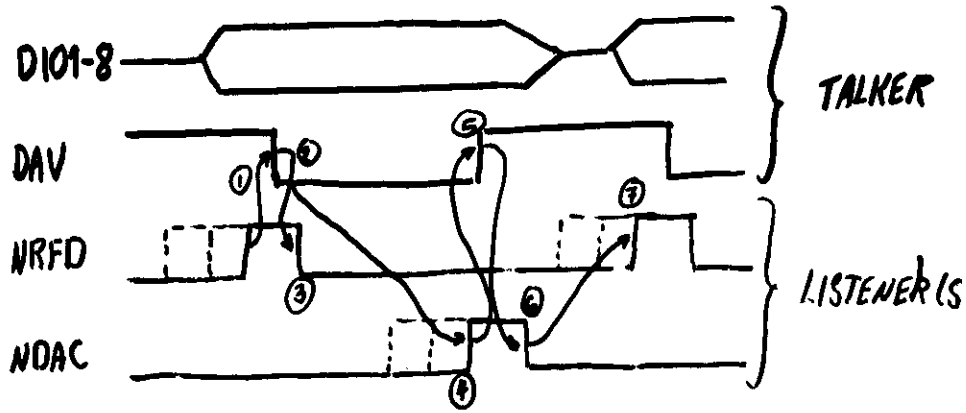
REN REMOTE ENABLE

EOI END OR IDENTIFY

GROUND

8 LINES

IEEE 488 3-LINE HANDSHAKE



SPECIAL HANDSHAKE ALLOWS MULTI-LISTENER

IEEE 488 WHAT HAPPENED TO ADDRESS ?

IF (ATN = 0) 8 BIT DATA IS TRANSMITTED

TALKER → LISTENER(S)

IF (ATN = 1) 7 BIT COMMAND TRANSMITTED

CONTROLLER → ALL DEVICES

ADDRESSING

CONTROLLER SETS ATN=1, THEN SENDS...

0 (UNL) UNLISTEN COMMAND

1 MLA LISTEN ADDRESS

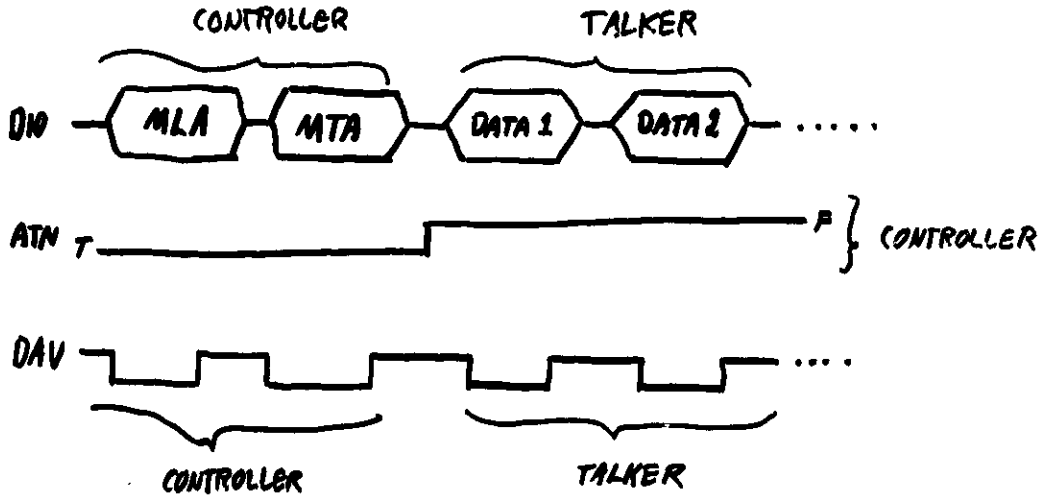
2 MTA TALKER ADDRESS

3 CONTROLLER SETS ATN=0, THEN TALKER SENDS...

DATA 1
DATA 2
DATA 3
⋮

DATA n

IEEE 488 ADDRESSING



TALKER REMAINS TALKER UNTIL

- ANOTHER TALKER ASSIGNED
- UNT UN-TALK SENT
- IFC CLEAR SENT

LISTENER REMAINS LISTENER UNTIL

- UNL UNLISTEN SENT
- IFC CLEAR SENT

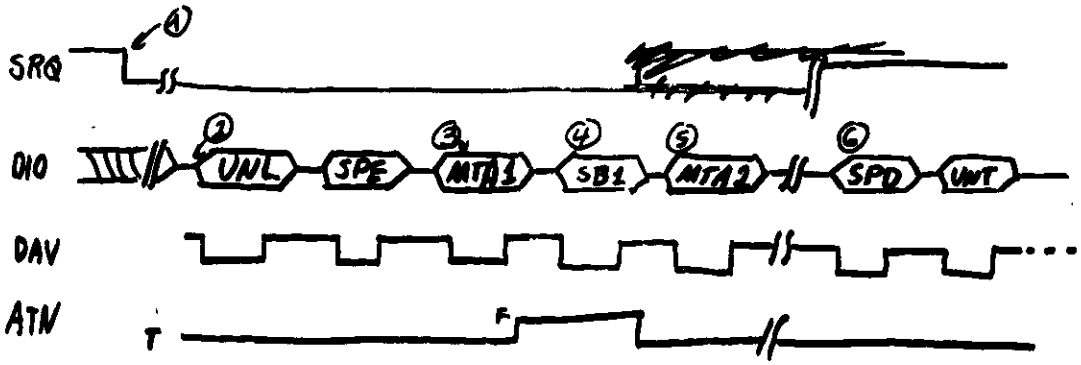
IEEE 488 "INTERRUPTS"

BETTER TO SAY 'SERVICE REQUEST'

1 OR-ED LINE: SRQ

'POLL' TO FIND SOURCE

SERIAL POLLING:



① SERVICE REQUEST SENT

② CONTROLLER RESPONDS: UNLISTEN TO ALL
SERIAL POLL ENABLE

③ CONTROLLER ADDRESS DEVICE

④ EACH DEVICE RESPONDS WITH STATUS BYTE

⑤ REPEAT ③ & ④ FOR EACH DEVICE

⑥ CONTROLLER ENDS WITH { SERIAL POLL DISABLE
UNTALK

IEEE-488 OTHER FEATURES

- REMOTE / LOCAL

  REMOTE: CONTROL OF DEVICE BY BUS

  LOCAL: CONTROL OF DEVICE BY FRONT PANEL
  I.E. HUMAN

- DEVICE CLEAR

  RESETS DEVICE (NOT BUS) TO SOME STATE

- TRIGGER

  ENABLES COMMAND START FROM BUS
  OF MULTIPLE DEVICES

IEEE 488 BUS ARBITRATION

WITH ATN = 0 — ONLY 1 TALKER HAS BUS
TALKER CHANGED BY CONTROLLER

WITH ATN = 1 — ONLY 1 CONTROLLER HAS BUS
CONTROLLER CHANGED BY PASSING
CONTROL WITH BUS COMMANDS.

AT ANY TIME — ONLY 1 MASTER (SYSTEM) CONTROLLER
CAN TAKE CONTROL BY IFC
'INTERFACE CLEAR'

IEEE 488 MECHANICS

- ONLY CABLE AND CONNECTOR
- 2 TYPES
  - IEEE/ANSI: 24 PIN RIBBON ← { METRIC BLACK / ENGLISH SILVER }
  - IEC 25 PIN RS 232 TYPE
- ONE DEVICE EVERY 2 METERS
  OR 20 METERS MAXIMUM
- CONFIGURATIONS

STAR

LINEAR

- SPECIAL CONNECTOR CABLE

CAMAC AND DISTRIBUTED INTELLIGENCE

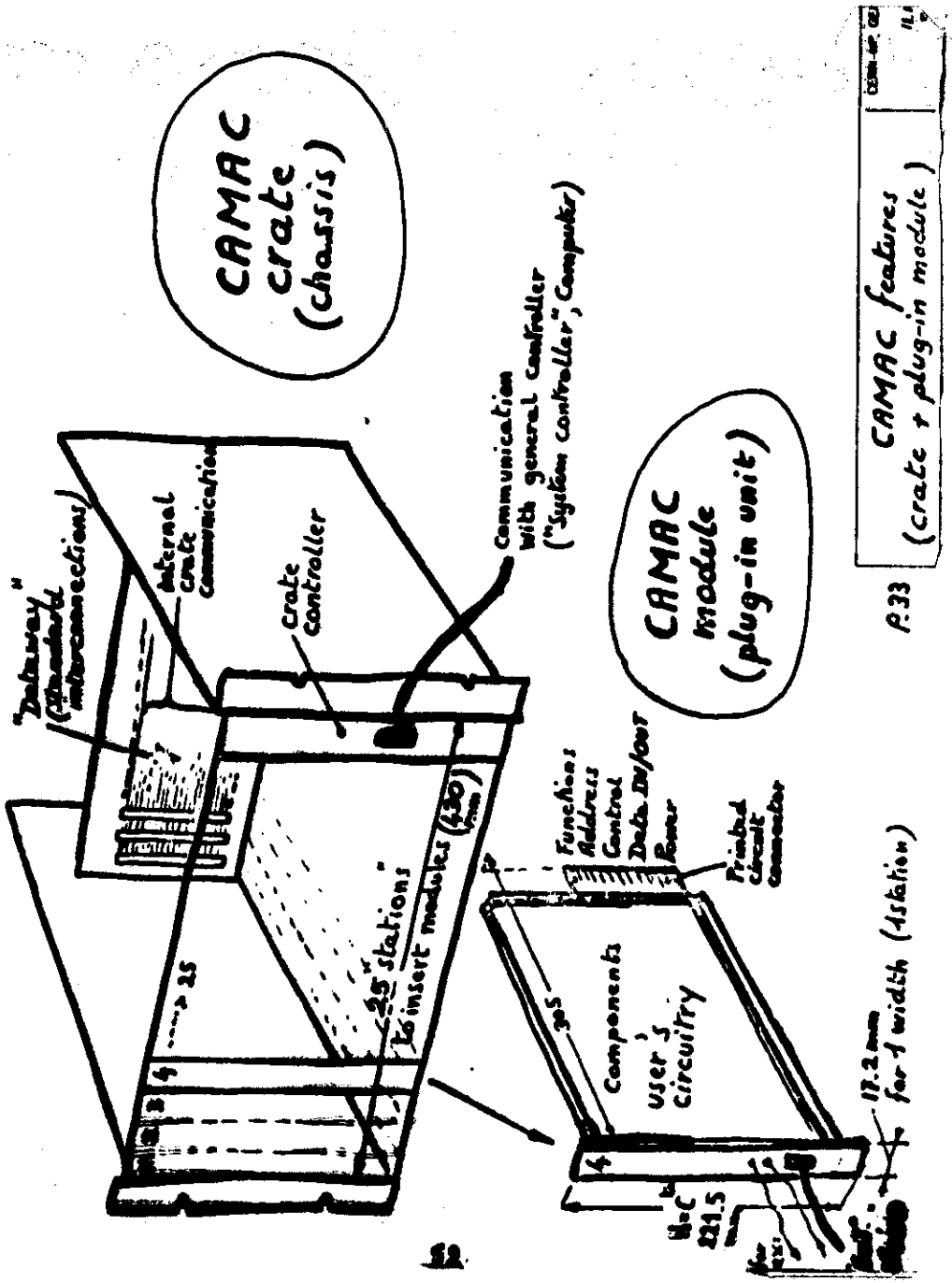
PART I: CAMAC a Review

HISTORY:

1964	NIM	COMMITTEE	PUBLISHES	NIM
1965	ESONE	COMMITTEE	PUBLISHES	?
1969	ESONE	"	PUBLISHES	CAMAC
1970	NIM	"	ACCEPTS	CAMAC

DOCUMENTS:

	ESONE	NIM	IEEE
CRATE + MODULES	EUR-4100	{TID-25875 TID 25877}	STD 583
BRANCH + CONTROLLER	EUR-4600	TID 25876	STD 596 (P)
SERIAL + CONTROLLER	?	TID-26488	STD 595 (P)
ANALOGUE SIGNALS	EUR-5100	TID 26614	NONE
SOFTWARE	IML/01	TID-26615	NONE



CAMAC DATAWAY ADDRESS

N STATION NUMBER 5 BITS — POSITION DEPENDANT

- N = 1 – 23 FOR MODULES
- N = 0
- N = 24 - 25 CRATE CONTROLLER

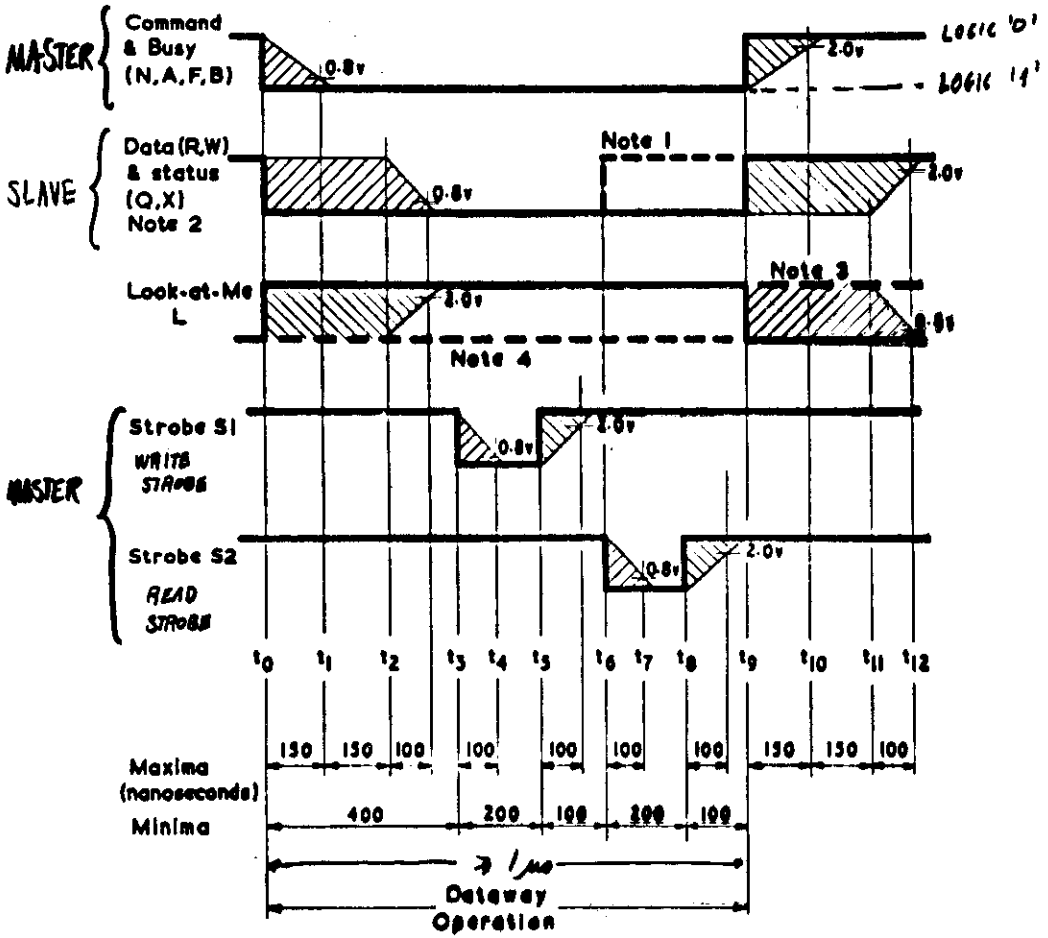
A SUBADDRESS 4 BITS

16 INTERNAL REGISTERS

USUALLY CORRESPONDING TO 16 DATA CHANNELS

CAMAC FUNCTIONS

- 5 F LINES 5 BITS ⇒ 32 FUNCTIONS
- READ(S)
  - BASIC READ F(0) — ALMOST ALL
  - READ & CLEAR F(2) — FREQUENT
  - READ ALTERNATE REGISTER F(1) } RARE
    (THIS CAN HAVE 32 REGISTERS)
  - READ COMPLEMENT F(3) }
- WRITE(S)
  - BASIC WRITE F(16) ↑ ALMOST ALL
  - WRITE ALTERNATE F(17)
  - SELECTIVE SET F(18), F(19)
  - SELECTIVE CLEAR F(20), F(22) ↓ RARE
- OTHERS
  - CLEAR F(9), F(11), F(10)
  - TEST STATUS F(8), F(27)
  - CONTROL F(24), F(25), F(26)
  - NON-STANDARD F(4), F(6), F(12), F(14), F(20), F(22), F(28), F(30)
  - RESERVED F(5), F(7), F(13), F(15), F(29), F(31)



Note 1: Data & status may change in response to S2.

Note 2: During some operations Q may change at any time.

Note 3: LAM status may be reset during operation.

Note 4: L signal may be maintained during operation.

FIG. 9. TIMING OF A DATAWAY COMMAND OPERATION.

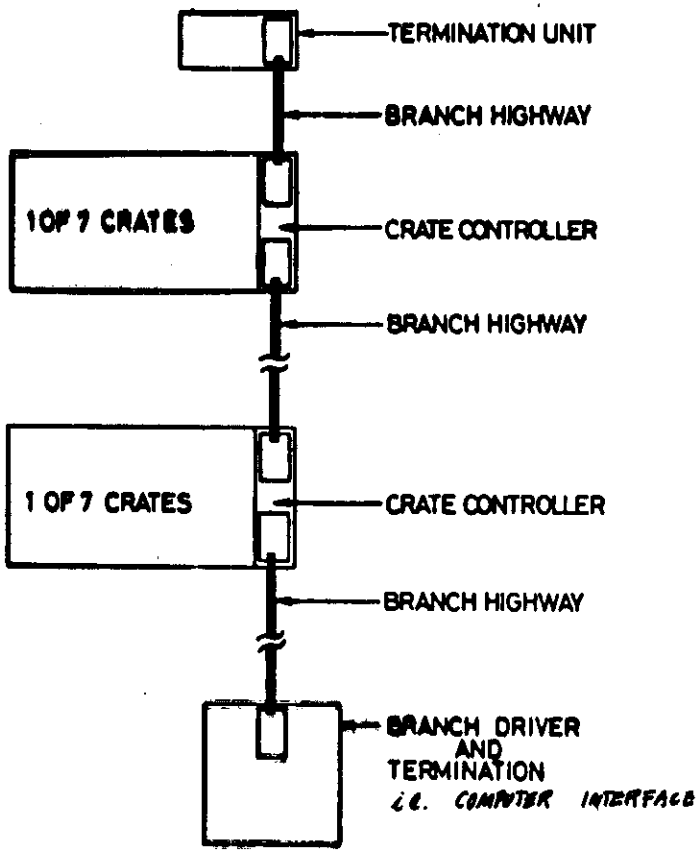


Fig. 1. CAMAC BRANCH: CHAIN CONFIGURATION

CAMAC BRANCH

TO { N / A / F } OF DATAWAY

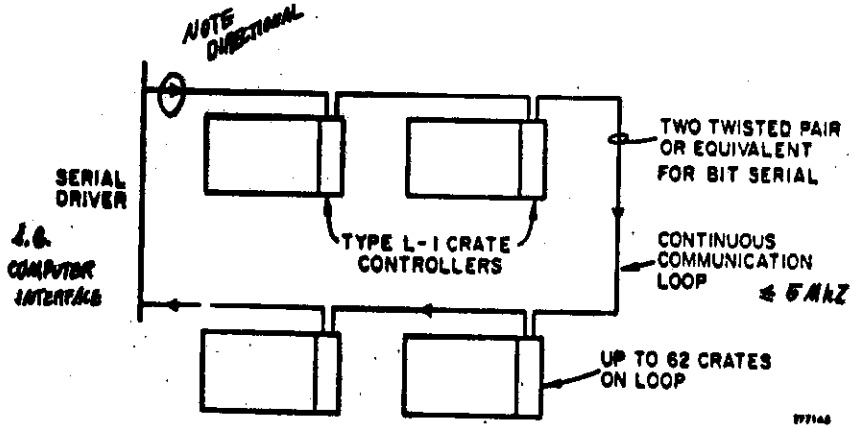
ADD BCR1, BCR2, ... BCR7
EACH ADDRESSES ONE CRATE

} ADDRESSING

COMBINE R & W TO BRW } DATA

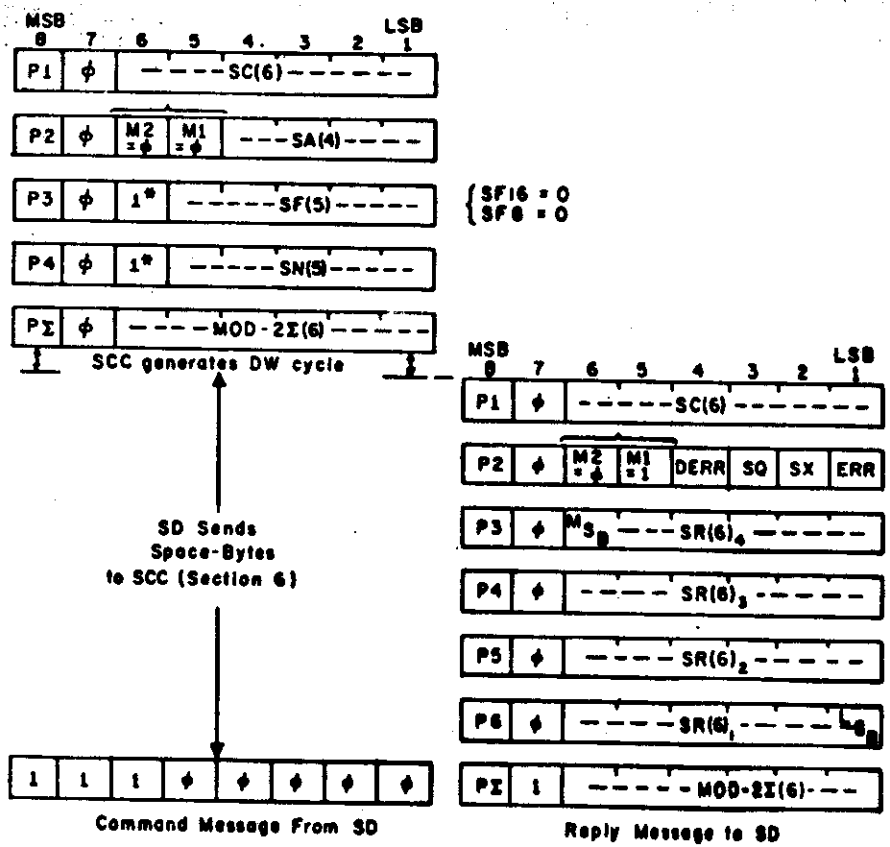
ADD BTA
BTB1, ... BTB7 } TIMING

SIMILIAR TO UNIBUS



CAMAC SERIAL HIGHWAY

4.2.5 Command-Reply Message Sequence-Read



* Reserved bit
ϕ = logic "0"
1 = logic "1"

~ 20 μsec Bit Serial
~ 2.5 μsec Byte Serial

CAMAC "INTERRUPTS"

CALLED 'LOOK-AT-ME' on DATAWAY
OR
'BRANCH DEMAND' on BRANCH
'DEMAND MESSAGE' on SERIAL HIGHWAY

SOURCE IS MODULE IN CRATE

L-LINE (LOOK-AT-ME) GOES TO CRATE CONTROLLER

ON BRANCH

UNIQUE BRANCH DEMAND LINE

DRIVER MUST POLL TO FIND CRATE

THEN READS 'L' PATTERN

THEN WITHIN MODULE (MAYBE)

ON SERIAL

DEMAND MESSAGE INSERTED IN STREAM

↳ CONTAINS CRATE CONTROLLER ADDRESS
+ MODULE ADDRESS

MULTIPLE CRATE CONTROLLERS

REQUIREMENTS

HAS N encoded L all (ACC)

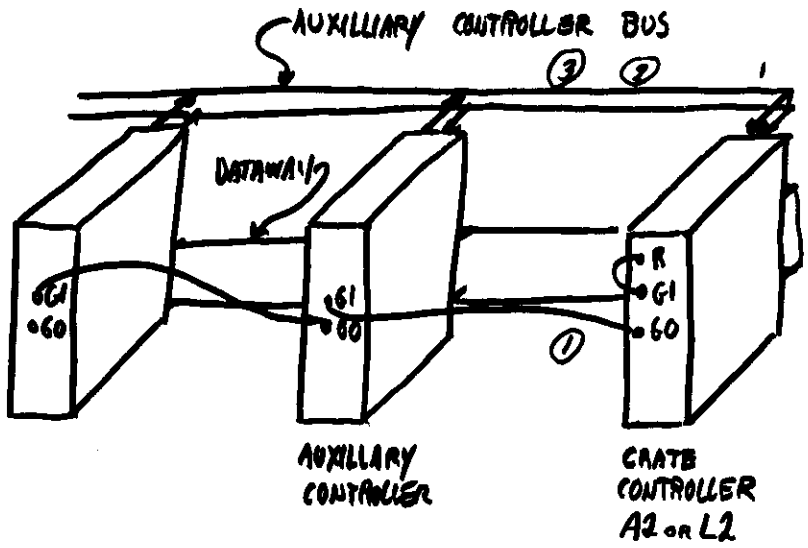
1. N AND L LINES TO AUXILIARY'S
2. L LINES D.C.
3. PRIORITY ARBITRATION
4. SERIAL OR PARALLEL SYSTEMS

HAVE ALREADY

OPEN COLLECTOR CONTROL LINE DRIVERS

CAMAC BUS ARBITRATION

ONLY OFFICIALLY ON DATAWAY (CRATE)



① ARBITRATION

3 BUSSED LINES: REQUEST, REQUEST INHIBIT, ACL

1 DAISEY CHAIN: GRANT-IN, GRANT-OUT

CABLE

② ENCODED-N LINES: CC DOES DECODING TO N_i

③ BUSSED L LINES: ACC CAN HANDLE LAM'S

BUSES TIE SYSTEM TOGETHER

- DIVIDE SYSTEM INTO UNITS
  - BOARD OR CHASSIS
  - FUNCTIONAL MODULARITY
- ADD NEW UNITS
  - NO REDESIGN
  - HOME MADE SPECIAL PURPOSE
- RECONFIGURE SYSTEM
  - EXPERIMENTAL NEEDS CHANGE
  - NEW EQUIPMENT BECOMES AVAILABLE
- TEST AND/OR REPAIR UNITS SEPERATELY
  - TEST BENCH AWAY FROM EXPERIMENT

STANDARD BUSES

- WELL DEFINED SPECIFICATIONS
  - BUS PROTCOL
  - MECHANICAL
  - → SAVES EFFORT COMPARED TO RE-INVENTING
- COMMERICAL UNITS AVAILABLE
  - MULTIPLE VENDORS ON MANY UNITS
  - LARGE RANGE
  - WELL TESTED
  - DOCUMENTATION
  - → SAVES EFFORTS COMPARED TO DESIGNING EVERYTHING
- SHARED EXPERIENCE
  - APPLICATION NOTES
  - SOFTWARE
  - ASSISTANCE FROM OTHERS
  - BORROW SPECIAL PURPOSE DESIGNS

HOW TO CHOOSE A (STANDARD) BUS

1) NEEDS

- MEMORY SPACE
- BUS MASTERSHIP
- INTERRUPTS
- MECHANICS
  - CARDS / CRATE

2) AVAILABILITY

- LOCAL VENDORS / IMPORTERS
- NUMBER OF MANUFACTURERS

3) COSTS

4) EXPERIENCE

- EXISTING EQUIPMENT
- SOFTWARE
- OTHERS

Ordering Interface Standards

IEEE	ANSI	IEC	EIA
IEEE 488-1978	ANSI MC1.1	IEC 625-1	*EIA RS-232-C
"Digital Interface for Programmable Instrumentation"	"Digital Interface for Programmable Instrumentation"	"An Interface System for Programmable Measuring Apparatus (Byte Serial Bit Parallel)"	"Interface Between Data Terminal Equipment and Communication Equipment Employing Serial Binary Data Interchange"
IEEE STANDARDS	ANSI STANDARDS	IEC STANDARDS	EIA STANDARDS
345 E. 47th Street New York, New York 10017 Price: $9.50 (U.S.)	1430 Broadway New York, New York 10018 Price: $10.00 (U.S.)	1, rue de Varembe 1211 Geneva 20 Switzerland Price: 150 Swiss Francs	2001 Eye St. N.W. Washington, D.C. 20006 Price: $5.10 (U.S.)

*recommended companion document "Industrial Electronics Bulletin No. 9 — Application Notes for EIA Standard RS-232-C" ($2.60 in U.S.)