INTERNATIONAL ATOMIC ENERGY AGENCY
UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION

INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS
34100 TRIESTE (ITALY) - P.O.B. 586 - MIRAMARE - STRADA COSTIERA 11 - TELEPHONES: 224281/2/3/4/5/6
CABLE: CENTRATOM - TELEX 460392-1

SMR/90 - 6

COLLEGE ON MICROPROCESSORS:

TECHNOLOGY AND APPLICATIONS IN PHYSICS

7 September - 2 October 1981

MICROPROCESSOR ARCHITECTURE

M.D. EDWARDS

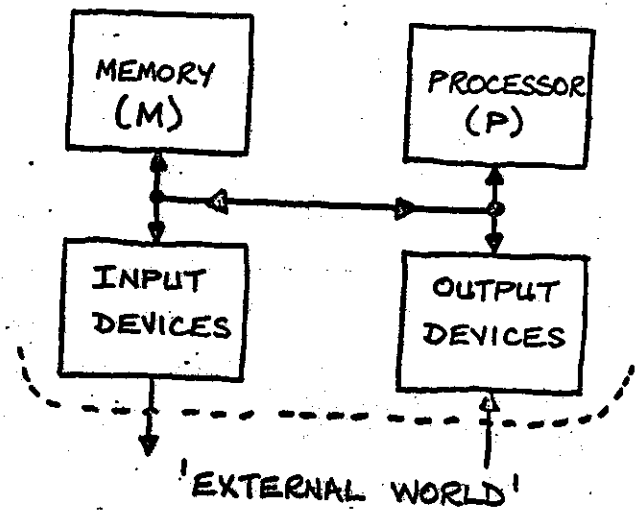
Computation Dept.
U.M.I.S.T.
Manchester
England

MICROPROCESSOR ARCHITECTURE

DR. MARTYN D. EDWARDS,
COMPUTATION DEPT.,
U.M.I.S.T.,
MANCHESTER,
ENGLAND,
U.K.

- OBJECTIVE
  TO ASCERTAIN HOW A COMPUTER MAY BE IMPLEMENTED ON AN INTEGRATED CIRCUIT.

COMPUTER ARCHITECTURE

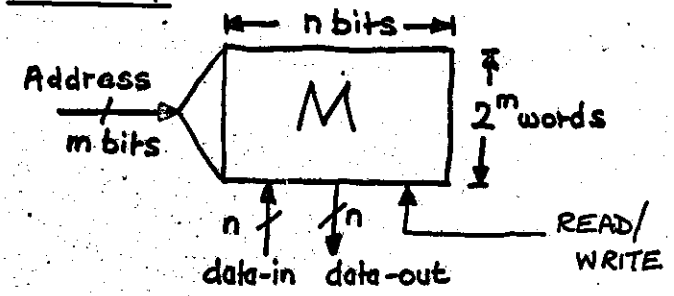


- WHAT DOES A COMPUTER DO?
  - IT TAKES IN INFORMATION FROM THE EXTERNAL WORLD (THROUGH INPUT DEVICES), PERFORMS SOME ARITHMETIC AND LOGICAL OPERATIONS ON THE INFORMATION (THROUGH THE MEMORY & PROCESSOR) AND PRODUCES DATA FOR THE EXTERNAL WORLD (THROUGH OUTPUT DEVICES).

- WHAT ARE THE MAIN COMPONENTS?
  - PROCESSOR
    - HEART OF THE COMPUTER WHICH CONTAINS ELEMENTS FOR PERFORMING ARITHMETIC AND LOGICAL OPERATIONS ACCORDING TO SOME DEFINED SEQUENCE OF INSTRUCTIONS.
  - MEMORY
    - BLOCK OF REGISTERS (BINARY WORDS) WHICH CONTAIN THE PROGRAM (SEQUENCE OF INSTRUCTIONS) & DATA (OPERANDS) FOR THE PROCESSOR
  - INPUT AND OUTPUT DEVICES
    - SUPPLY THE DATA NEEDED BY THE COMPUTER FROM THE EXTERNAL WORLD AND PASS 'PROCESSED' DATA TO THE EXTERNAL WORLD

(LEAVE I/O FOR THE PRESENT)

MEMORY



- MEMORY UNIT contains information to be used by the processor in the form of INSTRUCTIONS and OPERANDS.
- Memory contains registers (LOCATIONS) that hold an element of data or an instruction.
- A memory location is characterised by:
  - ADDRESS : specifies which memory location is to be read or written to
  - CONTENTS : data physically stored in the location.

- The information stored in a memory location is in the form of bits (0 or 1) - known as a WORD. The number of bits (n) in a memory location determines the operating parameters for the whole system. This is known as the WORD LENGTH; typically 4, 8, 16, 24, 32 bits.
- The size of the memory determines the power of the computer in terms of the amount of data & instructions which may be held in it. If the ADDRESS is m bits wide, then the maximum memory is 2^m words. Typically m = 12, 16, 20, 24, ... bits.
- MEMORIES may be written to or read from by the processor (RWM).

  However, there are memories which may only be read (ROM), and they are used for storing programs only.

PROGRAMS, INSTRUCTIONS, OPERANDS

PROGRAM

- set of instructions which has been created by the programmer & loaded into the memory. Instructions are stored and obeyed one at a time by the processor. The program defines the task that the computer performs

INSTRUCTION

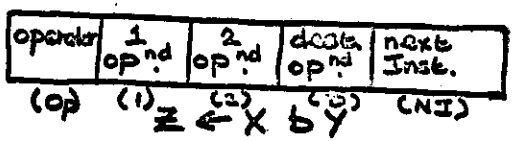
- command executed by the processor on information presented to it
  - OPERATION INSTRUCTIONS (arithmetic, move, logical)
  - CONTROL INSTRUCTIONS (modify the normal flow of operations in the program)

OPERAND

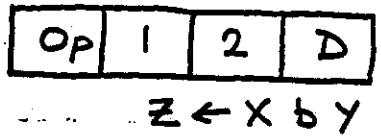
- information unit stored in memory which is operated on by the processor when executing an instruction.

INSTRUCTION TYPES

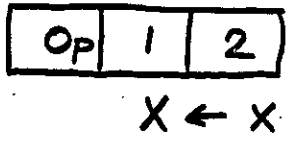
GENERAL 3 ADDRESS



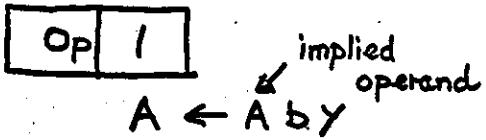
3 ADDRESS



2 ADDRESS



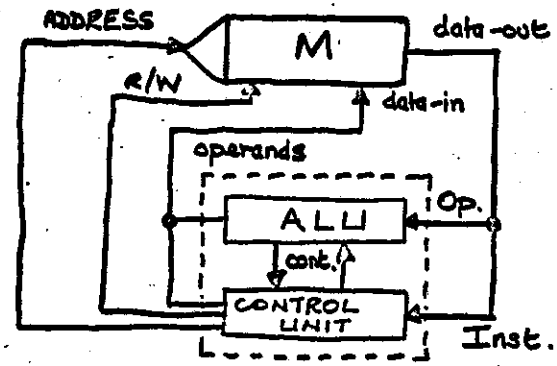
1 ADDRESS



0 ADDRESS

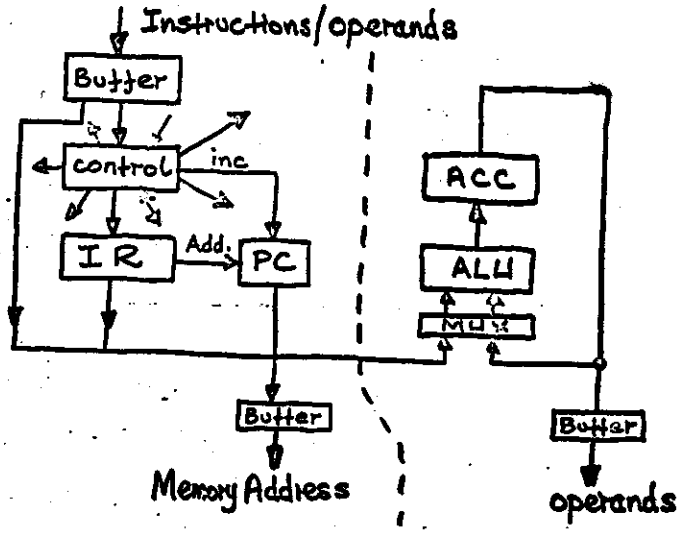
- 3 ADDRESS is the most powerful but they are wasteful in memory
- Normally compromise with less flexible BUT less wasteful instructions typically : 2 & 1 ADDRESS

▪PROCESSOR



- CONTROL UNIT
  - controls the actions of the processor & the memory. Sequence of activities is governed by the instructions in the memory
    - FETCH INSTRUCTIONS
    - DECODE INSTRUCTIONS
      - CONTROL ALU
    - FETCH OPERANDS
    - WRITE OPERANDS
- ALU
  - performs operations, determined by the instructions, on the operands fetched by the control unit.

SIMPLE PROCESSOR



- IR - Instruction register
- PC - Program counter
  - Address of the next instruction to be executed { PC ← PC+1 / PC ← (absolute address) }
- ACC - Accumulator
  - dedicated register which receives results from the ALU (1,2 address machine)
- ADDRESS = m bits (PC)
- ACC, IR normally n bits (WORD LENGTH)

PROCESSOR ACTIVITY

- processor, governed by the control unit, executes instructions according to a predefined sequence.
- sequence is known as the instruction cycle
- length (in time) of the instruction cycle is dependent upon the type of instruction being executed.

INSTRUCTION CYCLE

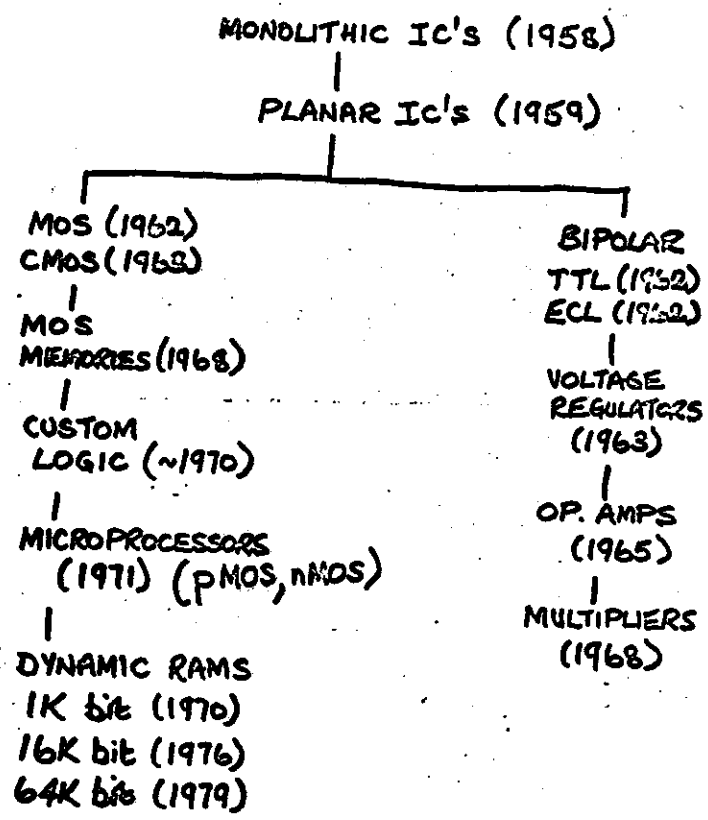
- FETCH NEXT INSTRUCTION : LOCATED AT PC
- DECODE INSTRUCTION : control unit identifies the instruction and initiates the appropriate actions.
- FETCH OPERANDS : control unit instigates the fetching of the required operands.
- EXECUTE INSTRUCTION : ALU performs the required operation. Result stored in ACC or memory

■ Above cycle is repeated for every instruction

TIMING IS CONTROLLED BY A CLOCK

- IMPLEMENTATION
  - IMPLEMENT
    - ALU section } PROCESSOR
    - CONTROL UNIT }
    - ROM } MEMORY
    - RWM }
    - INPUT/OUTPUT DEVICES
  - CONSIDERATIONS
    - WORD LENGTH (4, 8, 16, 32, ... bits)
    - COMPONENTS / CHIP
    - NUMBER OF PINS ON PACKAGED CHIP
    - POWER DISSIPATION
    - TECHNOLOGY
    - SPEED
    - DEVICE FUNCTIONAL COMPLEXITY

[ALL THESE CONSIDERATIONS ARE INTERDEPENDENT]



I.C. DEVELOPMENT

CHIP COMPLEXITY vs TECHNOLOGY

DATE	ELEMENTS/CHIP	FUNCTIONS/CHIP
60's -	100 ~ 500	GATES, FLIP-FLOPS
60's +	1000 ~ 5000	SHIFT REGS, COUNTERS
70's -	5K ~ 20K	1-4K RAMS, 4,8 bit µP's
70's +	20K ~ 125K	16-64K RAMS, 16 bit µP's
80's -	125K ~ 750K	256K-1M RAMS, MICROCOMPUTERS
80's +	750K ~ 5M	LARGE MEMORIES, COMPLETE SYSTEMS
90's	5M ~ 32M	?

ACTUAL IMPLEMENTATIONS

- ALU section
  - ▫ single IC
  - ▫ bit slice
- CONTROL UNIT
  - ▫ single IC
  - ▫ same IC as ALU
  - ▫ bit slice
- MEMORY
  - ▫ single IC
  - RWM static : → 1K x 8
  - RWM dynamic : → 64K x 1
  - ROM PROM : → 4K x 8
- INPUT/OUTPUT DEVICES
  - ▫ single IC

→ increasing complexity

LIMITATION : SIZE OF IC
+ NUMBER OF PINS
+ COMPONENTS/CHIP

MICROPROCESSOR

- ALU section and control unit on a single integrated circuit
- evolved from 4 → 8 → 16 → 32 bits as the technology (PMOS → nMOS) has improved and permitted more components/chip ⇒ more complex devices
- TYPES

4 bit μP → OBSOLETE (I4040)

8 bit μP → STANDARD (I8085, M6800, Z80)

8 bit microcomputer → standard (I8048)

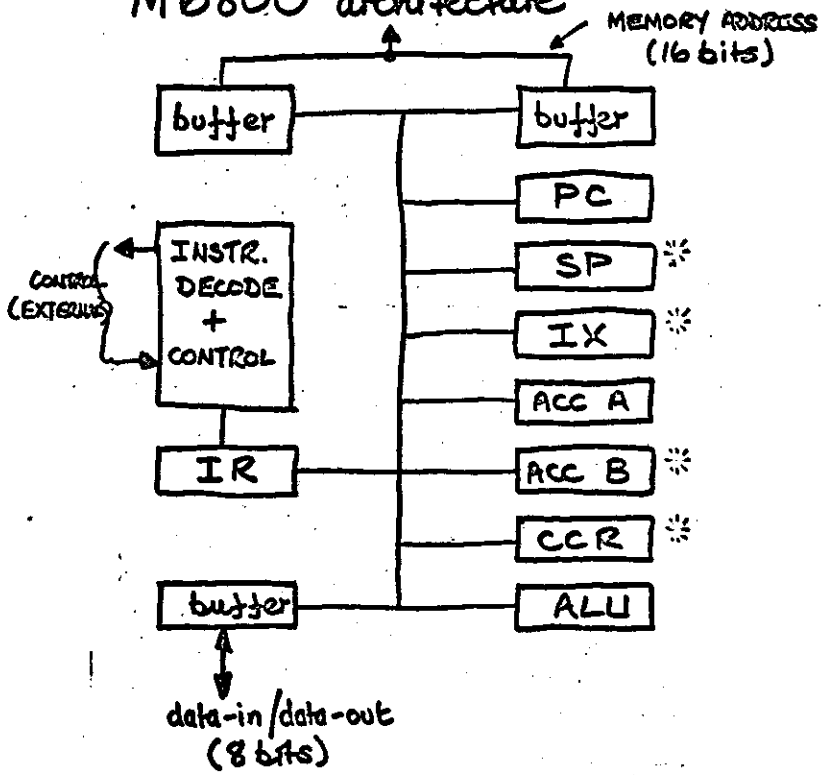
16 bit μP → available (I8086, Z8000, M68000)

32 bit μP → coming soon (I432)

↓

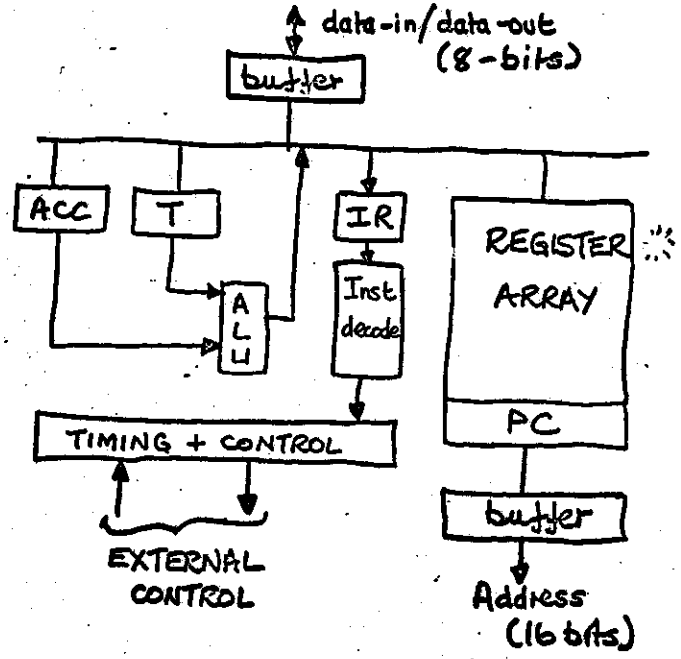
?

M6800 architecture



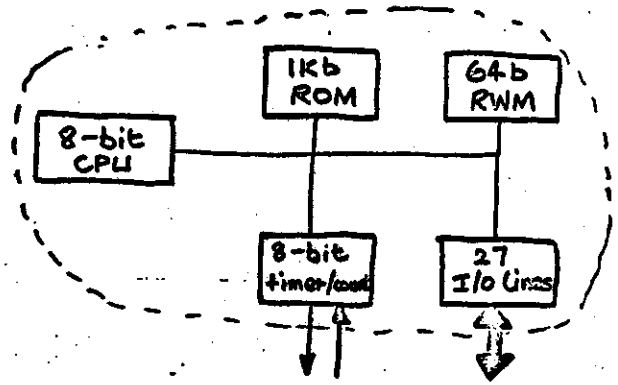
* ON CHIP REGISTERS
  - REALLY 'FAST' MEMORY ON THE MICROPROCESSOR

I8080 architecture



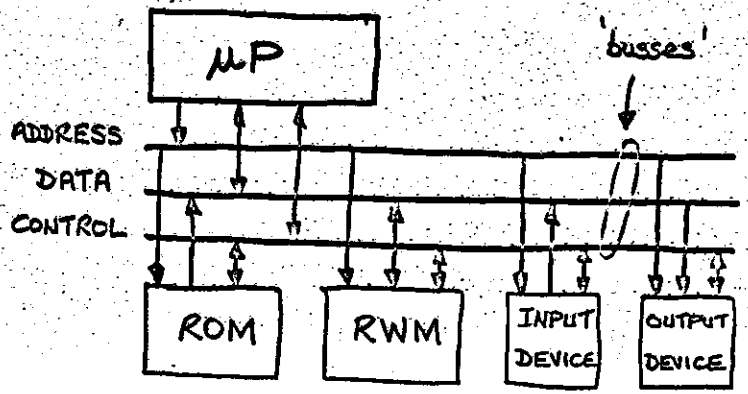
* AGAIN THERE ARE ON-CHIP REGISTERS (> M6800)

I8048 architecture

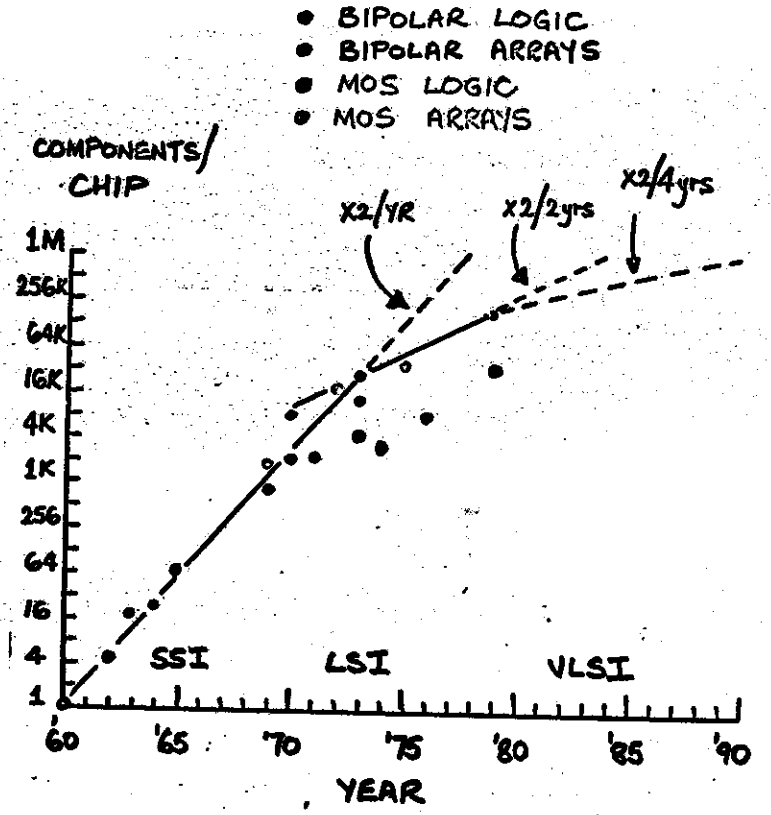


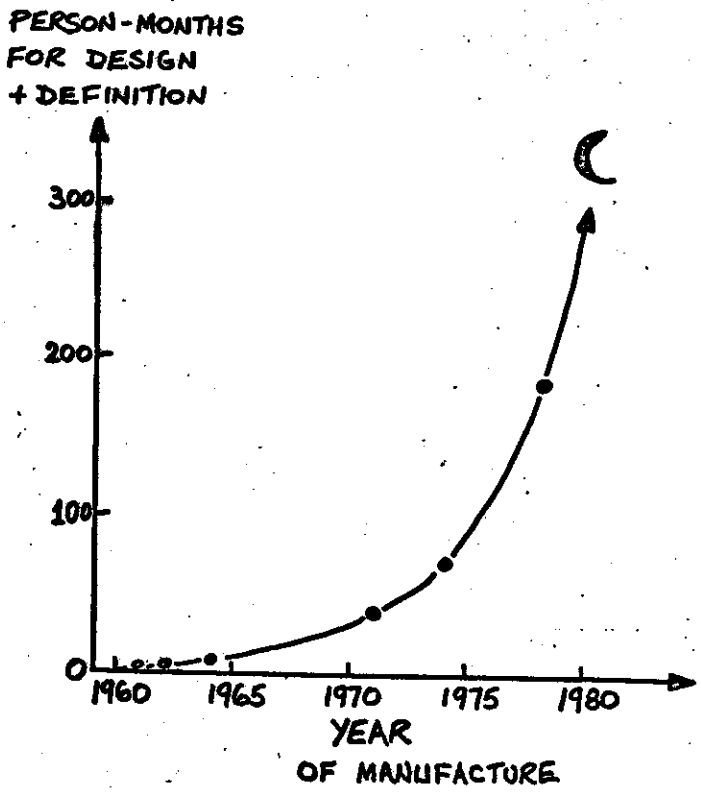
- MICROCOMPUTER
  - CPU
  - MEMORY
  - INPUT/OUTPUT
- USED IN 'SMALL APPLICATIONS'
  - PETROL PUMPS
  - POS TERMINAL
- Instructions are not as 'powerful' as 8-bit µP's
- difficult to expand memory + I/O

MICROPROCESSOR SYSTEM



- COMMUNICATION WITHIN A MICROPROCESSOR SYSTEM IS ACHIEVED WITH BUS STRUCTURES





(AFTER GORDON MOORE)

FUTURE

- AS TECHNOLOGY ADVANCES
  - ⇩
  - MORE COMPONENTS / CHIP
  - ⇩
  - GREATER COMPLEXITY (IBM 370, CRAY I)
- AS COMPLEXITY INCREASES
  - ⇩
  - LONGER TO DESIGN MICROPROCESSORS
  - ⇩
  - RAPID EVOLUTION WILL SLOW DOWN

SUMMARY

- REVIEW OF COMPUTER ARCHITECTURE
- TECHNOLOGICAL ADVANCES HAVE PERMITTED A PROCESSOR TO BE MANUFACTURED ON A SINGLE INTEGRATED CIRCUIT
  - MICROPROCESSOR
- FUTURE HOLDS NO BOUNDS IF WE CAN MANAGE THE COMPLEXITY.