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COLLEGE ON MICROPROCESSORS:

TECHNOLOGY AND APPLICATIONS IN PHYSICS

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# PROCESSOR-MEMORY SYSTEM

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# PROCESSOR-MEMORY SYSTEM



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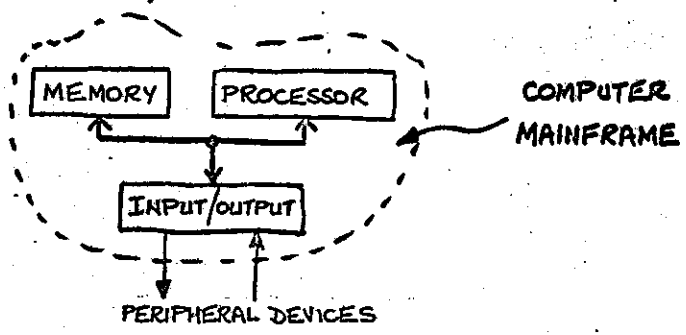
OBJECTIVE : TO EXAMINE THE PATHS THAT CONNECT A PROCESSOR TO THE MEMORY AND INPUT-OUTPUT SYSTEM.



## • COMPONENTS OF A µP SYSTEM



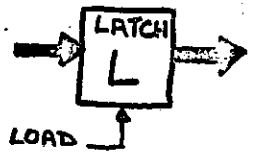

- PROCESSOR, PROGRAM, OPERAND MEMORY
- PERIPHERAL IMAGE MEMORY
  - CONNECTS THE PROCESSOR TO ITS PERIPHERALS.
  - LIKE MAIN MEMORY : ARRAY OF REGISTERS
- ABLE TO DESCRIBE PATHS THAT CONNECT THE MEMORIES TO THE PROCESSOR.


- SWITCH (S) CONTROLS THE INTERACTIONS WITH THE PROCESSOR AND ITS MEMORIES.

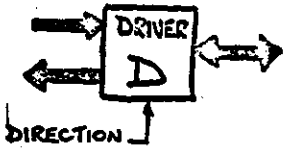
## BACKGROUND + CONVENTIONS



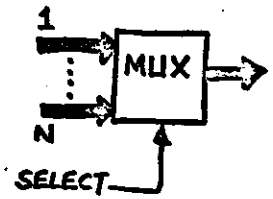
- INITIALLY ASSUME IMAGE + OPERAND MEMORIES ARE IN THE SAME ADDRESS SPACE (DIFFERENCES LATER)
- IN ORDER TO DESCRIBE THE ROUTES BETWEEN THE PROCESSOR + MEMORIES NEED TO DEFINE SOME SWITCH DEVICES




- STORES DATA UNTIL OVERWRITTEN.
- OUTPUT IS 'STATIC'
- LOADED BY 'LOAD' CONTROL SIGNAL.



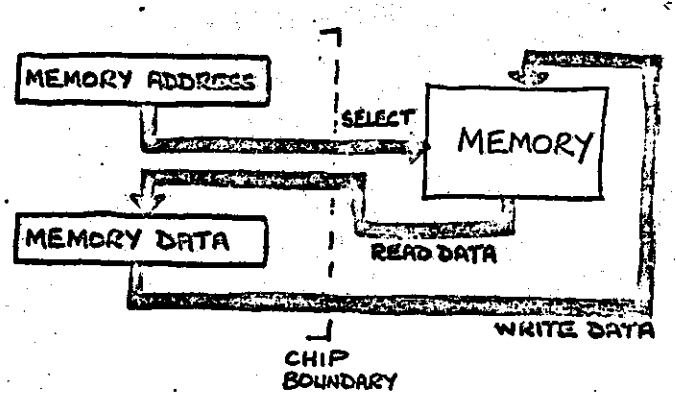

- DRIVES DATA FROM THE INPUT ONTO THE BIDIRECTIONAL LINE OR READS DATA FROM THE BIDIRECTIONAL LINE ONTO THE OUTPUT.
- CONTROLLED BY THE 'DIRECTION' CONTROL SIGNAL




- ROUTES ONE OF N INPUTS ONTO THE SINGLE OUTPUT.
- CONTROLLED BY THE 'SELECT' CONTROL LINE(S).

## SIMPLIFIED PROCESSOR



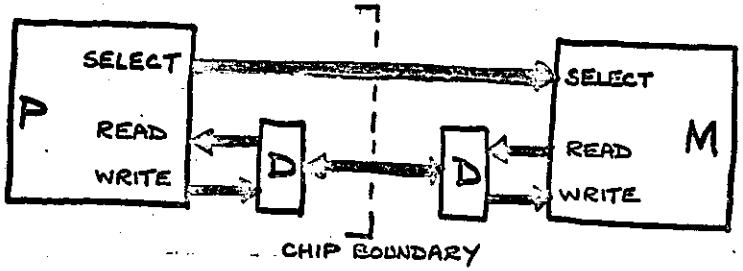



- PROCESSOR
  - SOURCE OF MEMORY ADDRESS (PC, IX, SP, .....)
  - SOURCE/DESTINATION OF MEMORY DATA
    - STATIC
    - DESTINATION : IR, ALU reg, GENERAL REG.
    - SOURCE : OPERAND reg.
- MEMORY
  - SELECT INPUT DEFINES MEMORY LOCATION
  - READ DATA ROUTE
  - WRITE DATA ROUTE
  - READ/WRITE CONTROL TO DEFINE MEMORY FN.
    - SIGNAL R/W
      - 1 = READ : 0 = WRITE
- ACTIVITIES
  - GENERATE SELECT
  - READ/WRITE DATA

TIMING ACTIVITY IS IMPLICIT

# PROCESSOR-MEMORY ROUTES

## 1. BIDIRECTIONAL DATA - DIRECT ADDRESS




- BIDIRECTIONAL DATA ROUTE
- 1 CONTROL SIGNAL READ/WRITE
  - SETS DIRECTION OF THE DRIVERS

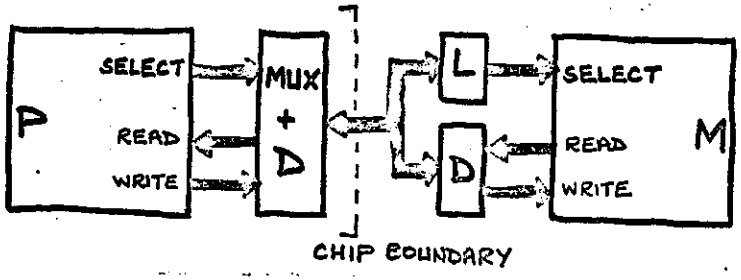
PIN COUNT = $N_{pn} = N_A + N_D + 1$

| PROCESSOR | WORD LENGTH ($N_D$) | ADDRESS ($N_A$) | MEMORY SIZE (K) | PIN COUNT ($N_{pn}$) |
|---|---|---|---|---|
| 8080 | 8 | 16 | 64 | 25 |
| 6800 | 8 | 16 | 64 | 25 |
| Z80 | 8 | 16 | 64 | 25 |
| 6501/2 | 8 | 16 | 64 | 25 |
| 6504 | 8 | 13 | 8 | 22 |
| 6503/5 | 8 | 12 | 4 | 21 |
| EA 9002 | 8 | 12 | 4 | 21 |
| PPS-8 | 8 | 14 | 16 | 23 |
| 2650 | 8 | 15 | 32 | 24 |
| TMS9900 | 16 | 16 | 32 | 33 |



## 2. SINGLE MULTIPLEXED ROUTE

- ADDRESS = DATA WIDTH

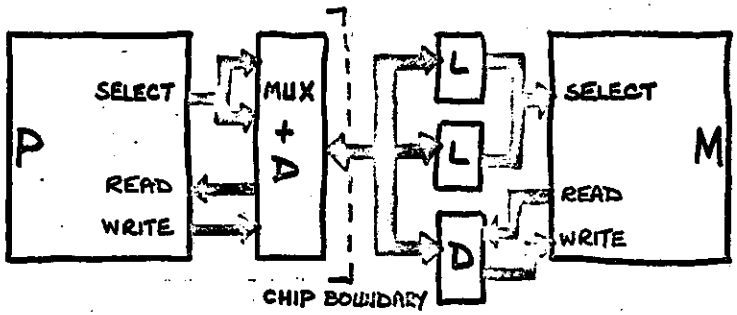



- REDUCED PIN COUNT BY MULTIPLEXING ADDRESS + DATA
- MUX + DRIVERS ARE COMBINED IN THE CHIP
- DEMULTIPLEXED EXTERNALLY
- 2 BEATS TO LOAD ADDRESS AND DATA
- ASSUME $N_A = N_D = N_P$ · $N_P$ = width of data port
- PIN COUNT = $N_{pn} = N_P + 2$
  - 1 READ/WRITE
  - 1 LOAD ADDRESS LATCH

| PROCESSOR | WORD LENGTH ($N_D = N_P$) | ADDRESS ($N_A$) | LATCH ($N_1$) | MEM SIZE (K) | $N_{pn}$ |
|---|---|---|---|---|---|
| GI-1600 | 16 | 16 | 16 | 64 | 18 |
| PACE | 16 | 16 | 16 | 64 | 18 |
| MPS-1600 | 16 | 16 | 16 | 64 | 18 |
| IM-1600 | 12 | 12 | 12 | 4 | 14 |
| 8048 (data) | 8 | 8 | 8 | 1/4 | (14) |
| F100 | 16 | 15 | 15 | 32 | 18 |

## 3. SINGLE MULTIPLEXED ROUTE

• ADDRESS > DATA WIDTH



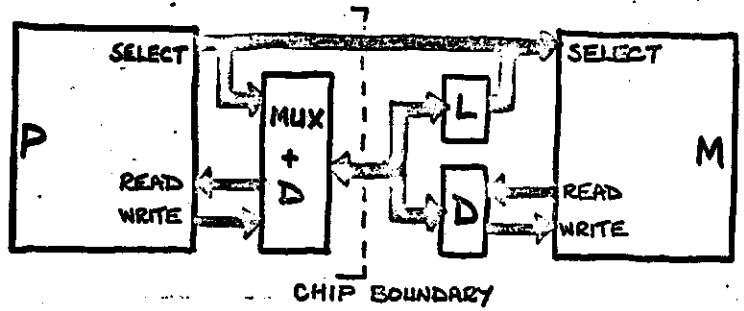

- VARIATION IS REQUIRED IF $N_A > N_P$
- ADDRESS IS SENT IN TWO BEATS
  - 3 BEATS TOTAL
- PIN COUNT = $N_{pn} = N_P + 3$
  - 1 READ/WRITE
  - 2 LOAD ADDRESS LATCHES

| PROCESSOR | WORD LENGTH ($N_D = N_P$) | ADDRESS ($N_A$) | LATCH ($N_1$) | MEM SIZE(K) | $N_{pn}$ |
|---|---|---|---|---|---|
| CRD-8 | 8 | 16 | 8+8 | 64 | 11 |
| I8008 | 8 | 14 | 8+6 | 16 | 11 |



## 4. BIDIRECTIONAL DATA - MULTIPLEXED ADDRESS

• MULTIPLEXED DATA ROUTE



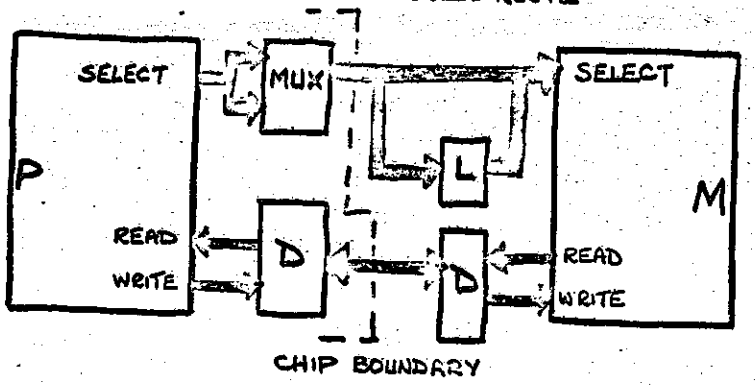

- INTERMEDIATE SOLUTION WHEN $N_A > N_D$
  - FASTER THAN SINGLE MULTIPLEXED ROUTE
  - NEEDS MORE PINS
- PART OF THE ADDRESS IS MULTIPLEXED WITH THE DATA
- REQUIRE A SINGLE LATCH, LENGTH $N_1$,
  - EXTRA CONTROL SIGNAL (LOAD LATCH)
- PIN COUNT = $N_{pn} = (N_A - N_1) + N_D + 2$
  - $N_1 \leq N_D$

| PROCESSOR | WORD LENGTH $N_D$ | ADDRESS $N_A$ | LATCH $N_1$ | MEM SIZE(K) | $N_{pn}$ |
|---|---|---|---|---|---|
| 8085 | 8 | 16 | 8 | 64 | 18 |
| 8048(prog) | 8 | 12 | 8 | 4 | 14 |
| MK5065 | 8 | 15 | 8 | 32 | 17 |

## 5. BIDIRECTIONAL DATA - MULTIPLEXED ADDRESS

• MULTIPLEXED ADDRESS ROUTE





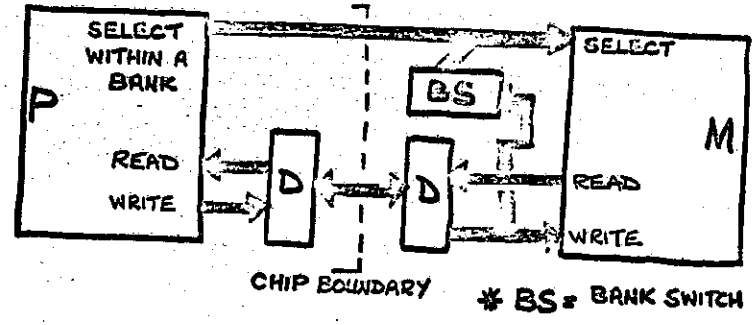

- AGAIN $N_A > N_D$
- ADDRESS IS MULTIPLEXED RATHER THAN THE DATA ROUTE
- REQUIRE A SINGLE LATCH, LENGTH $N_1$
  - EXTRA CONTROL SIGNAL (LOAD LATCH)

- PIN COUNT = $N_{pn} = (N_A - N_1) + N_D + 2$
  - $2N_1 \leq N_A$

| PROCESSOR | $N_D$ | $N_A$ | $N_1$ | MEM SIZE(K) | $N_{pn}$ |
|---|---|---|---|---|---|
| COSMAC | 8 | 16 | 8 | 64 | 18 |

## 6. BANK SWITCHING






- BANK SWITCHING EXTENDS BASIC ADDRESSING RANGE TO PROVIDE A LARGER MEMORY SPACE
- SOME µP's HAVE INBUILT BANK SWITCHING (SEE BELOW)
- ADDRESS IS CONCATENATED WITH $N_B$ BITS OF THE BANK SWITCH REGISTER TO PROVIDE FULL MEMORY ADDRESS
- SPECIAL INSTRUCTION TO LOAD BANK REGISTER
- PIN COUNT = $(N_A - N_B) + N_D + 2$
  - 1 READ/WRITE
  - 1 LOAD BANK REG.

| PROCESSOR | $N_D$ | $N_A$ | $N_B$ | BANKS | SIZE | TOTAL | $N_{pn}$ |
|---|---|---|---|---|---|---|---|
| SC/MP | 8 | 16 | 4 | 16 | 4K | 64K | 22 |
| CDP 1801 | 8 | 16 | 8 | 256 | 1/4 | 64K | 18 |

- BANK SWITCHING IS NOT FREQUENTLY USED DUE TO PROGRAMMING DIFFICULTIES WHEN SWITCHING MEMORY BLOCKS
- LATEST µP's (16-bit) HAVE A LARGE ADDRESSING SPACE ≥ 20 BITS (≥ 1 M bytes)

(Z8000, M68000, I 8086)

## SUMMARY : PROCESSOR-MEMORY ROUTES



- INDICATED THE MAIN FEATURES OF THE P-S-M ORGANISATION FOUND ON MOST µP's
- BIDIRECTIONAL DATA - DIRECT ADDRESS
  - POPULAR
  - HIGH SPEED
  - SIMPLE MEMORY INTERFACE
  - TENDS TO A LARGE NUMBER OF PINS
- SINGLE MULTIPLEXED ROUTE
  - POPULAR WITH 16bit µP's (earlier ones)
  - SLOW
  - LARGE ADDRESS LATCH
- BIDIRECTIONAL DATA - MULTIPLEXED ADDRESS
  - POPULAR WITH LATER µP's
  - NO APPARANT LOSS OF SPEED OVER 'DIRECT ADDRESS'
  - SIMPLE LATCH
  - GAIN ~ 7 PINS
- PIN COUNT
  - FIGURES GIVEN ARE HYPOTHETICAL
  - PINS MAY HAVE MULTIPLE FUNCTIONS
- ADDITIONAL FUNCTIONS
  - EXTRA SWITCH INFORMATION (INSTRUCTION FETCH, MEMORY R/W, STACK R/W)
  - CODED FUNCTIONS : 2 PINS COULD PROVIDE 4 SIGNALS

## SIGNALLING



- SIGNALS ARE SUPPLIED BY THE µP WHICH DICTATE WHEN VALID TRANSACTIONS MAY OCCUR.
- SIGNALS DEFINE PROTOCOLS FOR INFORMATION EXCHANGE BETWEEN µP AND MEMORY
- TIMING + SEQUENCE OF SIGNALS IS CRUCIAL!
- TWO CLASSES OF SIGNAL
  1. FUNCTION (WHAT)
  2. TIMING (WHEN)
- FUNCTION SIGNALS
  - READ AND WRITE ARE THE MAIN SIGNALS
  - DISTINGUISH BETWEEN MEMORY AND I/O TRANSFERS (maybe)
  - WITH MULTIPLEXED ROUTES, EXTRA SIGNALS TO LOAD LATCHES
- TIMING SIGNALS
  - RELATED TO THE µP CLOCK
  - SYNCHRONOUS SYSTEM
  - TIMING INFORMATION (WHEN) IS OFTEN ENCODED WITH FUNCTION INFORMATION (WHAT)

  EG. WRITE SIGNAL
  - TRULY TIMING ONLY SIGNALS eg MEMORY READY
- EXAMPLE µP's

**6800**

R/W : READ OR WRITE FUNCTION
VMA : ADDRESS VALID FOR MEMORY CYCLE
DBE : DATA AND ADDRESS ROUTE TIMING

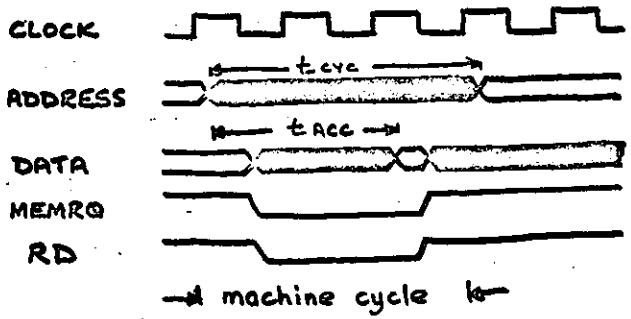
**8085**

ALE : LOAD ADDRESS FROM DATA ROUTE
IO/$\overline{M}$ : I/O OR MEMORY ACCESS
$\overline{RD}$ : READ FUNCTION AND DATA TIMING
$\overline{WR}$ : WRITE FUNCTION AND DATA TIMING
RDY : SYNCHRONISATION FOR SLOW MEMORIES

## • Z80

- MREQ : MEMORY ACCESS FUNCTION
- IORQ : I/O ACCESS FUNCTION
- RD : READ FUNCTION + DATA TIMING
- WR : WRITE FUNCTION + DATA TIMING
- WAIT : SYNCHRONISATION FOR SLOW MEMORY

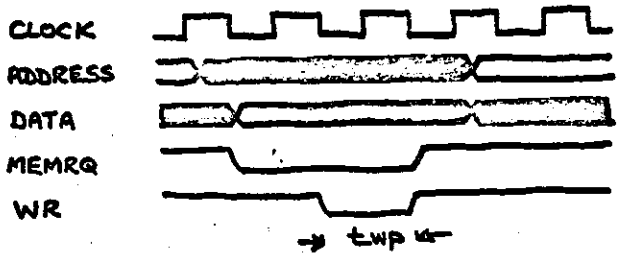
• MEMORY READ CYCLE FOR Z80




tcyc : CYCLE TIME tACC : ACCESS TIME

: ADDRESS VALID : BUS FLOATING : DATA VALID

• MEMORY WRITE CYCLE FOR Z80



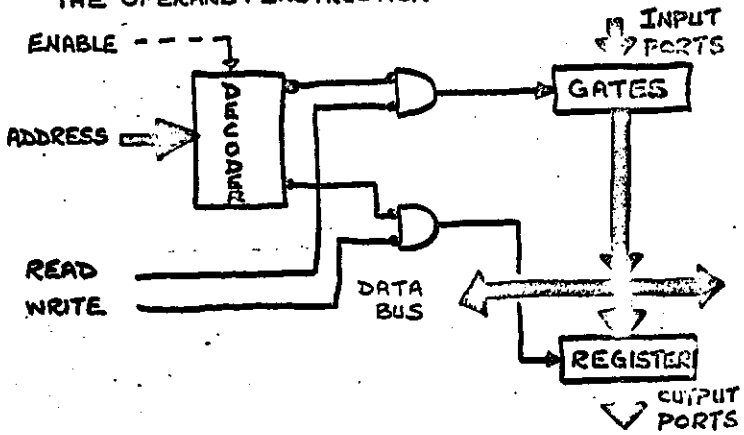

twp = WRITE PULSE WIDTH

(LOOK AT OTHER µP's YOURSELF !)



## • PERIPHERAL IMAGE MEMORY

• DATA AND ADDRESS ROUTES ARE SHARED WITH THE OPERAND / INSTRUCTION MEMORY




• TWO CHOICES FOR THE LOCATION OF THE IMAGE MEMORY
  - MEMORY MAPPED
  - DEDICATED MEMORY

• MEMORY MAPPED
  - REGISTERS ARE SITUATED IN MAIN ADDRESS SPACE
    - ENABLE not present
  - FRAGMENTED MAIN MEMORY
  - RICH SET OF I/O INSTRUCTIONS
    - SAME AS OPERAND ACCESSING
  - REQUIRE LARGE DECODING CIRCUITRY
  - ALL µP's MAY USE MEMORY MAPPED I/O
  - 6800 HAS MEMORY MAPPED I/O ONLY.

## DEDICATED MEMORY



- DEDICATED SMALL MEMORY ASSIGNED TO I/O
  - EXTRA CONTROL SIGNALS (IORQ, IO/M)
  - ENABLE is present
- DISABLE MAIN MEMORY WHEN 'I/O MEMORY' IS ACCESSED
- SPECIAL INPUT-OUTPUT INSTRUCTIONS
- SMALLER DECODERS → SMALLER MEMORY
- RANGE OF µP's WHICH SUPPORT DEDICATED I/O MEMORY

| PROCESSOR | WIDTH (bits) | N° OF PORTS IN | N° OF PORTS OUT | N° OF I/O INSTRUCTIONS |
|---|---|---|---|---|
| 8008 | 8 | 8 | 32 | 1 |
| 8080 | 8 | 256 | 256 | 2 |
| 8085 INT | 1 | 1 | 1 | 2 |
| 8085 EXT | 8 | 256 | 256 | 2 |
| Z80 | 8 | 256 | 256 | 12 |
| 8048 INT | 8 | 2 | | 4 |
| 8048 EXT | 4 | 16 | | 8 |
| 9900 INT | 1 | 1 | 1 | 5 |
| CDP1802 | 8 | 7 | 7 | 2 |
| MK 5065 | 8 | 16 | 16 | 4 |
| 2650 | 8 | 256 | 256 | 2 |
| IM 6100 | 12 | 64 | 64 | 6 |
| F8 | 8 | 256 | 256 | 4 |

INT : Internal } I/O REGISTERS
EXT : External }

## • SPECIAL INPUT-OUTPUT



- LARGE RANGE OF PERIPHERAL CIRCUITS ARE AVAILABLE WHICH ARE IMPLEMENTED ON LSI ELEMENTS
- THREE BROAD TYPES :
  - PROGRAMMABLE PARALLEL I/O
  - SERIAL I/O (PROGRAMMABLE)
  - TIMERS
- PROGRAMMABLE PARALLEL I/O
  - INPUT AND OUTPUT CIRCUITS ON THE SAME PIN OF THE LSI ELEMENT PACKAGE
  - A DIRECTION SIGNAL IS REQUIRED
  - EXAMPLES
    - M6820/1 — 2 8-bit ports
    - I8155 (RWM) — 3 ports : 8,8,6 bits
    - Z80-PIO — 2 8-bit ports
- SERIAL I/O
  - SERIAL/PARALLEL + PARALLEL/SERIAL
  - UART + USART
  - CONTROL WORDS : FORMAT, ERROR DETECTION, BAUD RATE, SYNCH/ASYNCH
  - EXAMPLES
    - M6850 — 1 synch port
    - I8251 — 1 synch/asynch port
    - Z80-SIO — 2 synch/asynch ports
- TIMERS
  - USED IN REAL-TIME APPLICATIONS WHERE 'PROGRAM' TIMING IS NOT ACCURATE ENOUGH
  - DRIVEN BY AN EXTERNAL CLOCK → COUNTER
  - PROGRAMMABLE FOR VARIOUS TIMING FUNCTIONS
  - EXAMPLES
    - I 8253 — 3 16-bit COUNTERS
    - M 6840 — 3 16-bit COUNTERS

## • SUMMARY

- EXAMINED THE VARIOOS SCHEMES FOR CONNECTING μP's TO MEMORIES.
- METHOD FOR CONTROLLING DATA TRANSFERS
  - FUNCTION + TIMING
- EXAMINED PERIPHERAL IMAGE MEMORY REQUIREMENTS
  - MEMORY MAPPED I/O
  - DEDICATED MEMORY
- SPECIAL I/O LSI ELEMENTS
  - PROGRAMMABLE PARALLEL I/O
  - SERIAL I/O
  - TIMERS
- COMPLEX I/O SUBSYSTEMS ARE AVAILABLE
  - FLOPPY DISK CONTROLLER
  - SDLC PROTCCOL CONTROLLER
  - CRT CONTROLLER
  - KEYBOARD/DISPLAY INTERFACE
  - DATA ENCRYPTION UNIT
  - UNIVERSAL PERIPHERAL INTERFACE
  - ALL PROGRAMMABLE