SMR/90 - 10

COLLEGE ON MICROPROCESSORS:

TECHNOLOGY AND APPLICATIONS IN PHYSICS

7 September - 2 October 1981

PRACTICAL COURSE FIGURES

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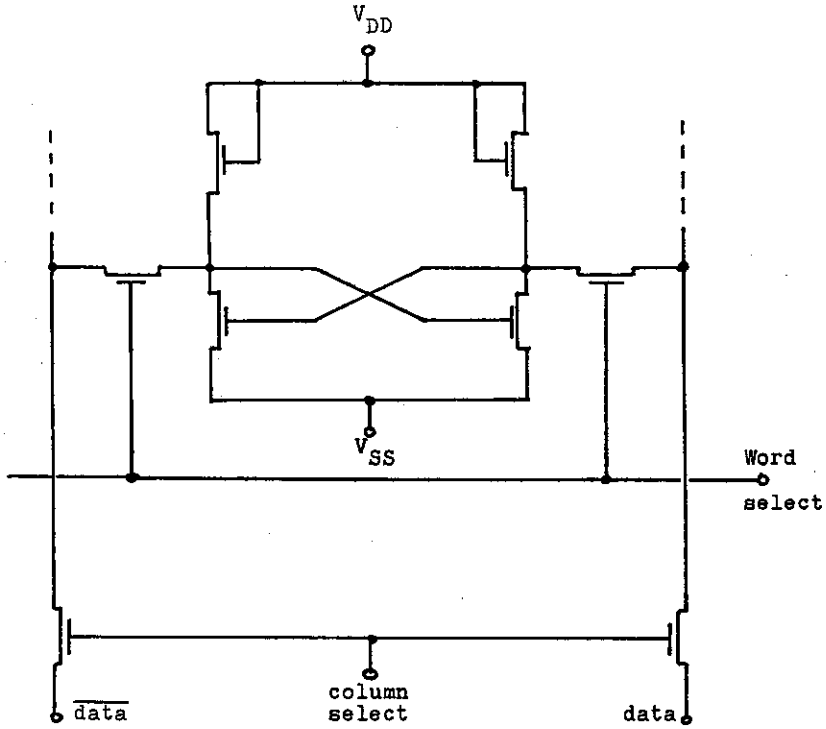
1211 Geneva 23
Switzerland

FIGURE CONTENTS



NMOS: $V_{DD} > 0$ PMOS: $V_{DD} < 0$

$V_{SS} < 0$ $V_{SS} > 0$

Fig. 2.1: Static 6-Transistor Cell

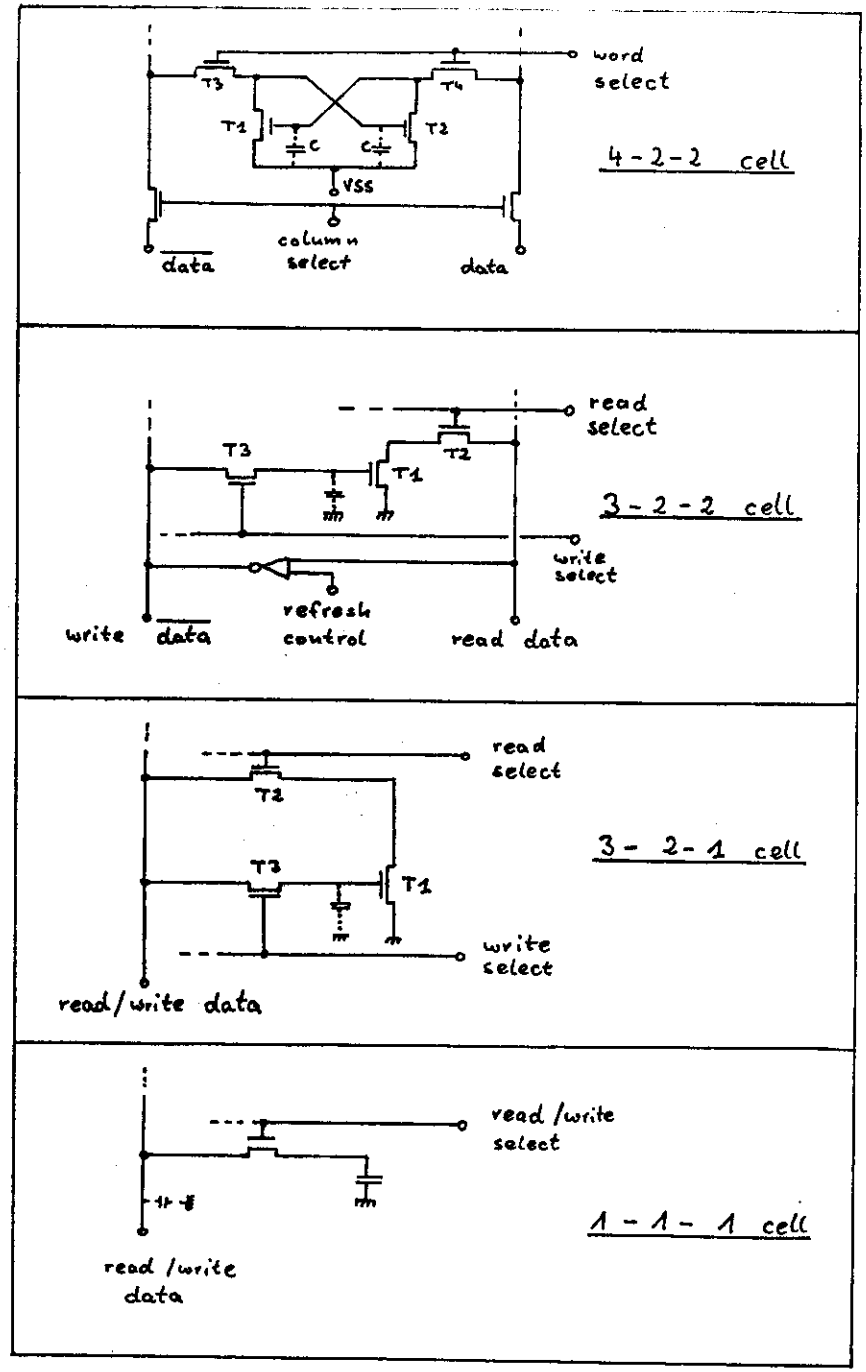
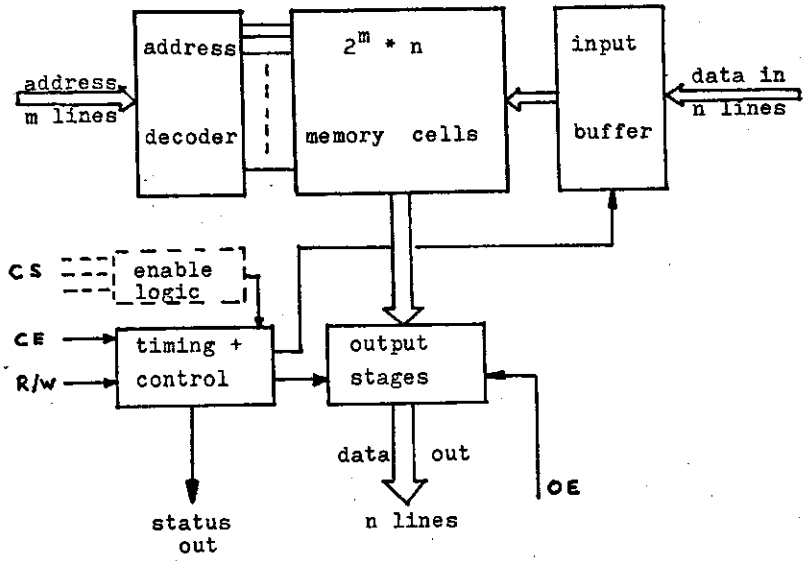


Fig. 2.2: Dynamic Memory Cells



Variations:

- bidirectionel data bus
- CS-lines activ high or low
- various output stages: -- totem pole
  -- open collector
  -- tristate
  -- TTL compatible MOS

Fig. 2.3: Internal Organisation of a RAM

THIS FIGURE IS NOT YET AVAILABLE

Fig. 2.4: Internal Organisation of a ROM

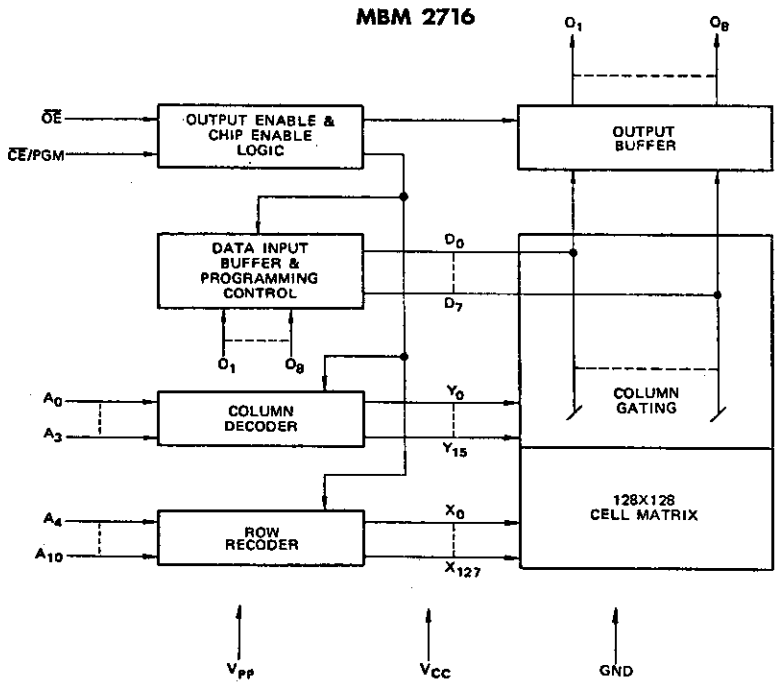
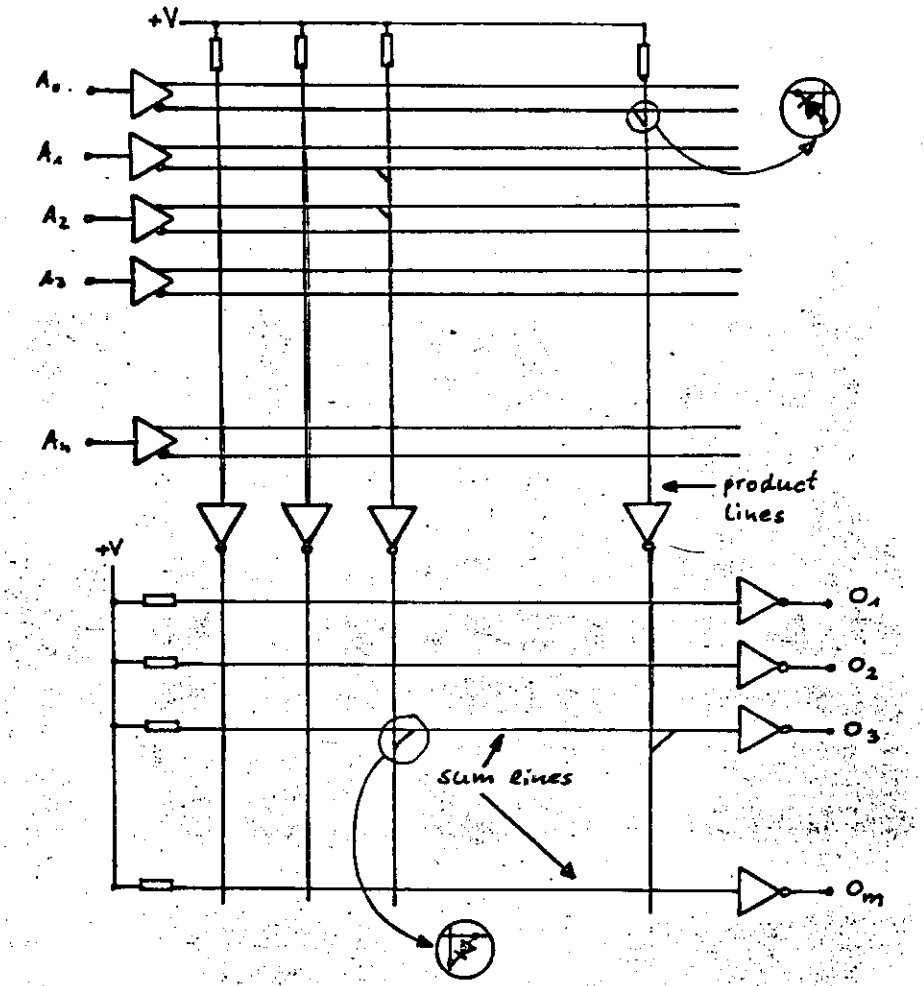


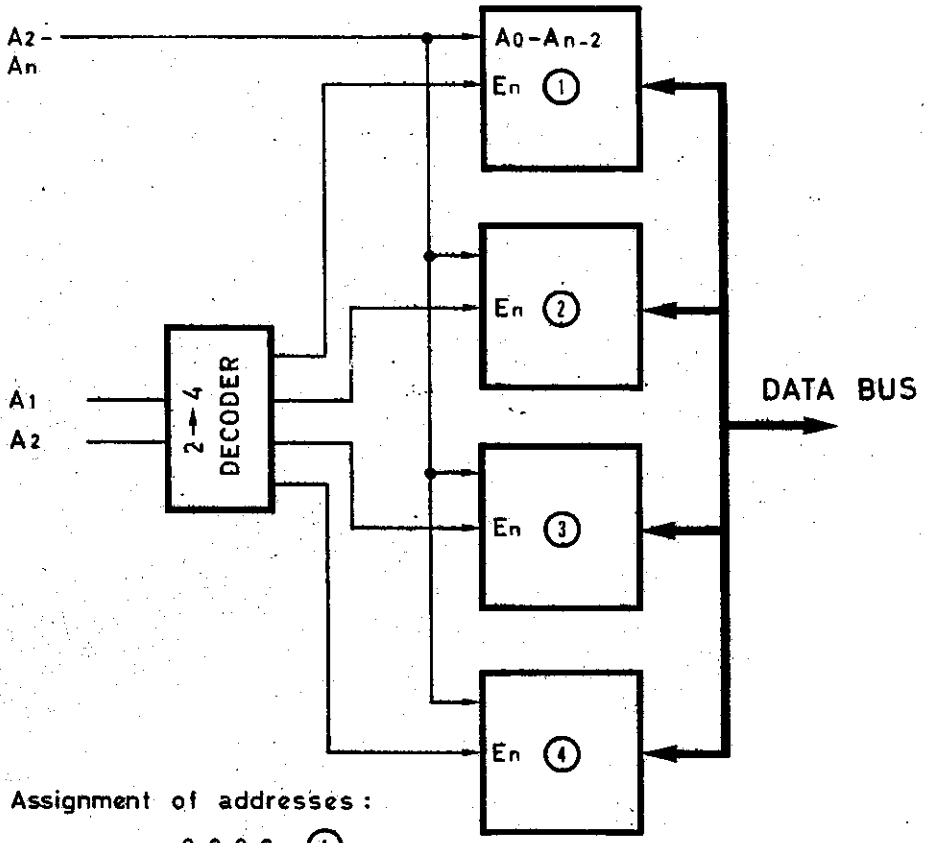
Fig. 2.5: Internal Organisation of an EPROM



Example: FPLA Signetics 82S100
82S101

- 16 input lines
- 48 product lines
- 8 sum lines

Fig. 2.6: Internal Organisation of a PLA



Assignment of addresses :

---	0 0 0 0	(1)
---	0 0 0 1	(2)
	0 0 1 0	(3)
	0 0 1 1	(4)
	0 1 0 0	(1)
	0 1 0 1	(2)
	0 1 1 0	(3)
	0 1 1 1	(4)

Fig. 2.7: Memory Interleaving

A) Static MOS RAMs

Year	1970	1975	1978	1980	1981
Capacity (bits)	256	1024	4096	16384	65536
Technology	P-MOS	N-MOS C-MOS	N-MOS C-MOS	N-MOS C-MOS	C-MOS
Access Time (ns)	≈1000	150-600	150-500	150-300	300
Power/Bit (mW) P-MOS	1,5				
Power/Bit (mW) N-MOS		0,5	0,1	0,03	
Power/Bit (mW) C-MOS		0,1	0,03	0,01	0,004

B) Dynamic MOS RAMs

Year	1970	1975	1978	1980	1981
Capacity (bits)	1024	4096	16384	65536	65536
Technology	P-MOS	N-MOS	N-MOS	N-MOS	N-MOS
Access Time (ns)	300-400	200-350	150-300	200	100
Power/Bit (mW)	0,4	0,1	0,03	0,006	0,005

Fig. 2.8: Evolution of RAM Memories (MOS)

Year	1972	1975	1977	1978	1980
Circuit	1702	2708	2716	2732	2764
Technology	P-MOS	N-MOS	N-MOS	N-MOS	N-MOS
Organisation	256x8	1024x8	2048x8	4096x8	8192x8
Access Time (ns)	650	450	450	450	450
Power (mW/bit)	0,4	0,1	0,04	0,02	0,007
Stand-by (mW/bit)	-	-	0,006	0,001	0,001
V Program (V)	+12,-35, -48	+26,+5, +12,-5	+25,+5	+25,+5	+25,+5
T Program (sec/word)	0,4	0,1	0,05	0,05	0,05
V Read (V)	+5,-9	+5,+12, -5	+5	+5	+5
Erase Time (minutes)	10-20	10-30	10-30	30	20-30

Fig. 2.9: Evolution of EPROM Memories

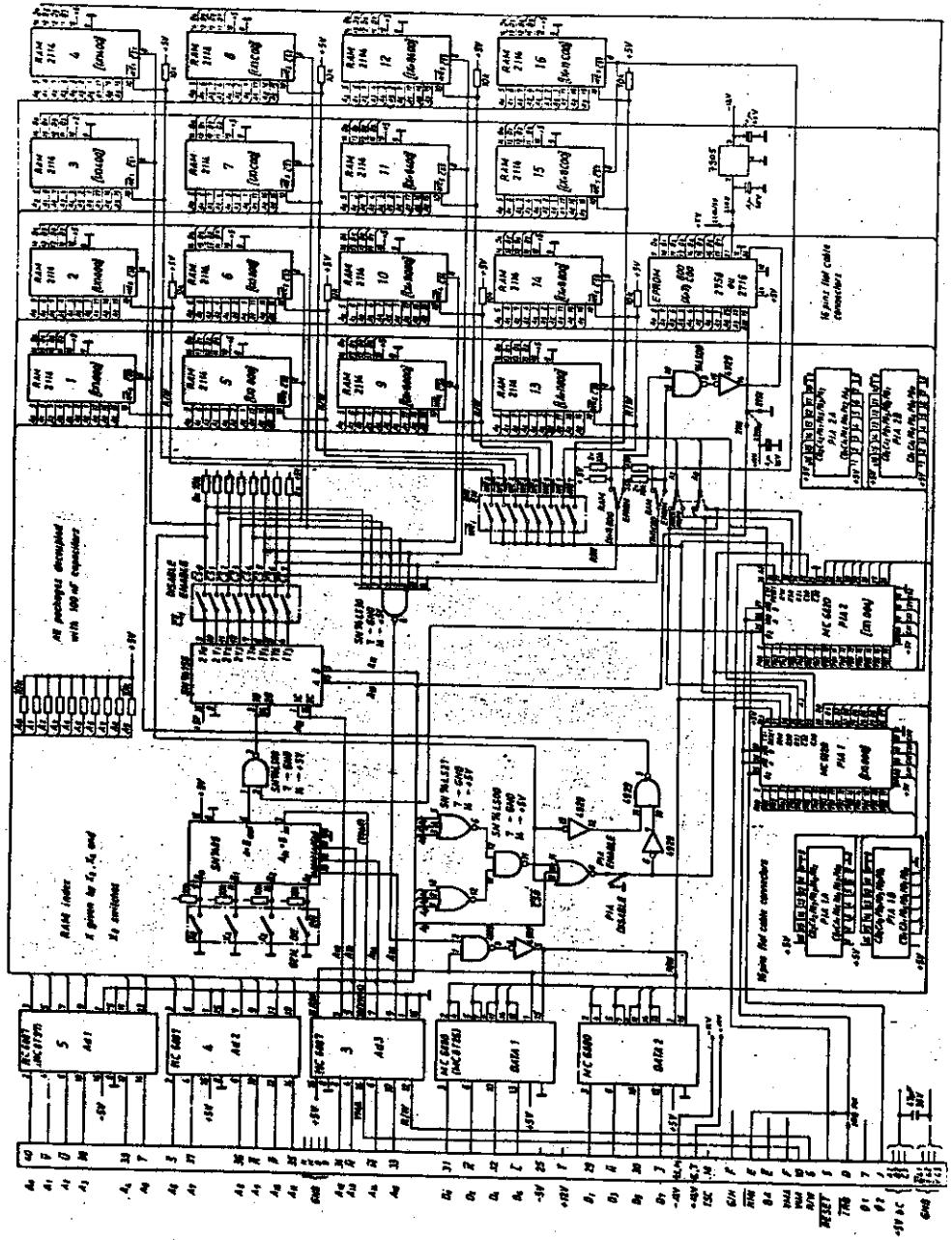


Fig. 2.10: Example of a Memory Extension Board

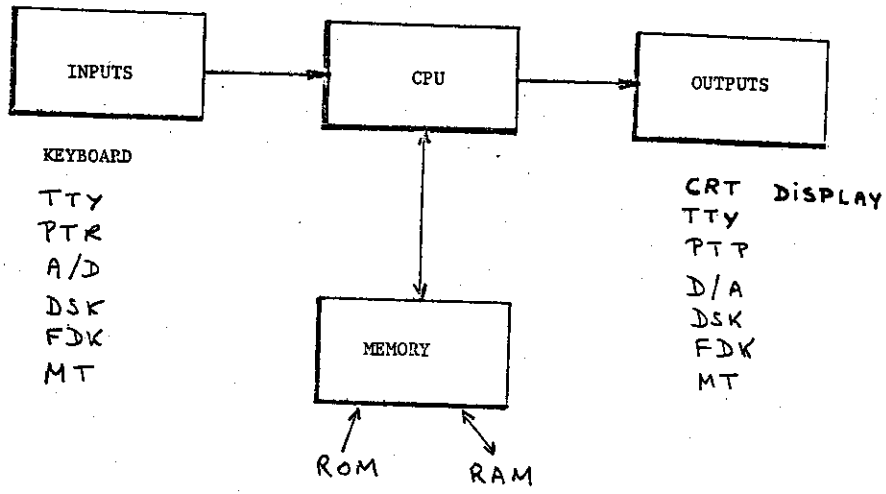
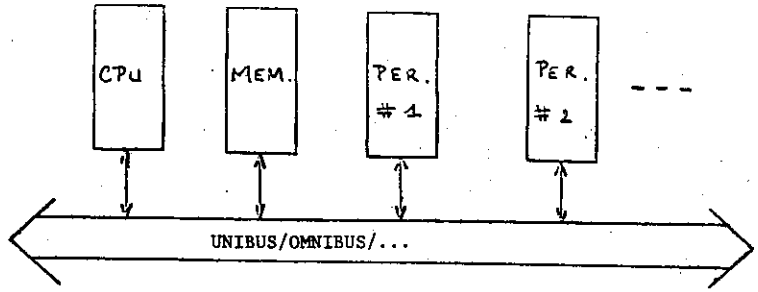
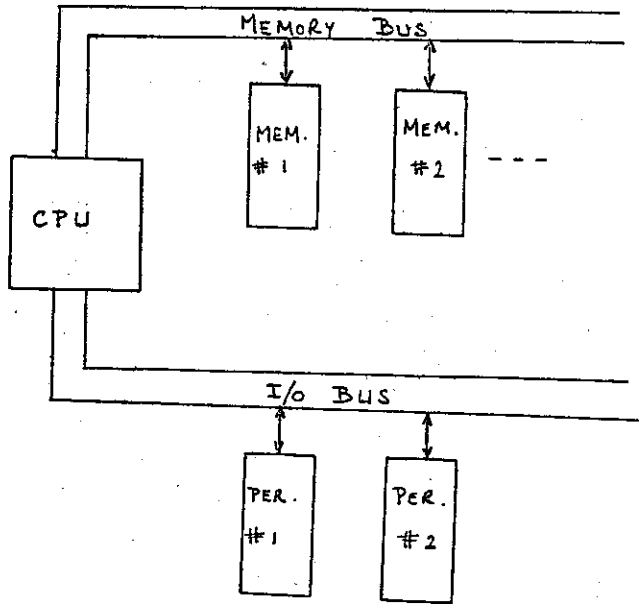


Fig. 3.1: Functional Diagram of a Computer



A) Single-Bus Structure

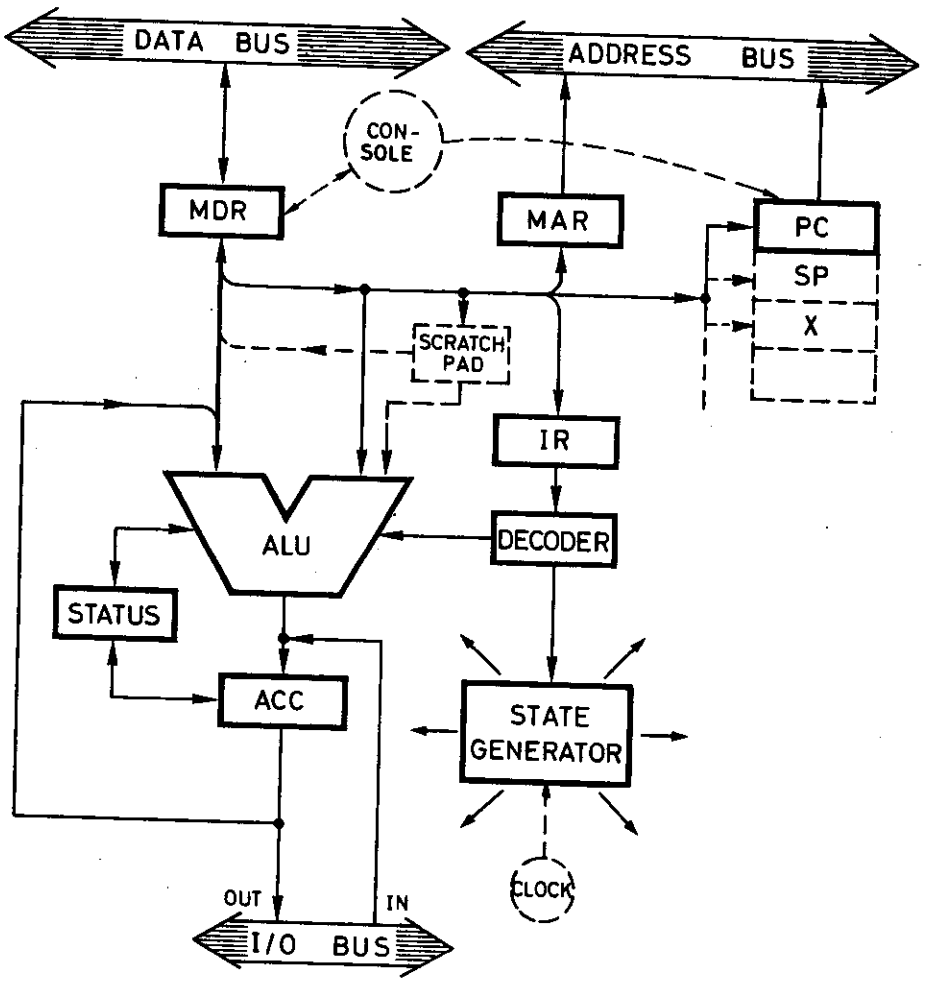
ex: PDP-11, Micro-Processors, ...



B) Double-Bus Structure

ex: HP 2100

Fig. 3.2: Different Bus Structures



ACC	ACCumulator
ALU	Arithmetic and Logic Unit
IR	Instruction Register
MAR	Memory Address Register
MDR	Memory Data Register
PC	Program Counter
SP	Stack Pointer
X	X register

Fig. 3.3: Typical CPU Architecture

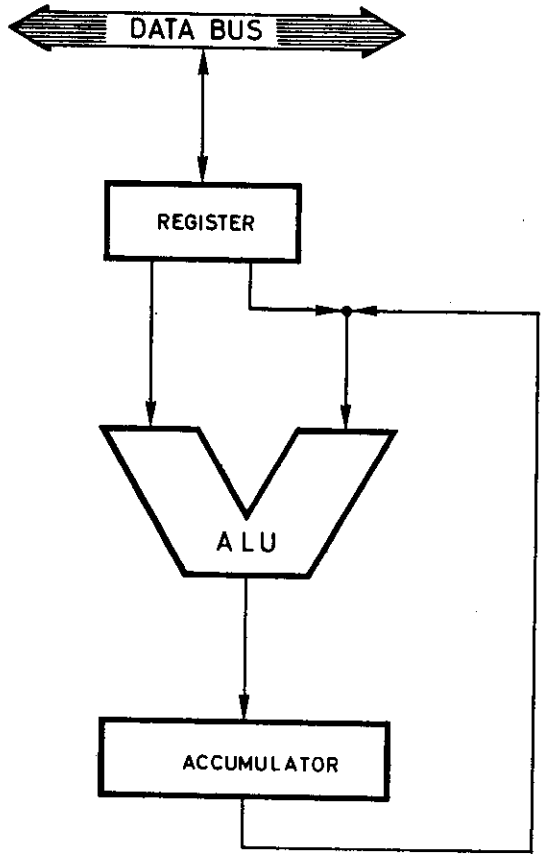
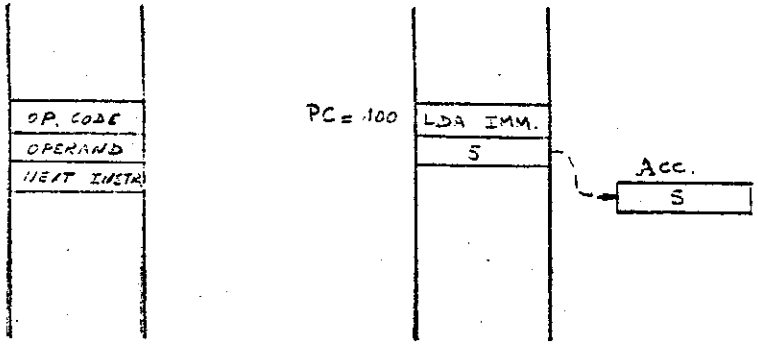
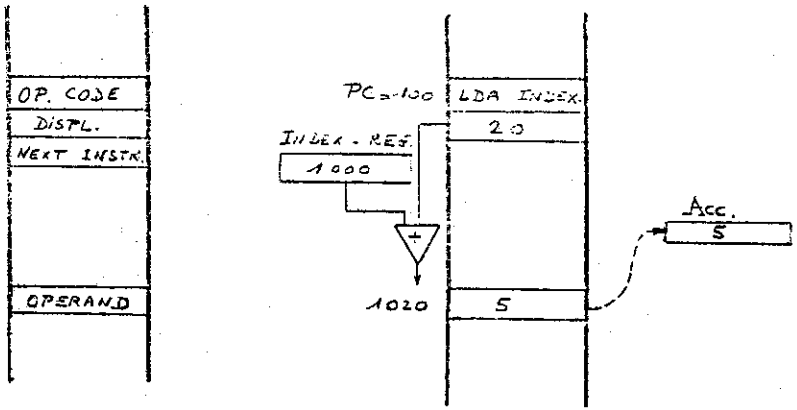


Fig. 3.4: Functional Diagram of an ALU



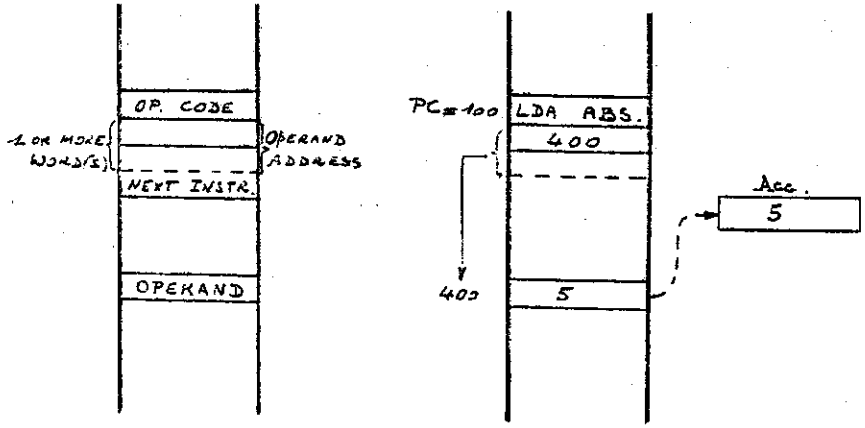
Effective Address: EA = PC + 1

Fig. 3.5: Immediate Addressing Mode



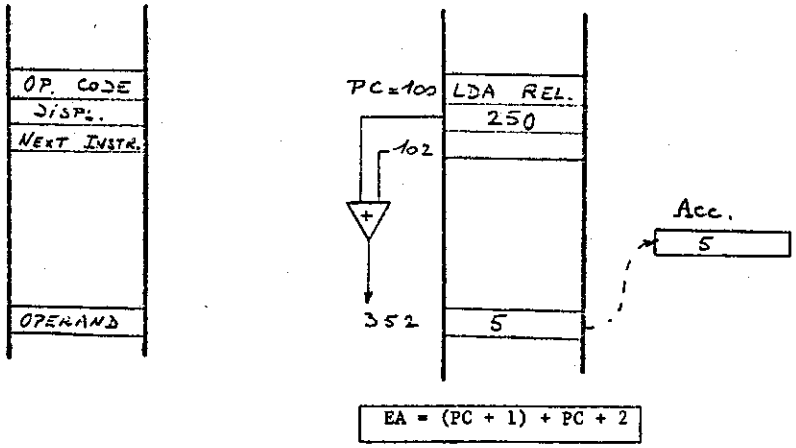
EA = (Index) + (PC +1)

Fig. 3.7: Indexed Addressing Mode



EA = (PC + 1)

Fig. 3.6: Absolute Addressing Mode



EA = (PC + 1) + PC + 2

Fig. 3.8: Relative Addressing Mode

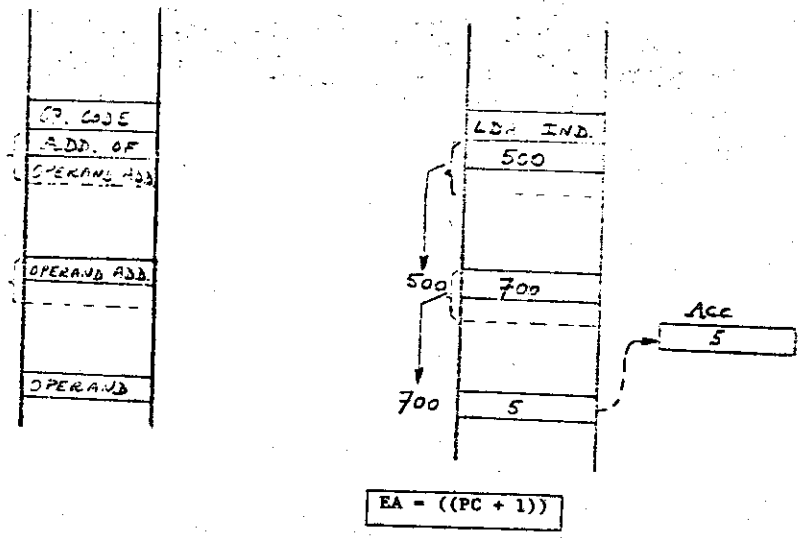


Fig. 3.9: Indirect Addressing Mode

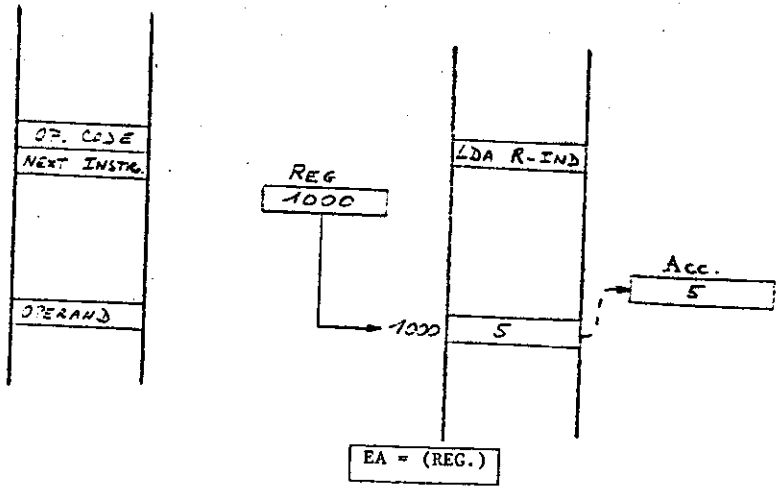


Fig. 3.10: Register Indirect Addressing Mode

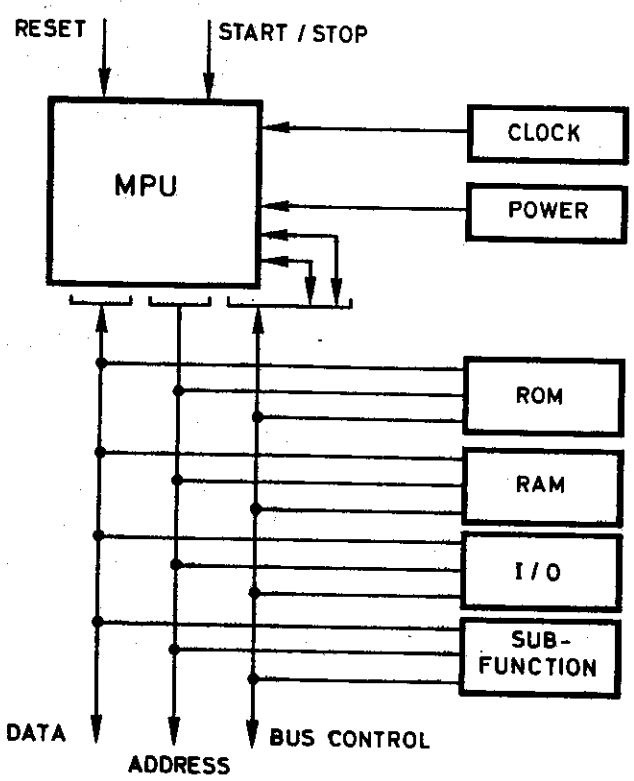


Fig. 3.11: Functional Diagram of a Microcomputer

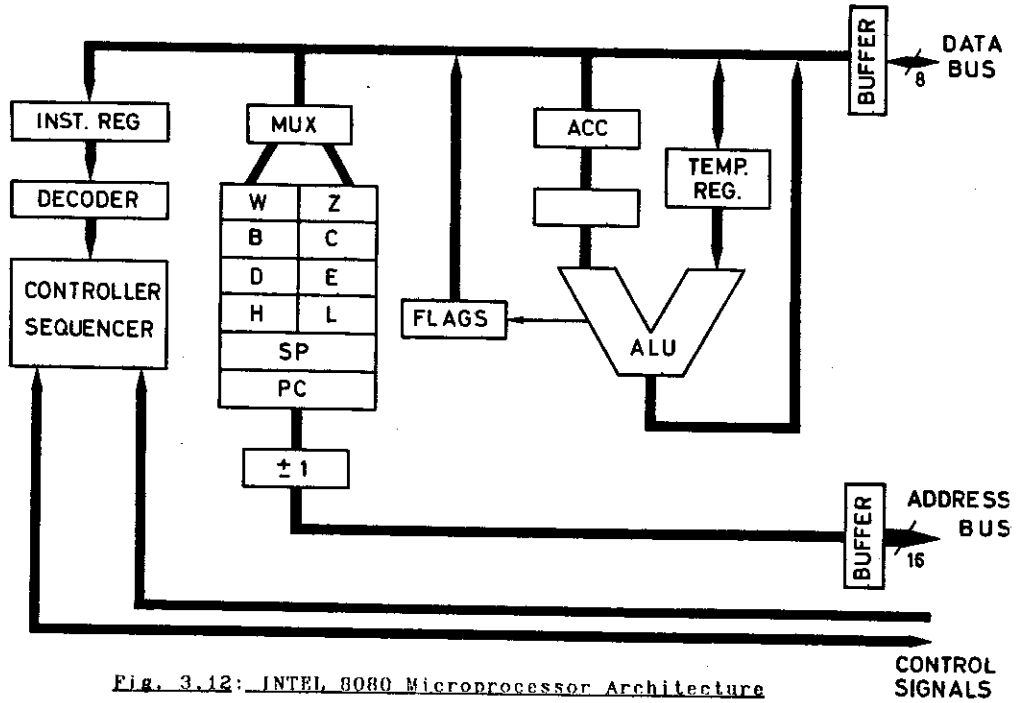


Fig. 3.12: INTEL 8080 Microprocessor Architecture

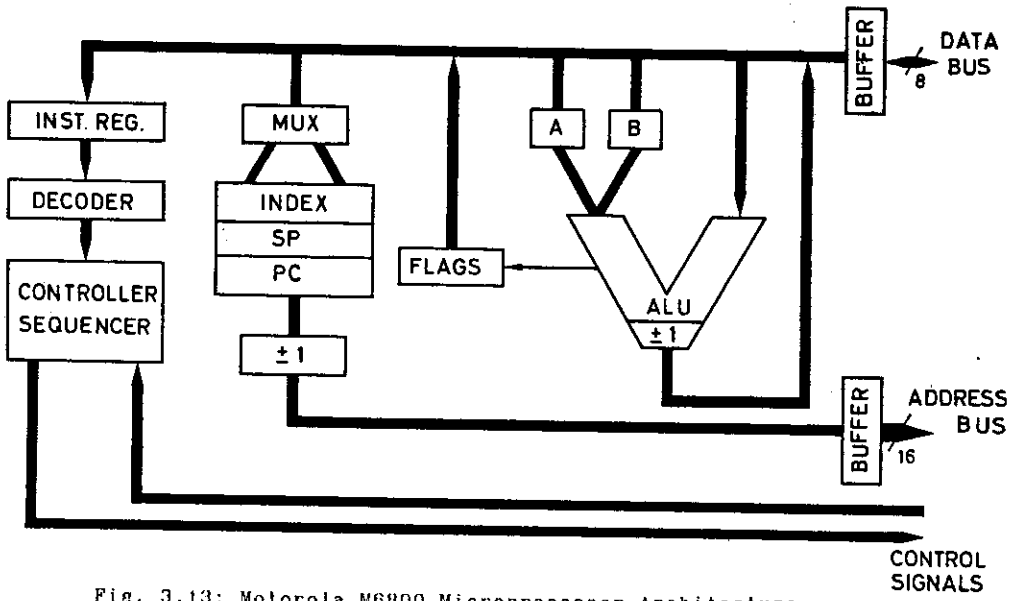


Fig. 3.13: Motorola M6800 Microprocessor Architecture

	INTEL 8080 (1975)	MOTOROLA M6800 (1976)
Accumulators	1	2
8-Bit Auxiliary Registers	6	0
Index Register	0	1
Clock Frequency (MHz)	2	1
Average Execution Speed (µs/instruction)	2	2
Power Supplies (V)	+5,-5,+12	+5
Second Sources	NS,TI,NEC, AMD, MITSUBISHI,...	AMI, SESCOSEM,...

Fig. 3.14: Comparison Table INTEL 8080 / MOTOROLA M6800

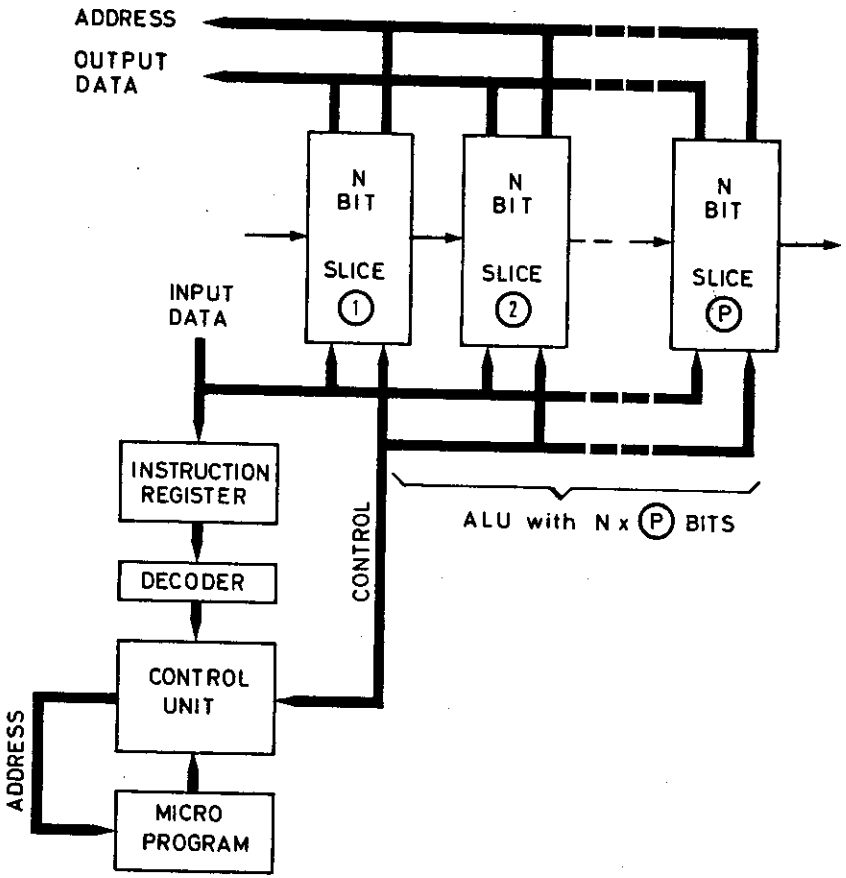


Fig. 3.15: Architecture of a Bit-Slice System

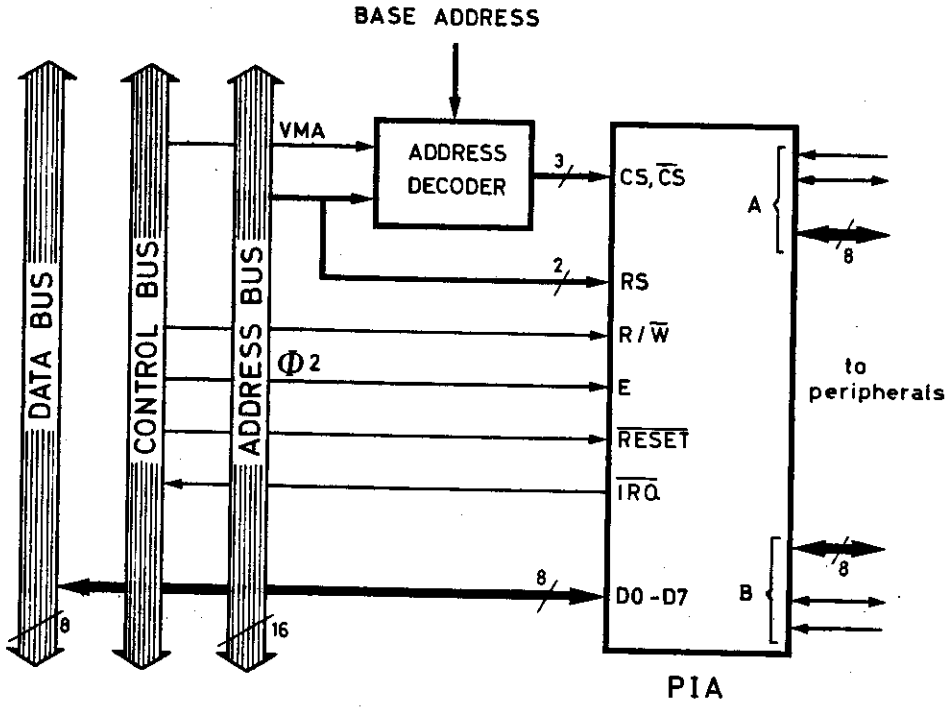


Fig. 4.1: PIA Typical Interconnection

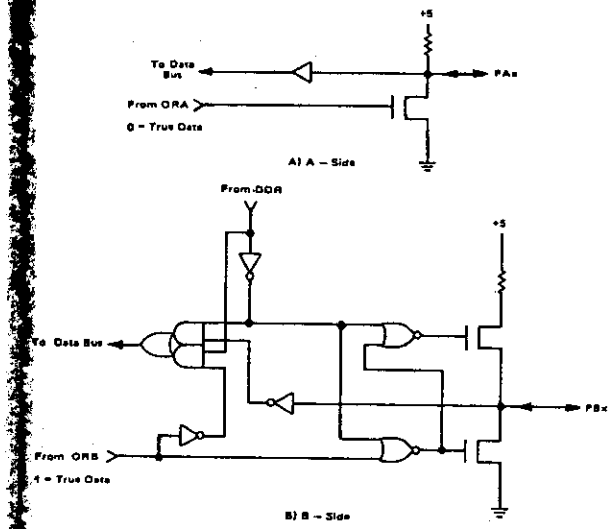


Fig. 4.2: PIA Output circuits

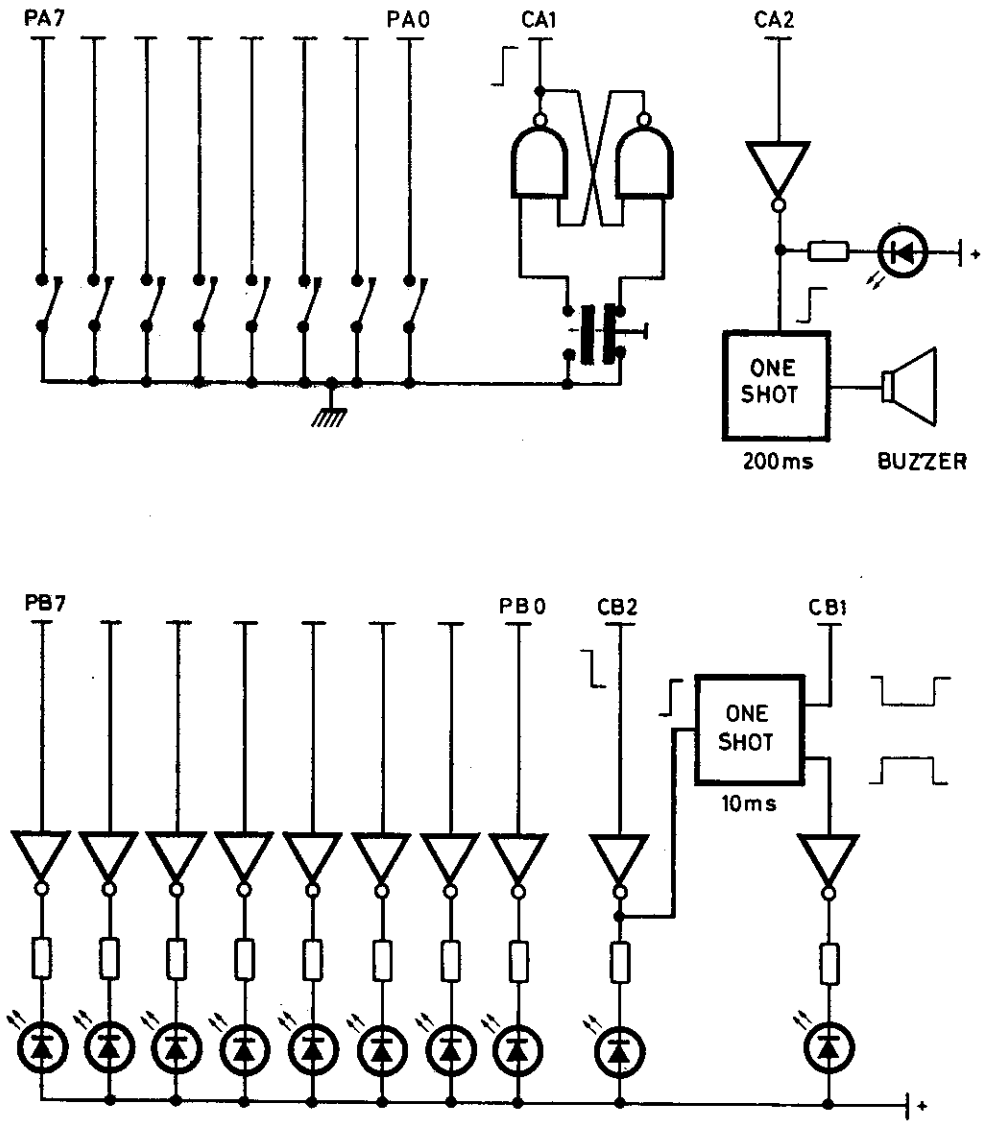
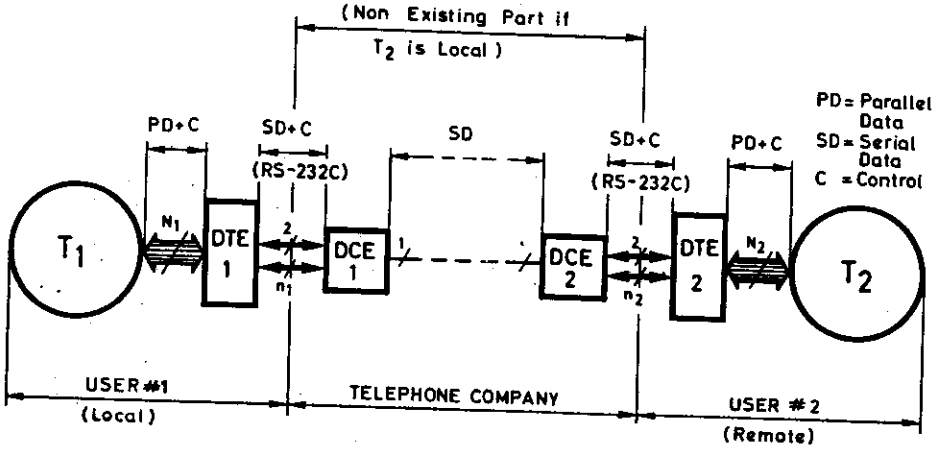


Fig. 4.3: PIA-MINI-I/O Circuit Diagram



T_1, T_2 User Terminal Station
(Console, Computer, ...)

DTE Data Terminal Equipment
(Serial Interface between Terminal and Modem)

DCE Data Communication Equipment
(Modem)

Fig. 4.4: Serial Data Communication System

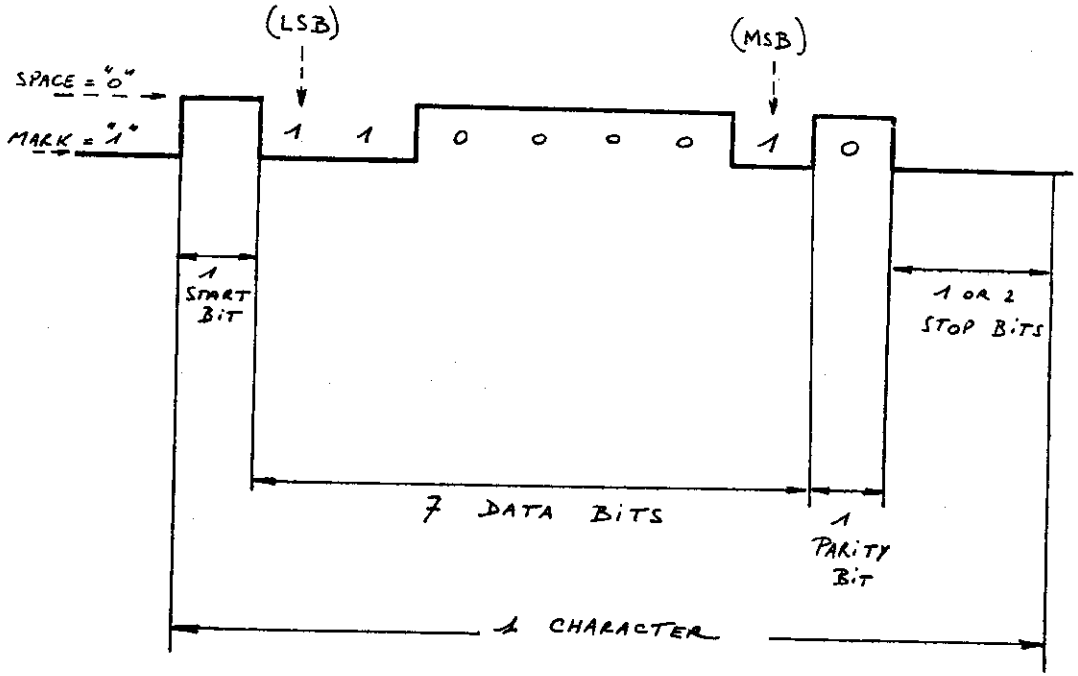


Fig. 4.5: Asynchronous Transmission of Character "C"

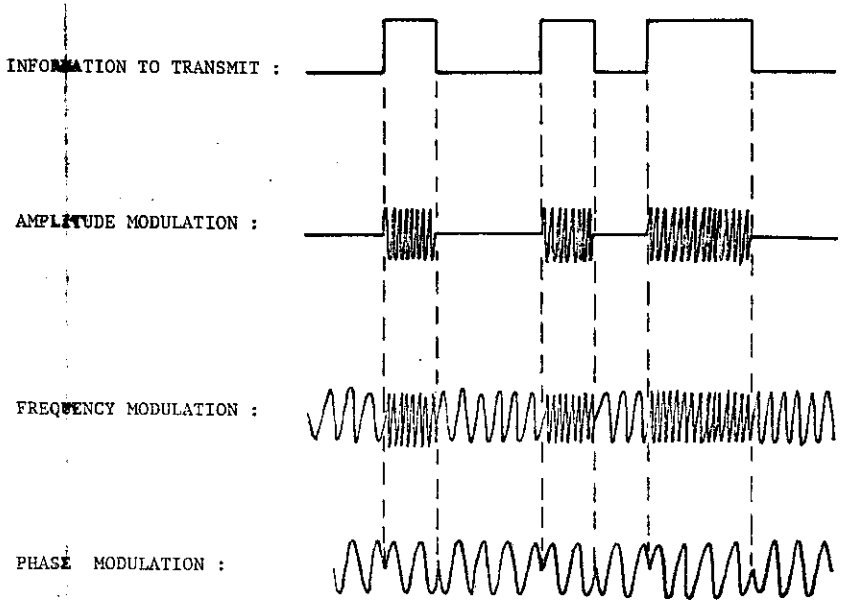


Fig. 4.6: Some Modulation Techniques

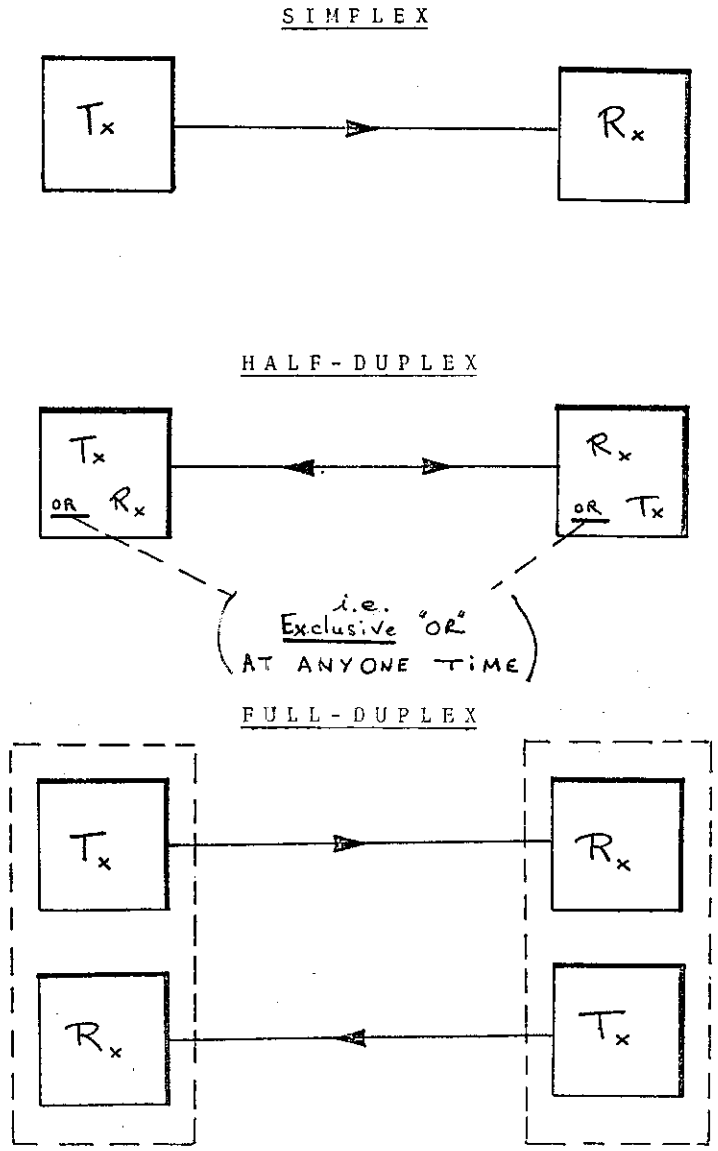


Fig. 4.7: Serial Transmission Techniques

RS-232-C Interface Circuit Functions

Pin 1. PROTECTIVE GROUND. Electrical equipment frame and ac power ground.

Pin 2. TRANSMITTED DATA. Data originated by the terminal to be transmitted via the sending modem.

Pin 3. RECEIVED DATA. Data from the receiving modem in response to analog signals transmitted from the sending modem.

Pin 4. REQUEST TO SEND (RTS). Indicates to the sending modem that the terminal is ready to transmit data.

Pin 5. CLEAR TO SEND (CTS). Indicates to the terminal that its modem is ready to transmit data.

Pin 6. DATA SET READY (DSR). Indicates to terminal that its modem is not in a test mode and modem power is ON.

Pin 7. SIGNAL GROUND. Establishes common reference between modem and terminal.

Pin 8. RECEIVED LINE SIGNAL DETECTOR (LSD). Indicates to the terminal that its modem is receiving carrier signals from the sending modem.

Pin 9. Reserved for test.

Pin 10. Reserved for test.

Pin 11. Unassigned.

Pin 12. SECONDARY RECEIVED LINE SIGNAL DETECTOR. Indicates to the terminal that its modem is receiving secondary carrier signals from the sending modem.

Pin 13. SECONDARY CLEAR TO SEND. Indicates to the terminal that its modem is ready to transmit signals via the secondary channel.

Pin 14. SECONDARY TRANSMITTED DATA. Data from the terminal to be transmitted by the sending modem's channel.

Pin 15. TRANSMITTER SIGNAL ELEMENT TIMING. Signal from the modem to the transmitting terminal to provide signal-element timing information.

Pin 16. SECONDARY RECEIVED DATA. Data from the modem's secondary channel in response to analog signals transmitted from the sending modem.

Pin 17. RECEIVER SIGNAL ELEMENT TIMING. Signal to the receiving terminal to provide signal-element timing information.

Pin 18. Unassigned.

Pin 19. SECONDARY REQUEST TO SEND. Indicates to the modem that the sending terminal is ready to transmit data via the secondary channel.

Pin 20. DATA TERMINAL READY (DTR). Indicates to the modem that the associated terminal is ready to receive and transmit data.

Pin 21. SIGNAL QUALITY DETECTOR. Signal from the modem telling whether a defined error rate in the received data has been exceeded.

Pin 22. RING INDICATOR (RI). Signal from the modem indicating that a ringing signal is being received over the line.

Pin 23. DATA SIGNAL RATE SELECTOR. Selects one of two signaling rates in modems having two rates.

Pin 24. TRANSMIT SIGNAL ELEMENT TIMING. Transmit clock provided by the terminal.

Pin 25. Unassigned.

Fig. 4.8: RS-232 Functions

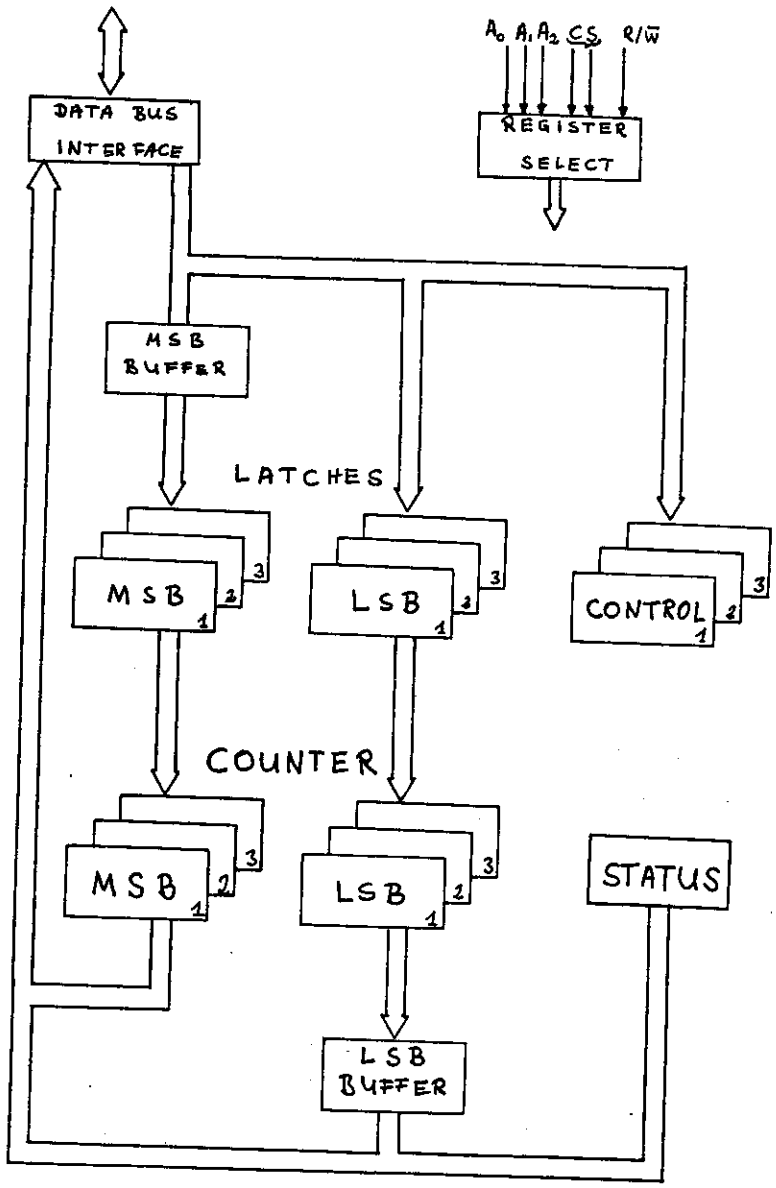
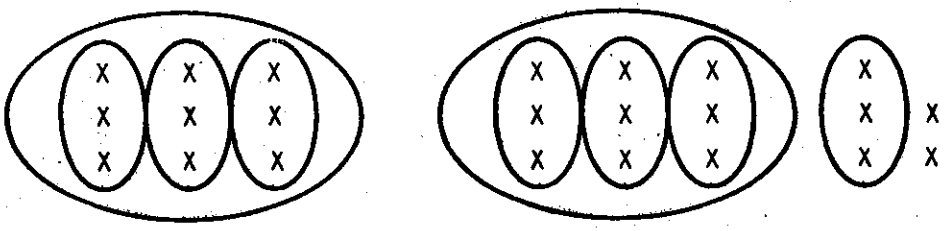


Fig. 4.9: MC6840 Programmable Timer Block Diagram



$(23)_{10} = (212)_3$

Fig. 6.1: Example of the Grouping Method in Base 3

PROGRAM: MEMORY DATA TEST | AUTHOR: JPV + WVR | DATE: AUG 81 | PAGE: 1/4

ADDR	CODE BYTE 1	CODE BYTE 2	CODE BYTE 3	LABEL	INSTR	OPERAND	COMMENT
ØØØØ				FIRST	RMB	2	ADDRESS OF FIRST MEMORY LOCATION
ØØØ2				LAST	RMB	2	ADDRESS OF LAST MEMORY LOCATION
ØØ4Ø				START			
ØØ1Ø	DE	Ø4			LDX	FIRST	GET POINTER TO FIRST LOCATION
ØØ12	4F				CLR A		SETUP FIRST DATA PATTERN
ØØ13	Ø9				DEX		TO INCLUDE FIRST AND LAST LOCATION
ØØ14				LOOP			
ØØ14	Ø8				INX		POINT TO NEXT LOCATION
ØØ15	A7	ØØ			STA A	Ø,X	WRITE DATA
ØØ17	E6	ØØ			LDA B	Ø,X	READ DATA BACK
ØØ19	11				CBA		IF (A) ≠ (B) THEN STOP
ØØ1A	26	Ø4			BNE	STOP	
ØØ1C	3C	Ø2			CPX	LAST	ELSE IF LOCATION ≠ LAST DO NEXT
ØØ1E	26	F4			BNE	LOOP	
				STOP			RETURN TO DSBUG + DISPLAY RESULT
ØØ2Ø	3F				SWI		
							RESULT : (X) = (LAST) : OK
							: (X) ≠ (LAST): (X) ≙ LOCATION
							(A), (B) ≙ GOOD, BAD DATA.

Fig.7.1: Hand-Coded Program Example

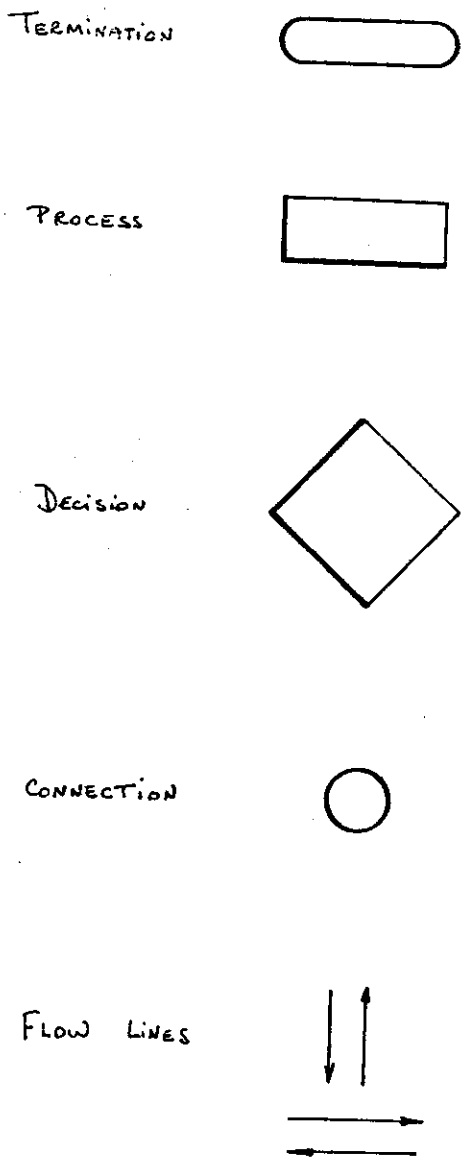


Fig. 7.2: Flowchart Basic Symbols

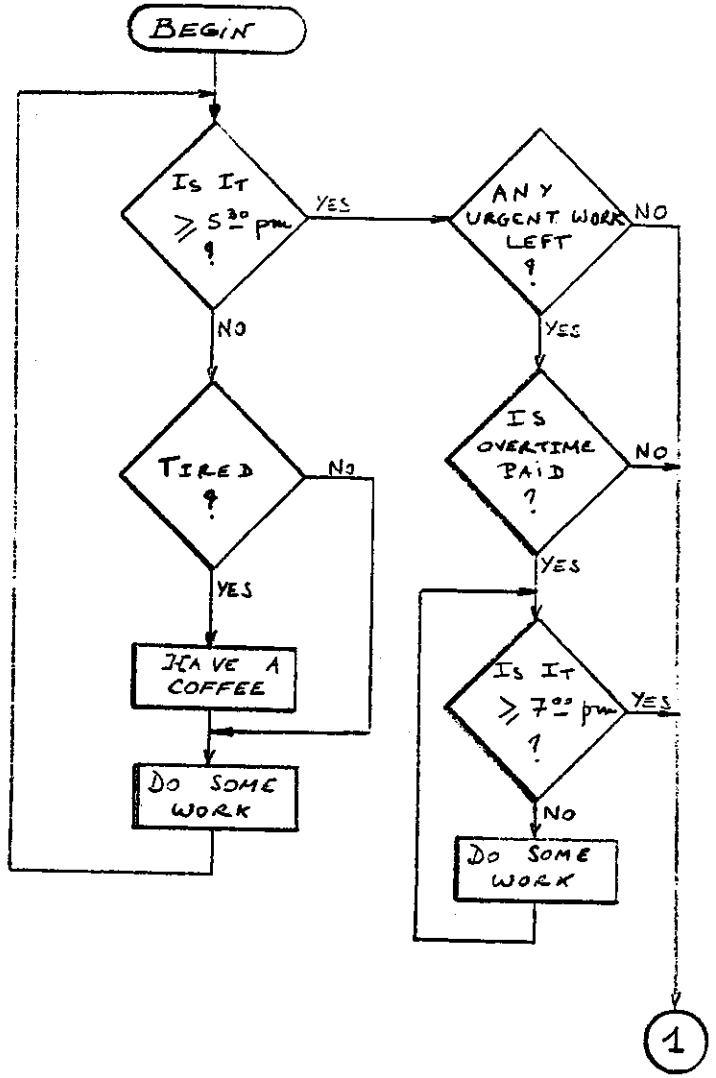


Fig. 7.3: A Flowchart Example: "Going Home from Work"

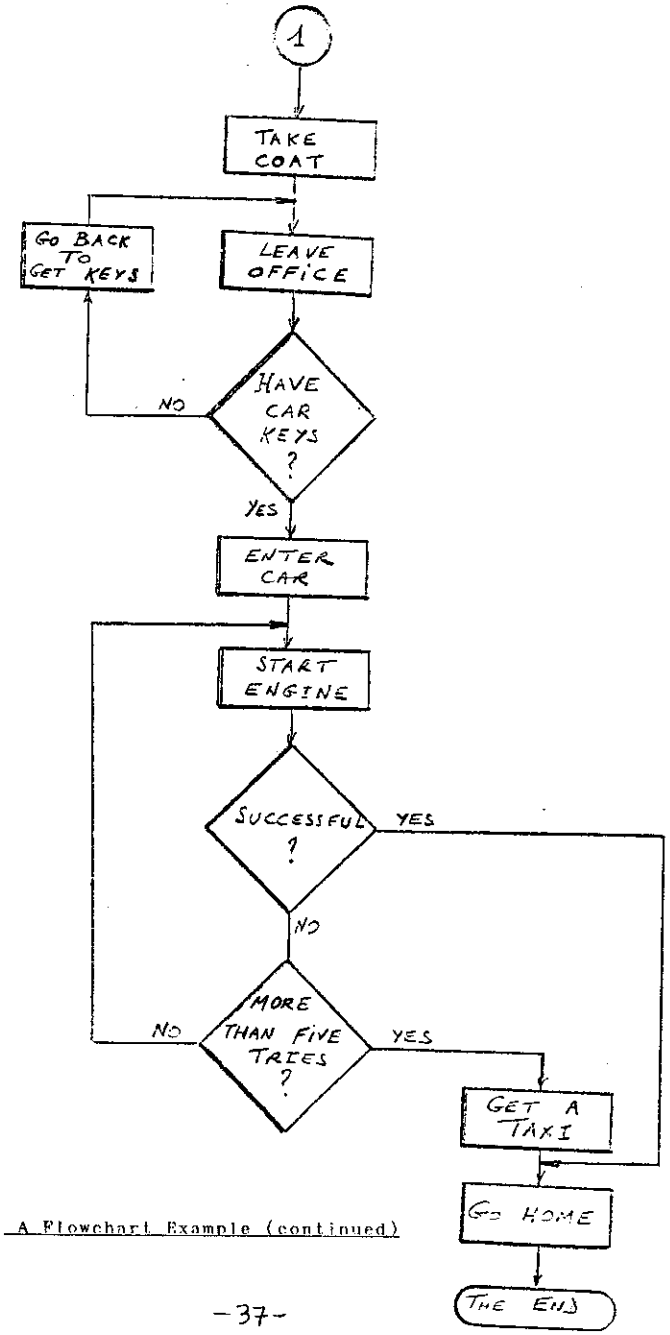
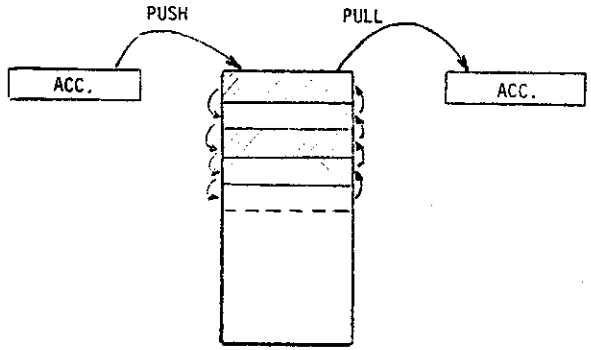


Fig. 7.3: A Flowchart Example (continued)

PRINCIPLE:



ADDRESSING MECHANISMS: the two possibilities

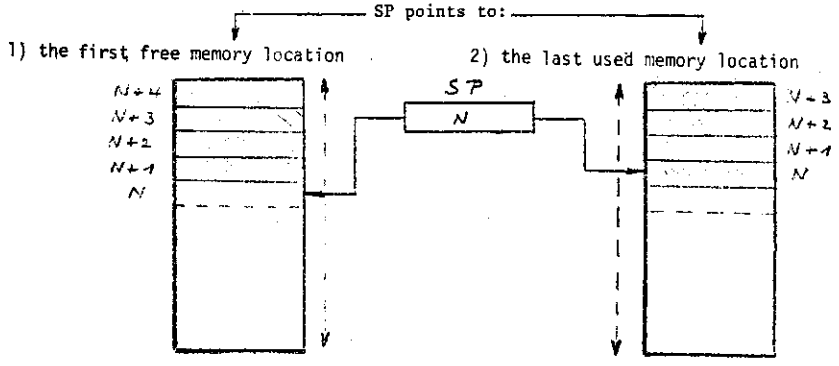
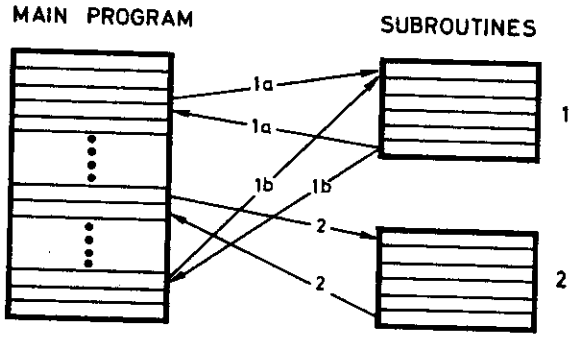


Fig. 7.4: The Stack

GENERAL :



M6800 :

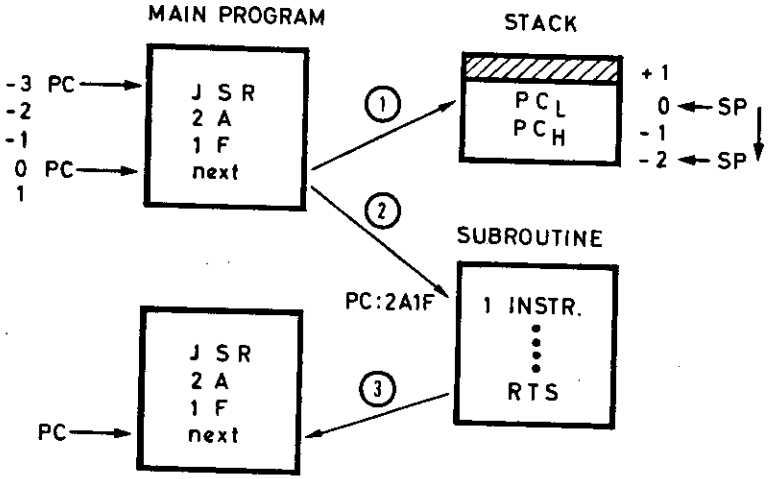


Fig. 7.5: Subroutines

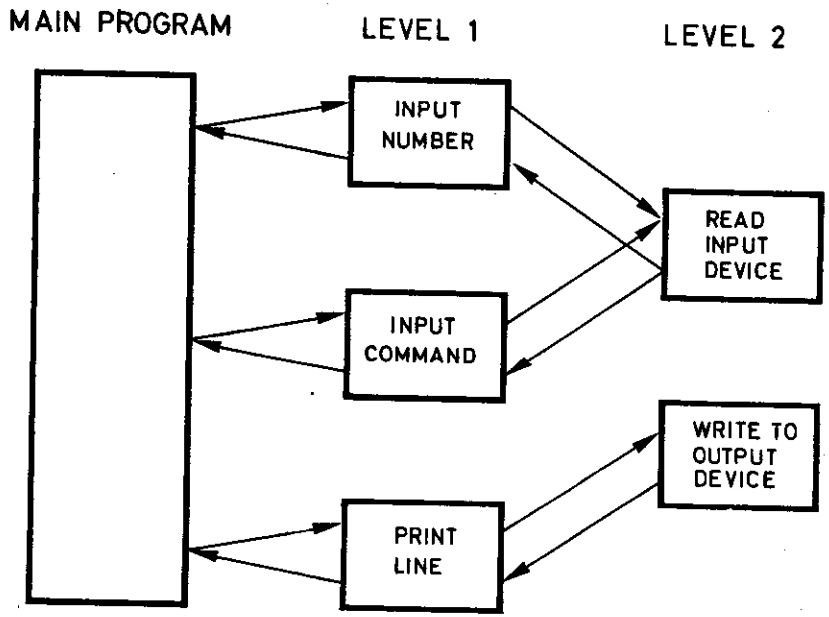


Fig. 7.6: Nested Subroutines