UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION
INTERNATIONAL ATOMIC ENERGY AGENCY
INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS

SMR/917 - 29

SECOND WORKSHOP ON SCIENCE AND TECHNOLOGY OF THIN FILMS

(11 - 29 March 1996)

" Large area Si devices: polycristalline silicon "

presented by:

F. PLAIS
Laboratoire Central de Recherches
Thomson C.S.F.
Domaine de Corbeville
91404 Orsay Cedex
France

These are preliminary lecture notes, intended only for distribution to participants.

LARGE AREA Si DEVICES : POLYCRISTALLINE SILICON

part 1 : etching

part 2 :deposition

part 3 :poly-Si TFTs

Trieste - ICTP- 26-27 / 3 / 96

by

François PLAIS

Thomson CSF LCR

Domaine de Corbeville

91404 ORSAY CEDEX

FRANCE

Etching : summary

introduction

lithography

etching tools

issues
(etch rate, selectivity
slope profile, uniformity
device damage)

endpoint detection (in-situ control)

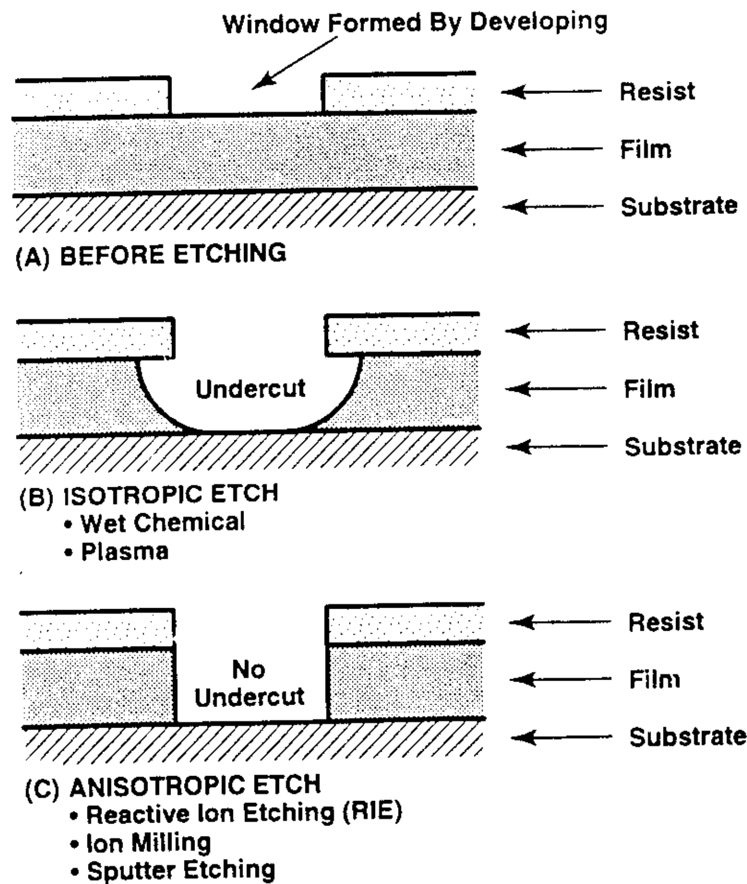
near-field microscopy for
profile/height control (in-line)

etch : the process of removing material (Si, SiO_2... thin films) by wet or dry etching techniques.

isotropic etch : proceeds laterally and vertically at the same time (and rate). wet etch is usually isotropic.

anisotropic etch : lateral etch rate very low. dry etch is usually anisotropic.

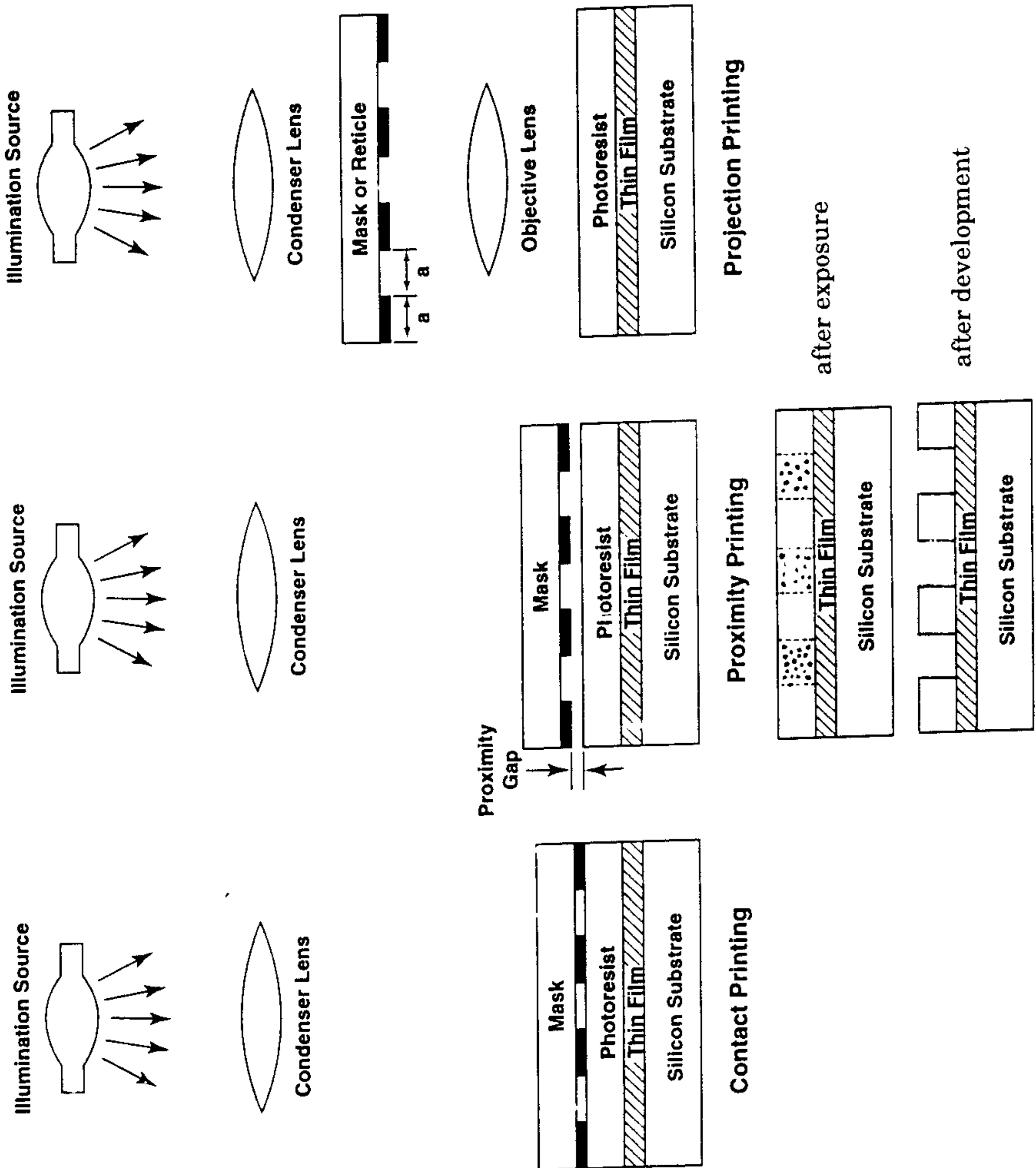
over-etch time : extra time required to complete the etch all over the substrate. not zero if etching tool not uniform or film thickness not uniform.



	wet etch (*)	dry (plasma) etch	
		RIE	HDP (**)
Uniformity	good (poor if incubation time)	reactor dependent	reactor dependent
Etch rate	high (undiluted)	high	high (or very)
Selectivity	can be infinite	controlled	controlled (better)
Slope profile	undercut	controlled (***)	controlled (***)
Device damage			
radiations	none	-	
Contaminations	can be high	from the walls	reduced

(*) not useful for polycristalline films (grain boundaries preferential etch)
(**) High Density Plasma (low pressure) for ICP, ECR ...
(***) even on double layer (see example of Ti-Mo)

etch rate	*affect*	throughput		
uniformity	*affect*	over-etch time	*which affect*	throughput
selectivity	*affect*			
slope control	*affect*	step coverage	*which affect*	yield
device damage	*affect*	yield		


Illumination Source
Condenser Lens
Mask or Reticle
a
a
Objective Lens
Photoresist
Thin Film
Silicon Substrate
Projection Printing
after exposure
after development
Illumination Source
Condenser Lens
Mask
Photoresist
Thin Film
Silicon Substrate
Proximity Printing
Proximity Gap
Thin Film
Silicon Substrate
Thin Film
Silicon Substrate
Illumination Source
Condenser Lens
Mask
Photoresist
Thin Film
Silicon Substrate
Contact Printing

trends towards

high density (high etch rate)

low pressure (anisotropy)

plasmas (reproducibility)

allowing

independent control of ion energies (selectivity)

trends towards

single wafer etching reactor with in-situ control

to

improve the yield

(driven by requirements of sub 0,5 µm Si technologies)

etching (film thickness > 50 nm) or cleaning (etching of very thin films)

<u>cleaning</u>

removal of adsorbed chemical species from the surface which can affect the process (surface adhesion) or the final device characteristics (interface states).

removal of particles : the lower the particle, the larger the adhesion force.
- dissolution in oxidizing agent or
- electrical repulsion in alkaline solution (with ultrasonic waves),
combined with mechanical treatment (brush)

<u>etching</u>

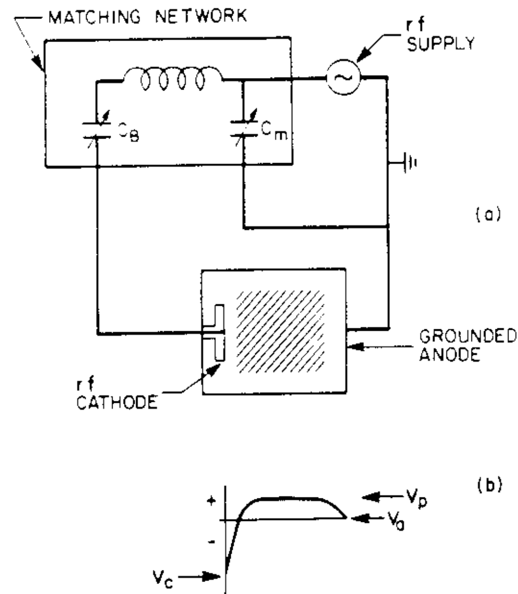
less ans less used in large electronics

some examples :

Al or Cr etch because of
- very good selectivities towards SiO_2 and resist
- tapered edges
- high cost of dry etch system (for Al)

transparent electrodes (ITO)

the most commonly used technique



Schematic representation of an rf RIE plasma

experimental considerations give $V_c / V_a = (A_a / A_c)$

problem → V_c which determines selectivity is not independent from the power which determines the etch rate

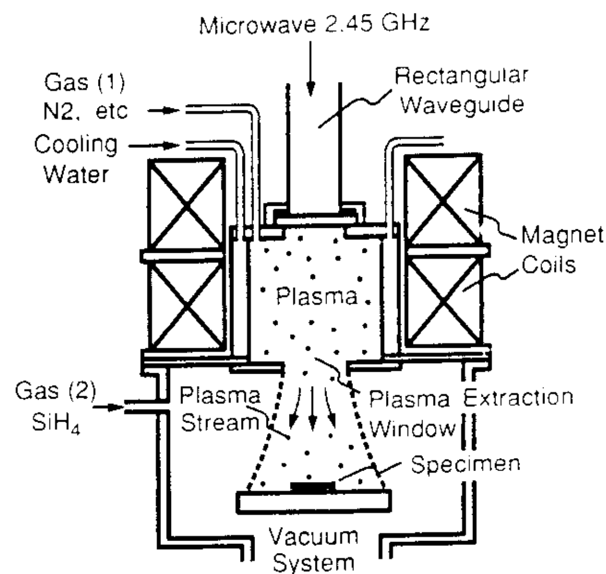
This kind of reactors already exist for the etching on large substrates

free electron in an electromagnetic field : Lorentz force
F = e **v** ^ **B**
result in an helicoidal trajectory

ECR for Electron Cyclotron Resonance

obtained under the following conditions :
- presence of a microwave electrical field (E) at 2.45 GHz
- presence of a static magnetic field (B) with an amplitude of 875 G
and perpendicular to E
→frequency of rotation around **B** is equal to frequency of **E** : electrons gain energy at each period until collision lead to energy transfer by dissociation, ionisation...

ECR introduced in Japan in the early 80's (NTT patent)
commercial systems available from Hitachi for 8" Si wafers

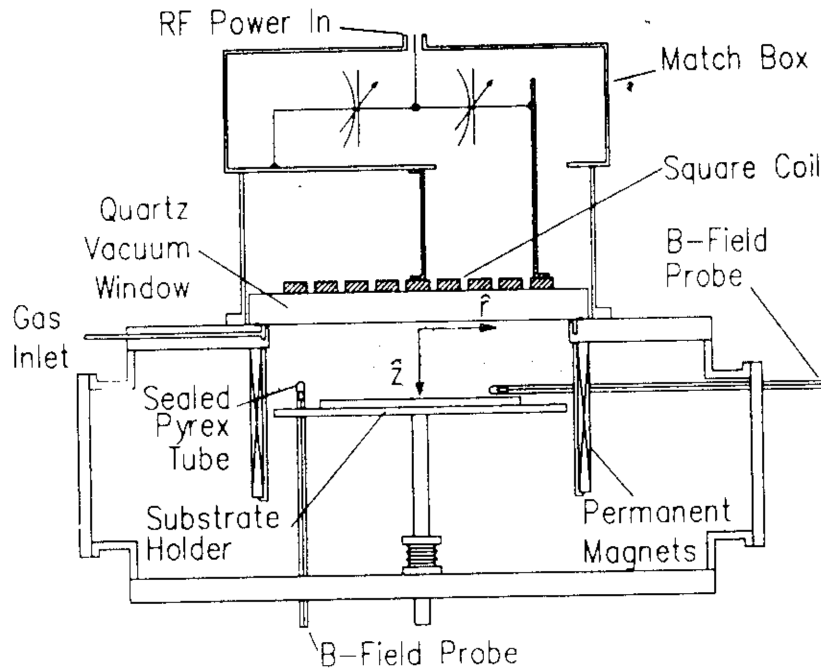


Schematic side view of an ECR type plasma (Matsuo, JJAP 22 (1983) L210)

DECR introduced in France in the mid 80's (CNRS-CNET patent)
D for distributed
developped by Alcatel
main applications in deposition (see part 2)

recent tools (Patents from IBM and Lam Research, 1990)

most widely accepted high density source for etch applications (sub 0.5 μm design rules)
100 Lam systems in the world



side view of an ICP reactor

simple architecture (radio-frequency, antenna outside the vacuum chamber)
independent control of ion energy

<u>plasma characteristics</u>

- large process window : 1 - 10 mTorr
  10^{11} - 10^{12} e^{-} cm^{-2}
- the magnetic field decreases exponentially inside the chamber (cut-off) at P=900W, r = 6 cm, $B_r(z) = B_0 \exp(-z/z_0)$ with B_0 = 2.1 G and z_0 = 2cm (plasma skin depth)
- the electrical field is in the window plane along the direction of the coil, with a maximum of amplitude (at the window) of 200 V/m

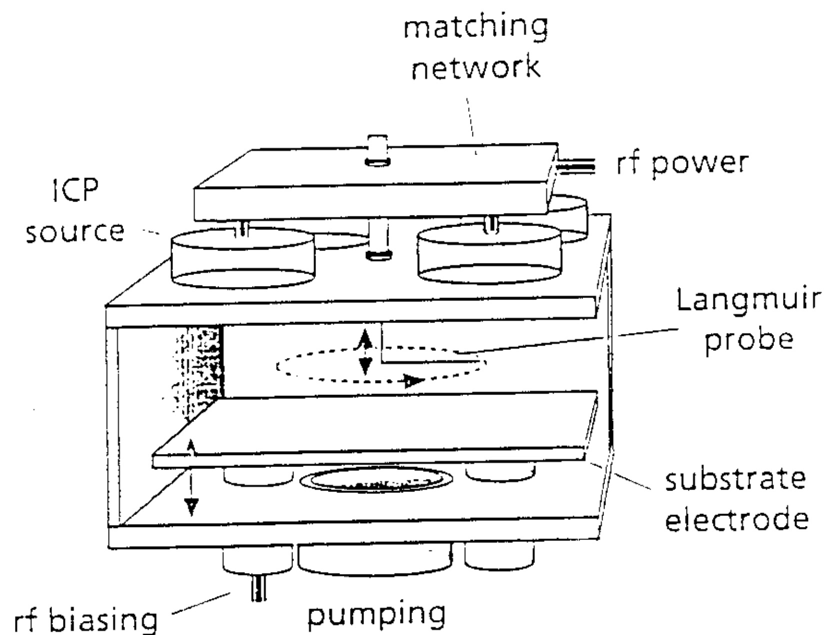
In this kind of electromagnetic field, electrons can gain time average energy without any collisions (different from paralell-plate reactor)

Hopwood, JVST A11 (1993) 147

large area ICP reactors for FPD

- joint program between Lam Research and Xerox for the developpment of a dry etch manufacturing system for FPD

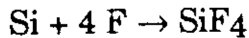
- report of an ICP reactor for treatment of 600 x 400 mm2 substrates

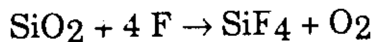


Large area ICP reactor (Heinrich, 8 IVMC '95)

Etching of Si and SiO_2 in $CF_4 + O_2$ discharge

Fluorine atom is the main echant specie through the reactions :


$Si + 4\,F \rightarrow SiF_4$


$SiO_2 + 4\,F \rightarrow SiF_4 + O_2$

F is continuously created by dissociative reactions :

$CF_4 \rightarrow CF_{4-x} + x\,F$

and consumed by :

- etching of material
- recombination with CFx

<u>adding O_2 in the discharge</u>

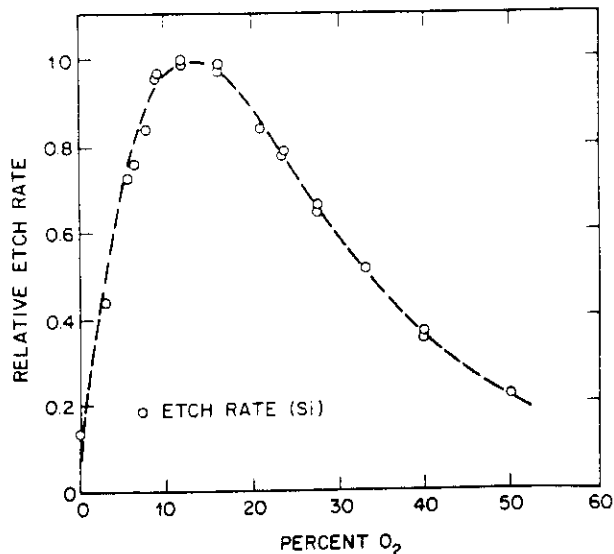
- creates CO, CO_2 and COF_2 species and reduces the recombination of F atoms.

  → increase of etch rate

until, at higher dose

- decreases the mean electron energy
- induce competition between F and O at the active sites on the Si surface

  → decrease of etch rate



Si etching rate is roughly correlated with the evolution of F density.

Mogab, JAP 49 (1978) 3796

<u>SiO_2 contact window opening → high selectivity over Si</u>

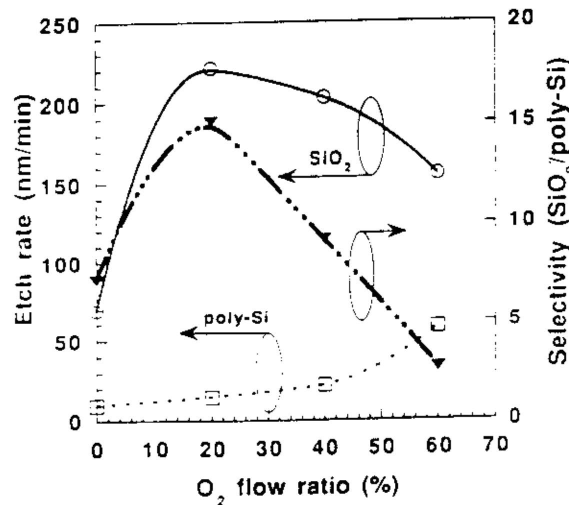
conventionnally accomplished in carbon-rich fluorocarbon discharges
etch selectivity depends on the selective deposition of polymer films on non oxidised surfaces

$C_4F_8 + O_2$, ECR reactor

without rf bias of the substrate, the polymer deposition rate is higher than 200 nm/min even in the presence of O2 (40%).

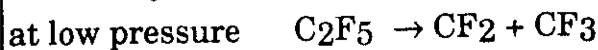
for 40% O_2, the selectivity increases (from 6 to 16) when the pressure decreases (from 4 10^{-3} mbar to 5 10^{-4} mbar).

at a pressure of 1.3 10^{-3} mbar, selectivity and SiO_2 etch rate are maximum for an oxygen percentage of 20 %.

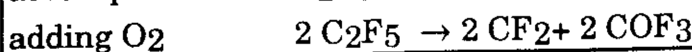


SiO_2 and Si etch rates versus O_2 percentage (MW and RF powers, 1800 and 700 W, 1.3 10^{-4} mbar) (Kimura, JJAP 34 (1995) 2114)

Selectivity is correlated with the concentration of CF_2 in the discharge :



at low pressure $C_2F_5 \rightarrow CF_2 + CF_3$

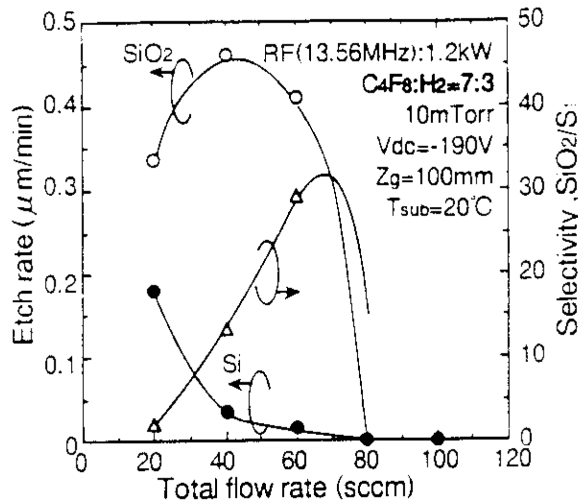


adding O_2 $2\ C_2F_5 \rightarrow 2\ CF_2 + 2\ COF_3$

SiO2 contact window opening → high selectivity over Si

by adding hydrogen in the CF discharge, better control of selective deposition of polymer is possible

$C_4F_8 + H_2$, ICP reactor

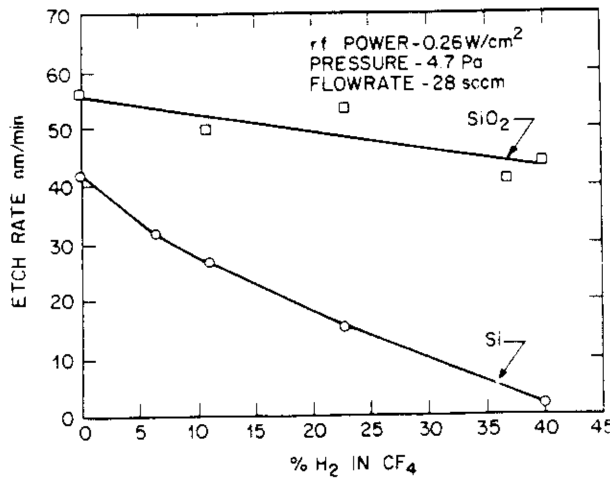


Etch rates of SiO_2 and Si in ICP C_4F_8-H_2 discharge

adding H scavenge F atoms which are responsible for Si etching
selective deposition of polymer on Si

Fukasawa JJAP 33 (1994) 2139

similar effect reported earlier in RIE system with CF_4-H_2 chemistry



Ephrath JES 126 (1979) 1419

straight profiles can be obtained by RIE :

⇒ using carbon containing gas mixture
(sidewal passivation by polymer formation, stops the isotropic etch)

⇒ using very low pressure plasma
(etch profile mainly controlled by ions motion)

⇒ using low temperature
(reduce the isotropic component of etch rate)

tapered edges can be obtained by :

⇒ wet etchant

only in some particular cases : metal (Al or Cr but not Mo) or SiO_2 (thin films)

⇒ dry etchant (plasma)

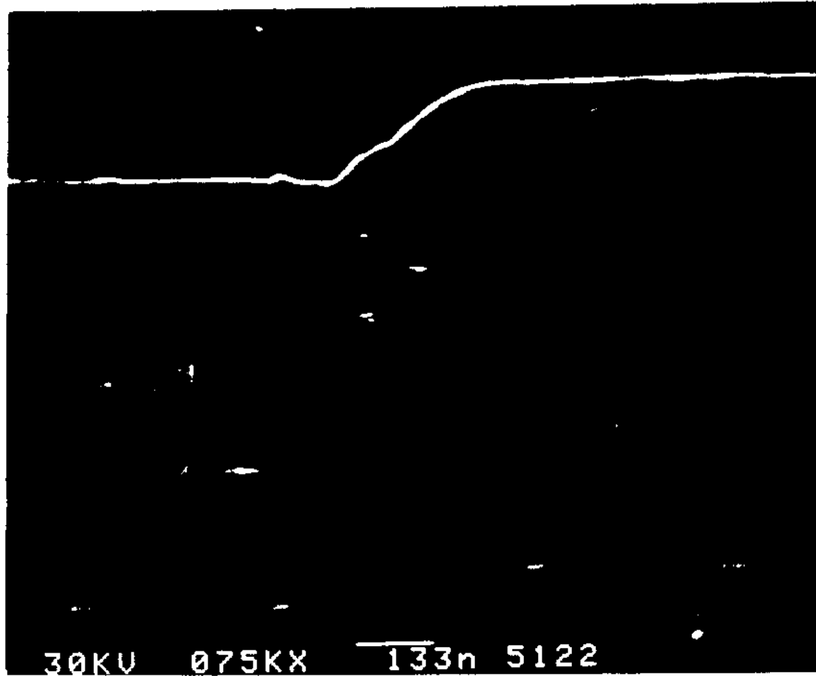
starting from reflowed resist using a chemistry which etches resist (depending on the ratio of resist etch rate over material etch rate, the final slope angle wil be lower or higher than that of the resist)

using a gas mixture which isotropically etches the resist mask

among the advantages
⇒ no need for further planarization
⇒ better coverage = higher yield

Si etching in SF6 / CHF3 / O2 (10 / 40 / 30)

using sharp edge resist, obtaining of 45° slope, because of the lateral resist consumption by O_2.



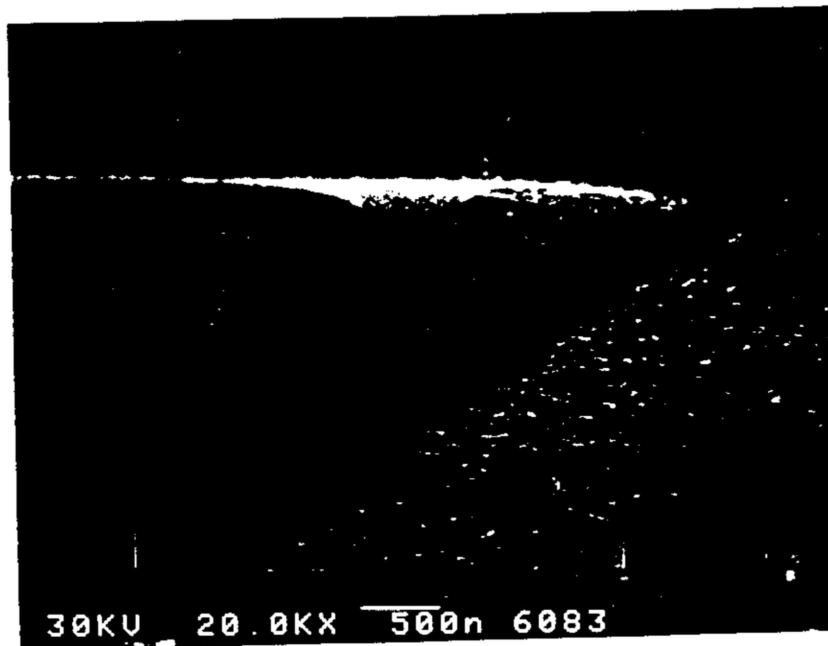
using "hard" baked resist, the slope can be much lower.

Si etching in SF6 / CHF3 (5 / 45)

using sharp edge resist, obtaining of straight profiles is possible.

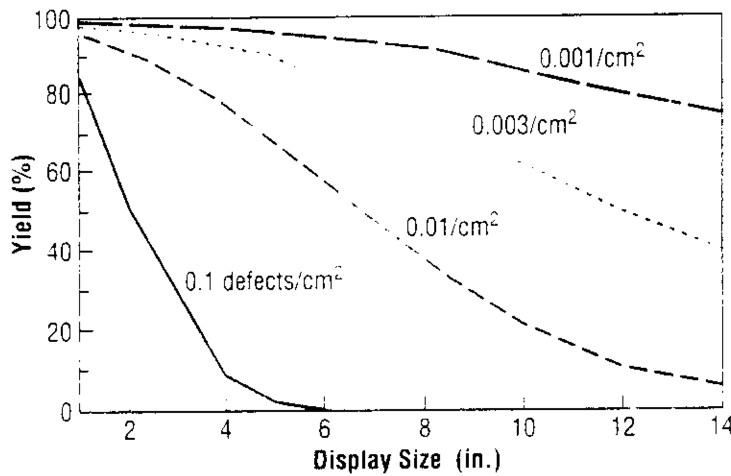
Ti-Mo double layer etching in SF6 / O2 (40 / 20)

using sharp edge resist, the edge slope is already low (< 45°).



using "hard" baked resist, the slope can be much lower (10 °).

This contamination affect dramatically the yield and the cost, especially for FPD. (not especially a problem with etching systems, but also with deposition or implantation systems)

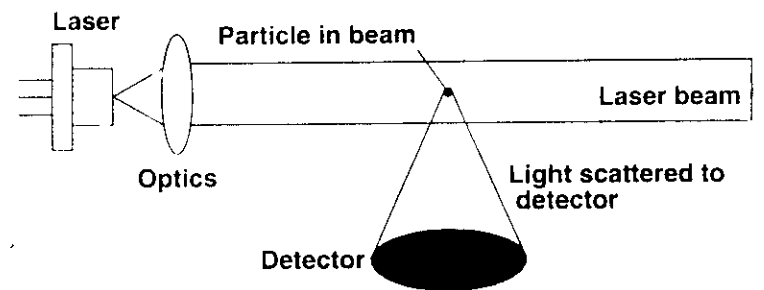


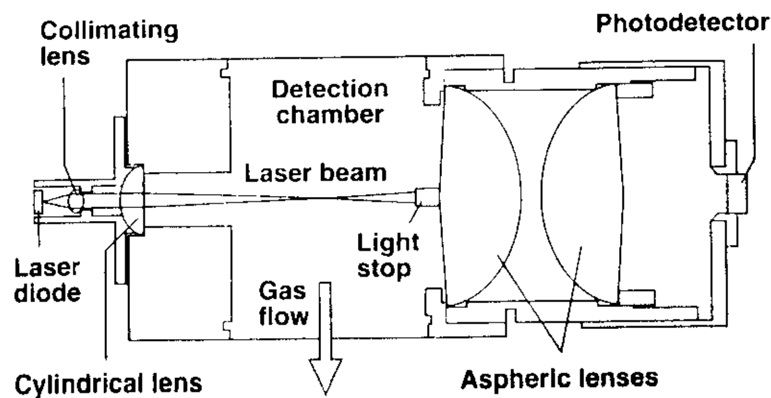
from O'Mara, SST

Much care is taken regarding particulate contamination during processes (clean rooms, laminar flows of filtered air, quality of products...) including the replacement of human workers by robots for transport.

→ Now, plasma tools are becoming a major source of particle contaminations.

The particlees can be detected in-situ by Laser Light Scattering (LLS).





The particles are generated

- by the plasma chemistry (for deposition system)
- by flake of deposited material from the reactor walls (even in the etching systems)

they are sustained in the plasma (negatively charged) until they fall by gravity

- during the plasma treatment
- after the plasma turn off

as you can not suppress the formation of dust in the plasma,
you have to manage with it.

studies by LLS have shown that particles are trapped in particular regions of the plasma

- over the edges of the wafer (ring trap) at the sheath boundary
- over the center of the wafer (dome trap) at the sheath boundary

using LLS, electrode design can improve the particle elimination (intentionnaly placed particle traps with connection to exhaust)

In ECR reactor, it has been shown that particles drift along magnetic field lines and impige the substrates. In that case, they can stick into the surface or resist and induce defects.

Selwyn, JJAP 32 (1993) 3068

radiations damages — cured by annealing
contamination damages — removed by (wet) cleaning

plasma induced defects for the case of silicon substrate (model)
(S. J. Fonash, JES 137 (1990) 3885)

region 1 : residue layer (tens of Å)

depends on the etching chemistry (anisotropy and selectivity often depend on the formation of a surface blocking layer)

pure polymer — removed by resist stripping or solvent cleaning

SiF_xO_y (case of CF_4/O_2 plasma) — removed by diluted HF after stripping

metallic impurities contamination : problem with high density plasma
- remove antennas from the chamber
- use hard material (Al_2O_3) as much as possible

region 2 : bonding damaged layer

caused by ion acceleration to the substrate
effect worse when decreasing pressure or increasing power (main correlation with energy of ions and not density)
threshold at 30 eV (displacement of Si atom in the lattice for E>20 eV)

affect
- barrier height at Au-Si schottky junction
- interface states density in MOS diodes

example : deposited SiO_2 on Si by DECR plasma (see part 2)

on a blank (100) Si substrate after standard cleaning (*)

→ $D_{it} \sim 2\ 10^{10}\ cm^{-2}\ eV^{-1}$

on a blank (100) Si substrate after $SiCl_4$ RIE and improved cleaning (*)

→ $D_{it} \sim 10^{11}\ cm^{-2}\ eV^{-1}$

(no residue, heavy ions)

on a blank (100) Si substrate after $CHF_3/SF_6/O_2$ RIE and improved cleaning (**)

→ $D_{it} \sim 10^{12}\ cm^{-2}\ eV^{-1}$

(polymer, light? ions)

(*) standard cleaning : surface oxydation (30Å) and diluted HF, removes 15 Å of Si
(*) improved cleaning : repetition of the standard cleaning

region 3 : impurity permeation layer

typically for hydrogen
not clear how deleterious is the effect
main problem reported is the passivation of dopant (but easily reactivated)

radiation effects : creation of positive charges in SiO_2 under UV exposure (from high density low pressure plasma, H_2 or O_2)

most popular technique because of its simple principle
(for transparent or semi-transparent films)

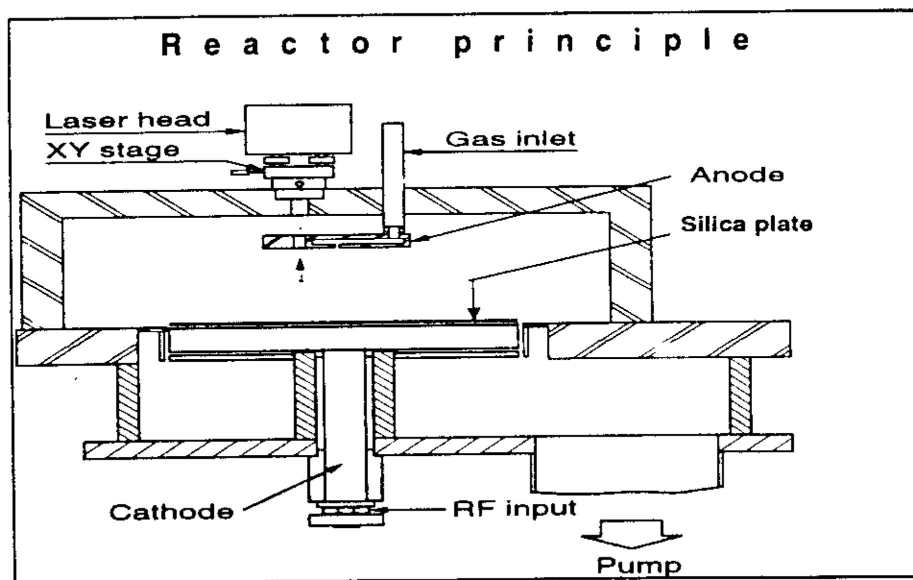
laser light is reflected at the outer (top) and inner (bottom) interface between the etched film and vacuum or substrate. and, depending on actual film thickness and refractive index, two beams interfer.

→ continuous etch rate measurement and end-point detection

best accuracy for film thickness larger than thickness corresponding to one period

Si	80C Å
Si_3N_4	1500 Å
resist	~1900 Å
SiO_2	2200 Å

accuracy improved by the use of the first derivative of the signal



example of implementation on a RIE reactor
(substrate on the biased electrode in RIE, small optical aperture...)

end-point control : overetch time has to be calibrated according to the uniformity of the reactor

complement to laser interferometry for
- very thin films
- metallic or transparent films

commonly used plasmas are glow discharges (a part of the plasma species is electronically excited into an optically emitting excited state)

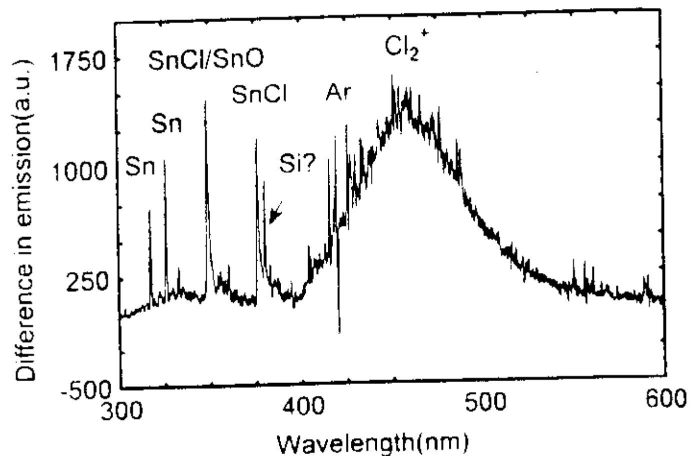
→ informations concerning the species present in the plasma can be obtained from their optical signatures.

→ can be used for plasma analysis but active species are not necessary desactivated by radiations

→ for end-point control, one line relative to the material etched is enough : it can be found in tables and checked by experiment (differences of spectrums)

more complex than laser interferometry because of the use of a spectrometer but it is a global end-point control, which takes into account reactor uniformity.

examples :
following of Al etching through the recording of the intensity of the 2614Å line.
following of n+ type Si on Si (aSi TFT : Back Channel Etch structure)
following of transparent electrode (ITO) etching (Molloy JES 142 (1995) 4285)



Tuning impedance control (automatic) is for a long time a standard equipement of the electrode bias in RIE system, with the aim to improve coupling and efficiency by annuling reflected power.

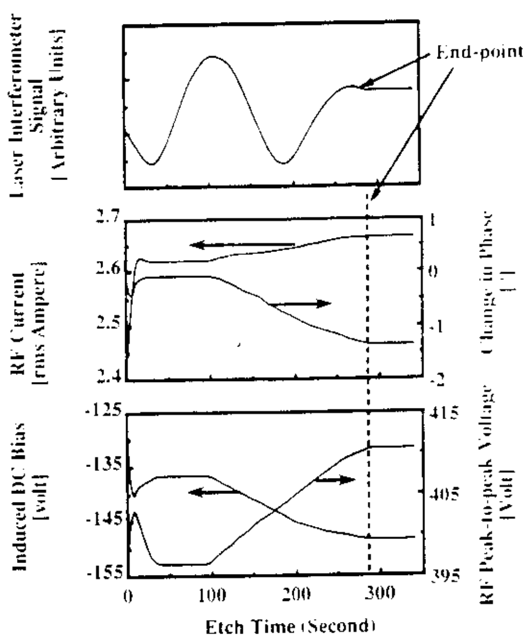
The technique just involve the recording of some of the rf energy coupling parameters (between generator and plasma) : a signature of plasma impedance.

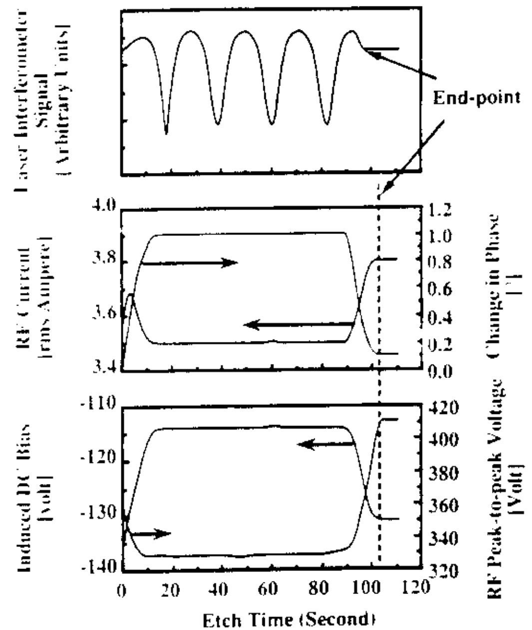
Simple control because external.

after the plasma turn on,

- gas phase composition change with respect to etchant products
- after a short time (scale of seconds) tuning parameters converge to a first set of tuning values
- after etch completion and evacuation of residual etchant species, tuning parameters converge to a secund set of values

examples :





Patel APL 61 (1992) 1912

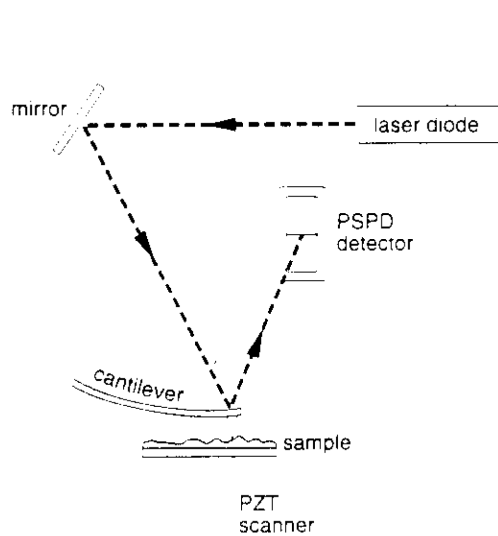
The in-line control in displays fab is mainly :
- optical microscope (limited in resolution)
- stylus profilometer
- electrical measurements (if possible)

The precise control of lithographic - etching processes (detection of small defects, size < 0,5 μm) is only possible by Scanning Electron Microscopy, but it is destructive.

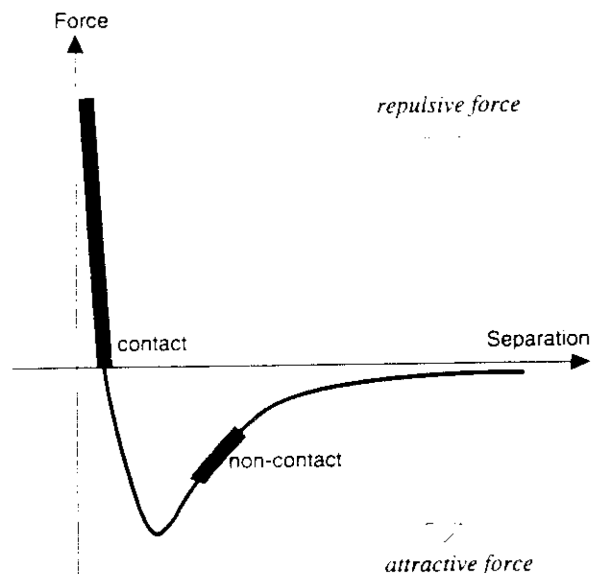
For a few years, a new technique is available, the

Atomic Force Microscopy,

which allows the precise characterisation of the surface (roughness, resist defects or residues...) and the measurements of etched step (profilemeter) and feature size (Dimensional Control).



Schematic of optical-deflection technique for detecting cantilever deflection.



Van der Waals force versus tip to sample distance.

Deposition : Summary

Si_3N_4 deposition for glass capping

SiO_2 deposition for gate insulation

Deposition : Si_3N_4

Silicon nitride is the material of choice for passivation cf active devices and circuits because of its excellent diffusion barrier properties (moisture and alkali ions)

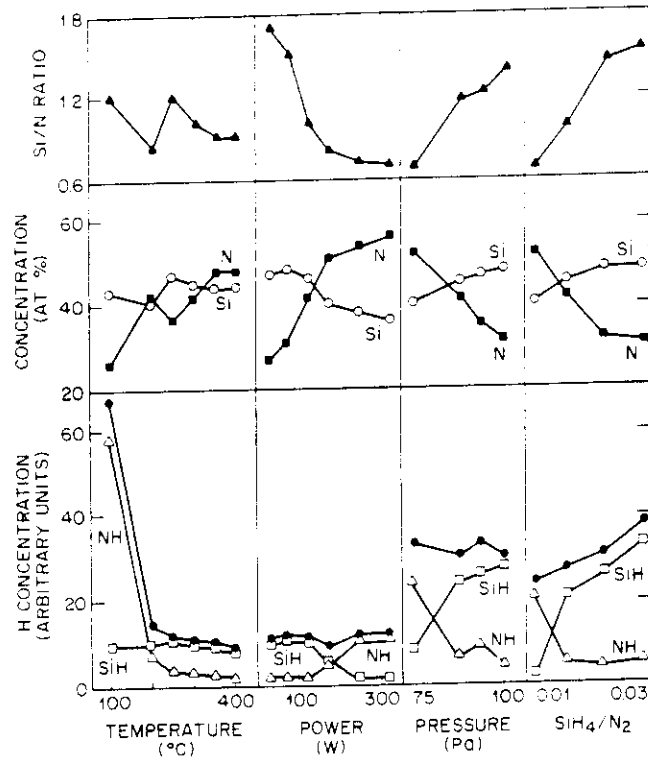
→ well suited for glass capping

Film Property	APCVD 900°C	PECVD 300°C
Composition	Si_3N_4	$Si_xN_yH_z$
Si/N ratio	0.75	0.8–1.0
Density	2.8–3.1 g/cm^3	2.5–2.8 g/cm^3
Refractive index	2.0–2.1	2.0–2.1
Dielectric constant	6–7	6–9
Dielectric strength	1×10^7 V/cm	6×10^6 V/cm
Bulk resistivity	10^{15}-10^{17} ohm-cm	10^{15} ohm-cm
Surface resistivity	>10^{13} ohms/square	1×10^{13} ohms/square
Stress at 23°C on Si	$(1.2\text{-}1.8) \times 10^{10}$ dyn/cm^2 (tensile)	$(1.8) \times 10^9$ dyn/cm^2 (compressive)
Thermal expansion	4×10^{-6}/°C	>4<7×10^{-6}/°C
Color, transmitted	none	yellow
Step coverage	fair	conformal
H_2O permeability	zero	low–none
Thermal stability	excellent	variable, >400 °C
Solution etch rate		
BHF(6:1) 20–25°C	10– 15 Å/min	200–300 Å/min
49% HF 23°C	80 Å/min	1,500–3,000 Å/min
85% H_3PO_4 155°C	15 Å/min	100–200 Å/min
85% H_3PO_4 180°C	120 Å/min	600–1,000 Å/min
Plasma etch rate		
70% F_4/30% O_2, 150 W, 100°C	200 Å/min	500 Å/min
Na^+ penetration	<100 Å	<100 Å
Na^+ retained in top 100 Å	>99%	>99%
IR absorption		
Si–N maximum	~870 cm^{-1}	~830 cm^{-1}
Si–H minor	none	2,180 cm^{-1}

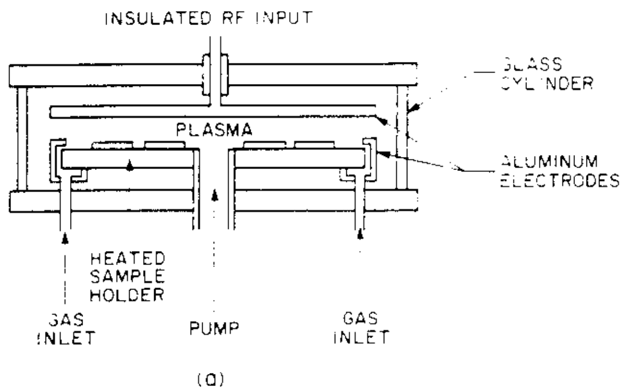
a comparison of properties of silicon nitride prepared fron SiH4-NH3-N2 by thermal APCVD abd PECVD (Kern, JVST 14 (1977) 1082)

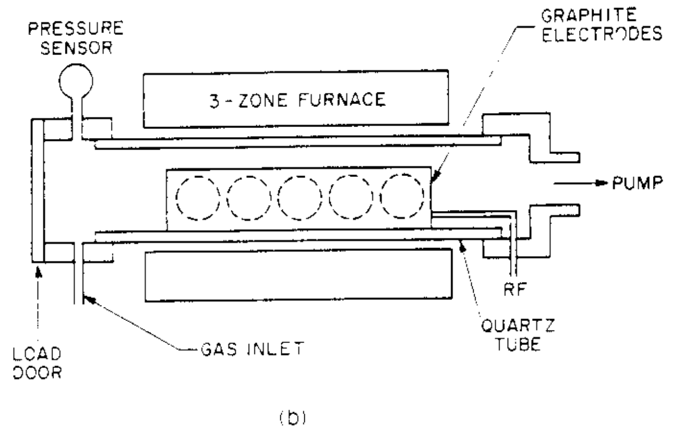
If the composition of the CVD material (LPCVD or APCVD) is close to Si_3N_4, the one of PECVD depends a lot on deposition conditions.

The material is usually described as an alloy ($Si_xN_yH_z$).



from Dun, JES 128 (1981) 1555





parallel-plate radial design	**parallel-plate tubular design**
cold wall batch for Si up to 4" (single wafer for 6 and 8")	hot-wall batch for first generation glass sheets (150 mm x 150 mm)

radial refers to gas flow
tubular refers to furnace geometry

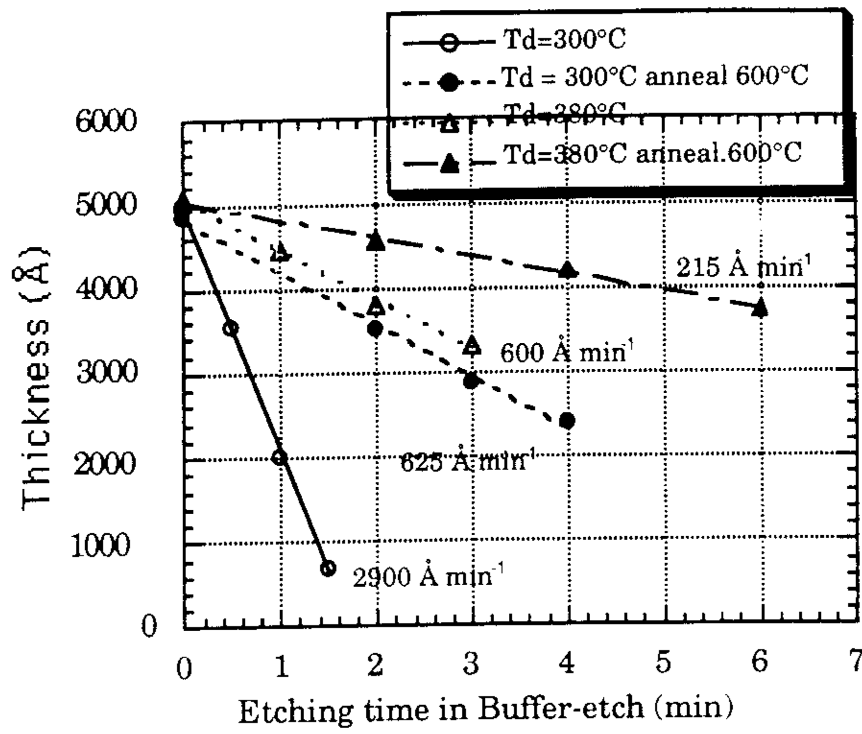
improvement of uniformity by the :

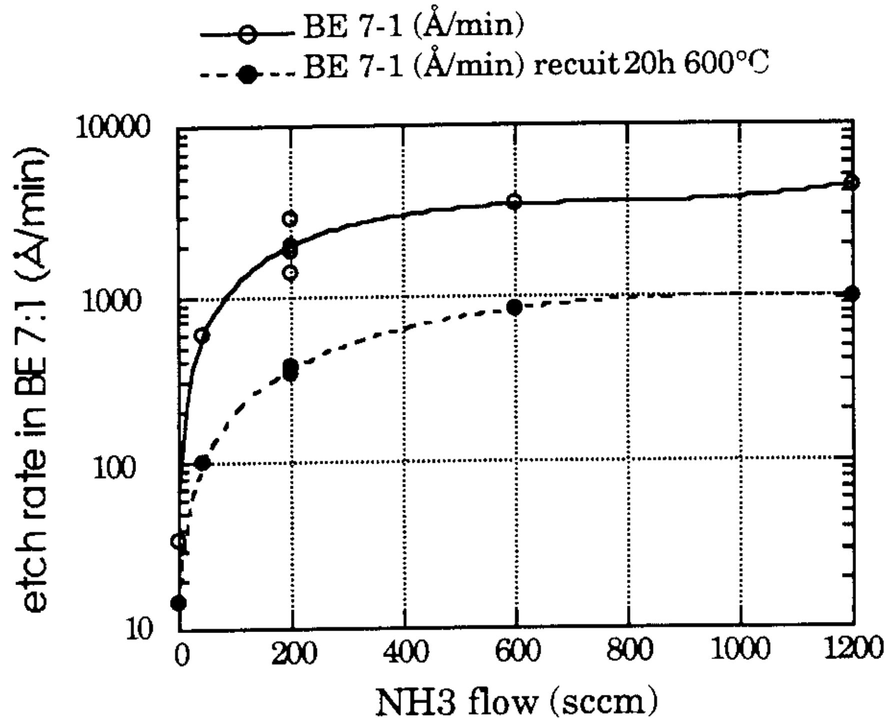
use of gas shower electrode	use of pulsed rf power

The optimisation of a deposition process depends onrequirements on film quality.

For glass capping, $Si_xN_yH_z$ has to be deposited at low temperature (CVD not possible)
must act as a diffusion barrier for impurities contained in the glass, even after a few tens of hours at 600°C

measured in Buffered HF (HF:NH4F, 1:7) at 20°C

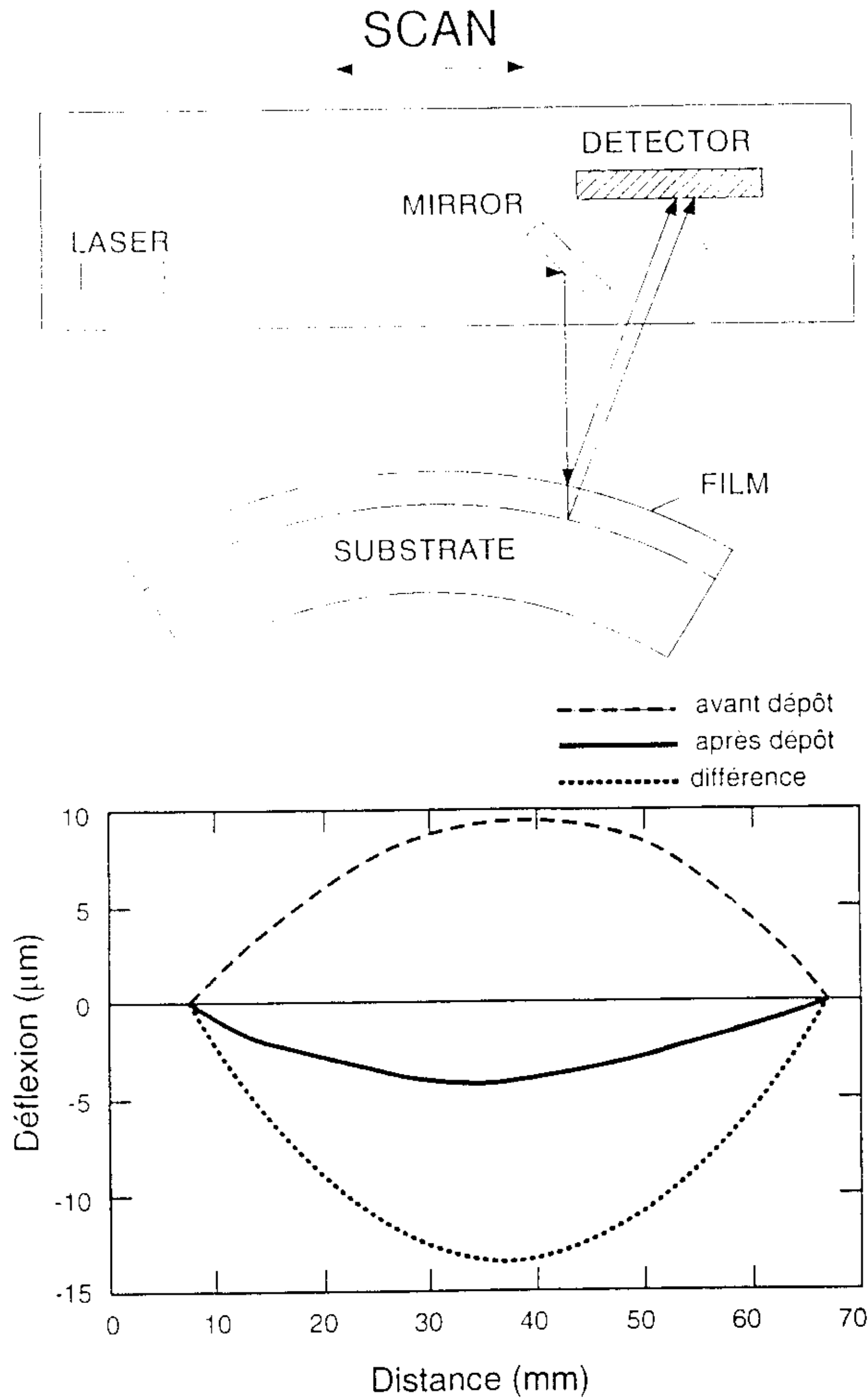


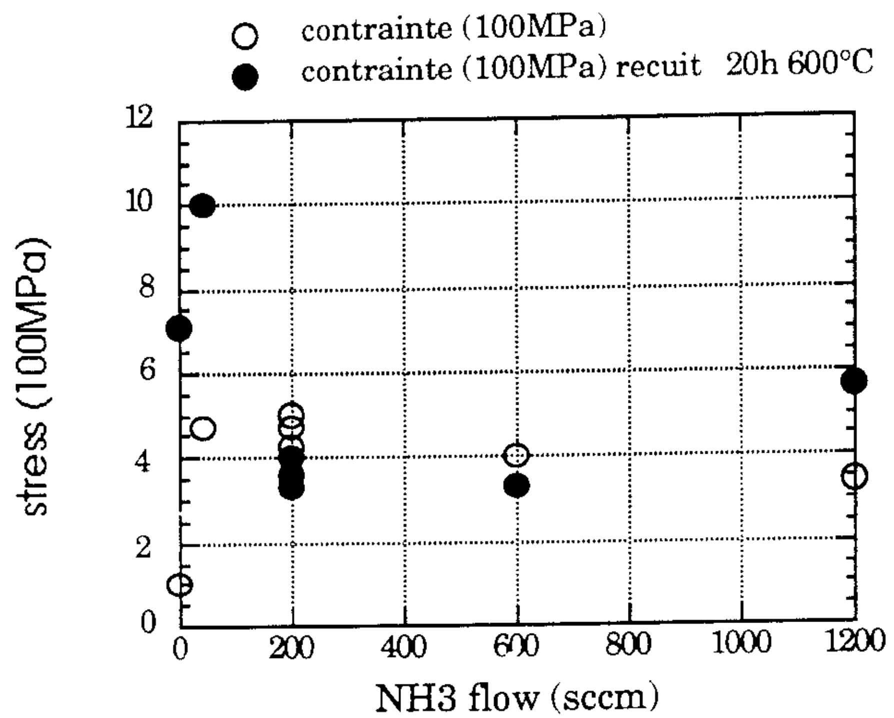


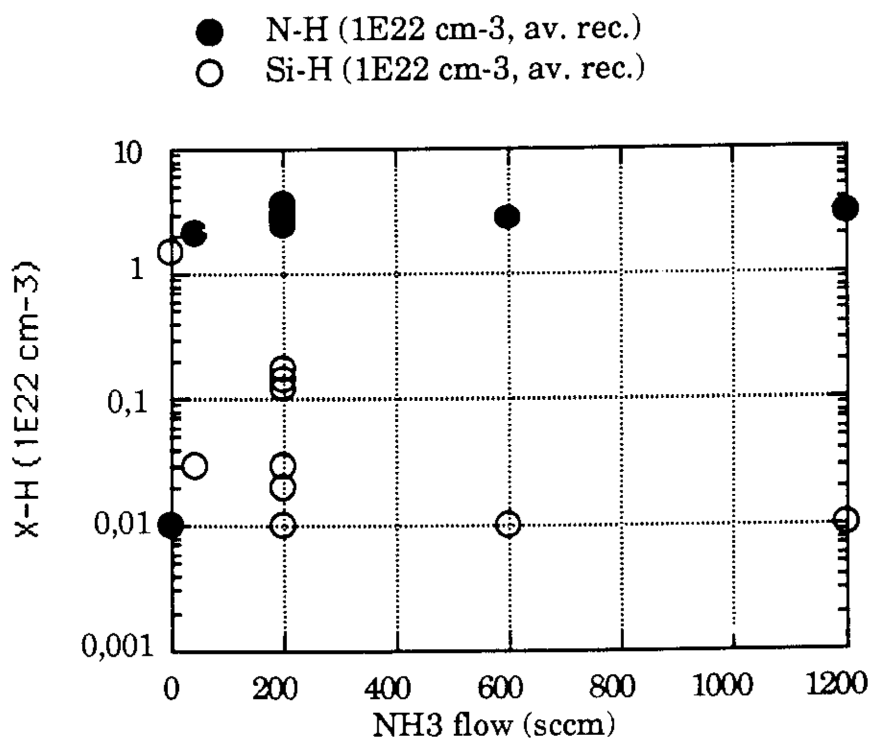
The lower the etch rate
the higher the density
the lower the diffusion coefficients **IF STOICHIOMETRY CONSTANT**

stress can be tensile or compressive
usually a few hundreds of MPa (a few 10^9 dynes/cm^2)
to be kept as low as possible to avoid cracks and peel-off

principle of measurement (Flexus system)




contrainte (100MPa)
contrainte (100MPa) recuit 20h 600°C
stress (100MPa)
NH3 flow (sccm)
0
2
4
6
8
10
12
0
200
400
600
800
1000
1200


N-H (1E22 cm-3, av. rec.)
Si-H (1E22 cm-3, av. rec.)
X-H (1E22 cm-3)
NH3 flow (sccm)
10
1
0,1
0,01
0,001
0
200
400
600
800
1000
1200

MOS diode : Metal - Oxide - Semiconductor diode → control of MOSFET curent flow

accumulation regime   inversion regime

Energy diagram of the MOS system for n-type silicon

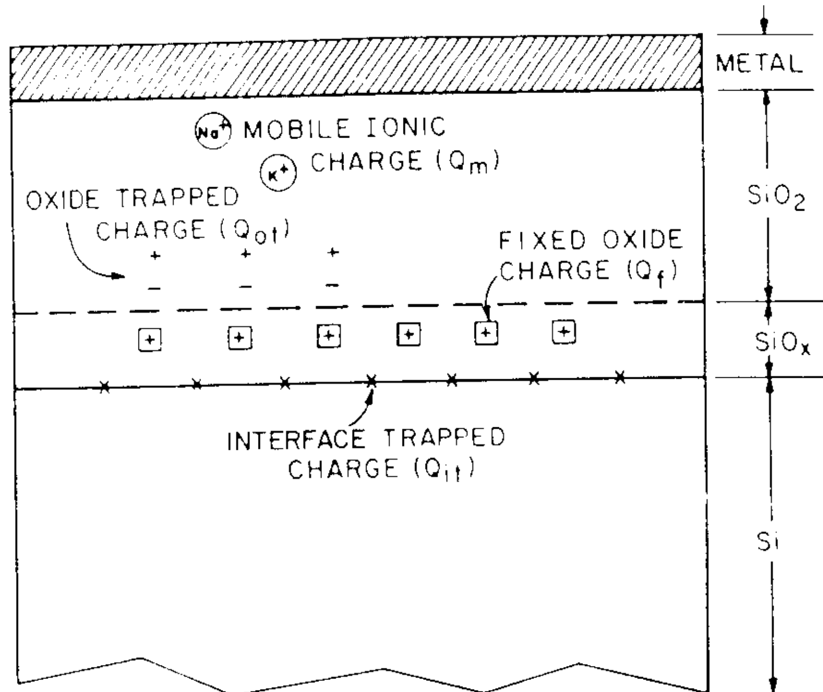
accumulation regime   inversion regime

Energy diagram of the MOS system for p-type silicon

n - MOSFETs : on for Vgs > 0
off for Vgs > 0

p - MOSFETs : on for Vgs < 0
off for Vgs > 0

electrically active defects modify the C(V) characteristics and as the consequence, the MOSFET subthreshold slope.



Terminology of defects at the Si-SiO_2 interface (Deal IEE TEC 27 (1980 606)

Extraction of interface traps capacitance (and density) from combined high - low frequency C(V) measurements

at high frequency, interface traps do not contribute to the measured capacitance (the lower trap time constant is higher than the measurement signal period).

in that case $1 / C_{HF} = 1 / C_{ox} + 1 / C_{sc}$

at low frequency, all interface traps contribute to the measured capacitance (the longer trap time constant is lower than the measurement signal period).

in that case $1 / C_{LF} = 1 / C_{ox} + 1 / (C_{sc} + C_{it})$

C_{it} is deduced from C_{LF} and C_{HF}.

CHEMICAL VAPOR DEPOSITION

APCVD

300°C - 450°C
760 Torr

LPCVD

450°C - 800°C
1 Torr

PECVD

200°C - 400°C
0,1 - 10 Torr
13,56 MHz

or

2,45 GHz

$B = 0$
"remote"

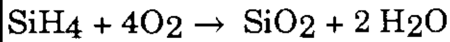
$B \neq 0$
ECR
DECR

CVD for Chemical Vapor Deposition

atmospheric pressure CVD	APCVD	hot wall
low pressure CVD	LPCVD	hot wall or cold wall

among the advantages : batch reactors, large throughput, large up-time
old technique but mature production tools

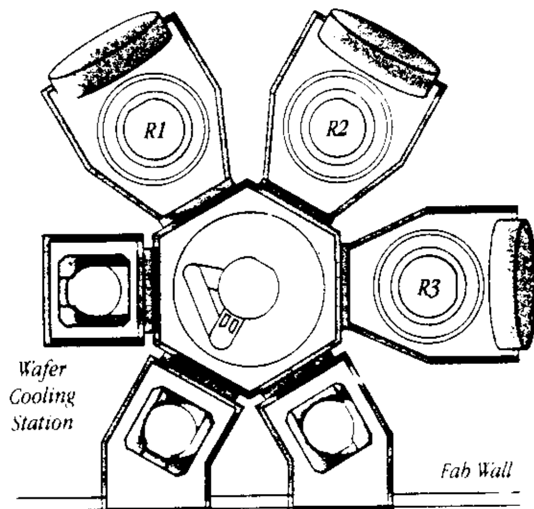
Deposition only on heated surfaces by cracking of gas molecules and surface reactions to form solid compounds and gaseous reaction products

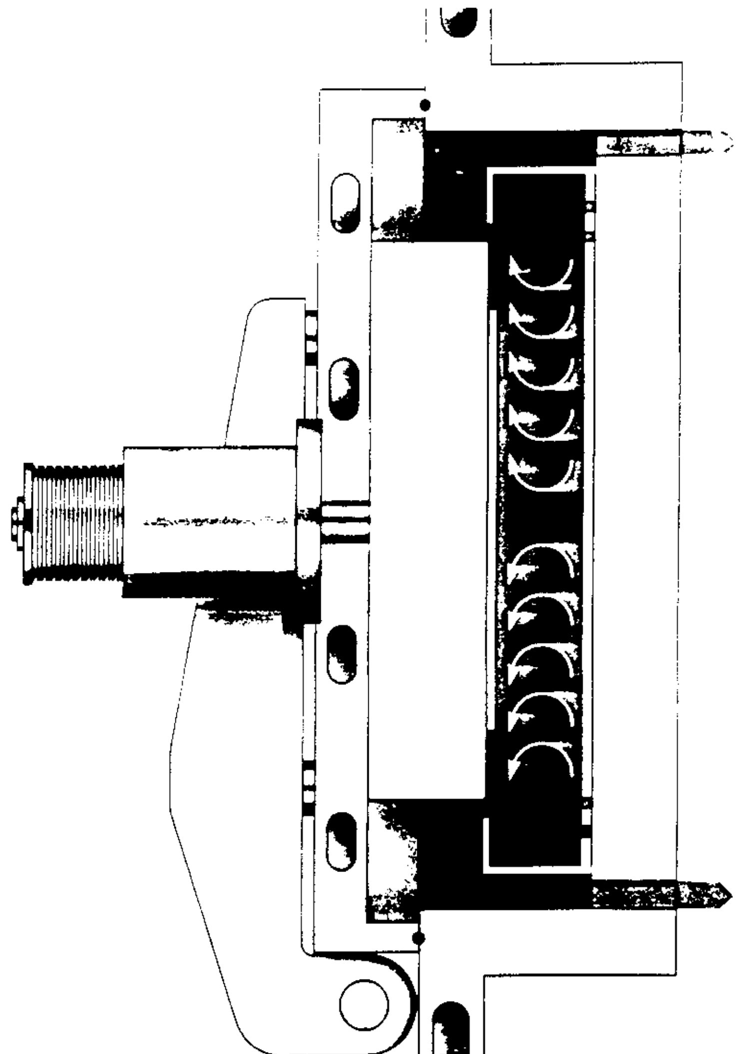


$SiH_4 + 4O_2 \rightarrow SiO_2 + 2\,H_2O$

mainly used in IC's fabrication for intermetals insulation with TEOS + O_3 chemistry
better step coverage than in $SiH_4 + O_2$ chemistry

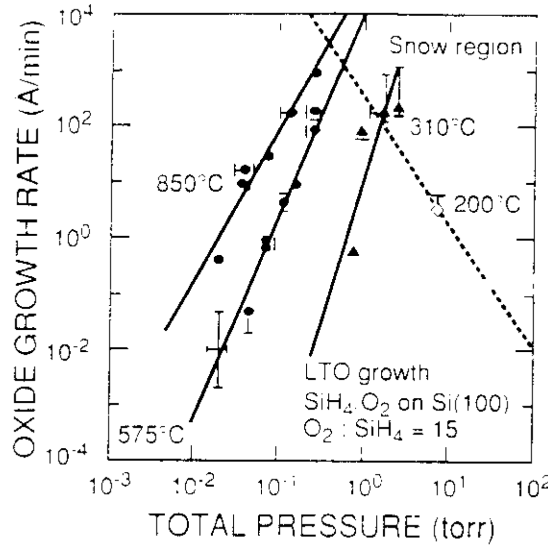
single-wafer deposition system
from Watkins-Johnson company



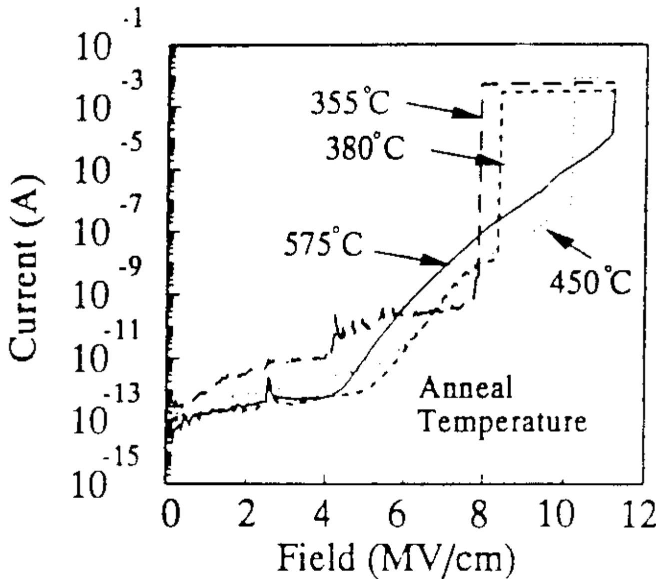


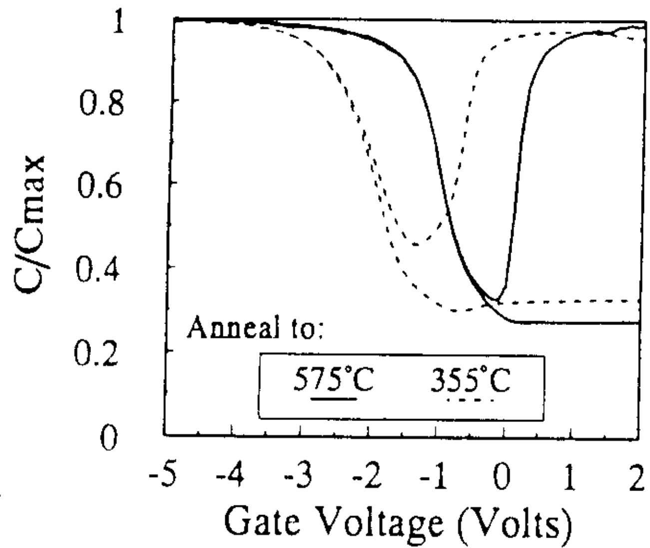
CVD chamber (reduced chamber volume, cold wall, distributed gas injection...)

Evaluation of the LPCVD process for gate oxide deposition (Liehr, APL 60 (1992) 198)
UHVCVD system, cold wall, lamp heated substrate
RCA cleaned wafers, final HF treatment under vapor phase



oxide deposition rate as a function of the total pressure (SiH_4 + O_2 chemistry)
snow region : deposition of dust (SiOHx particles) in all the reactor





Electrical evaluation of Al-SiO_2-Si diodes for different deposition temperature(current-voltage and C(V))

LPCVD oxides deposted at temperatures below 450°C exhibit high leakage current, low field breakdown and strong carrier

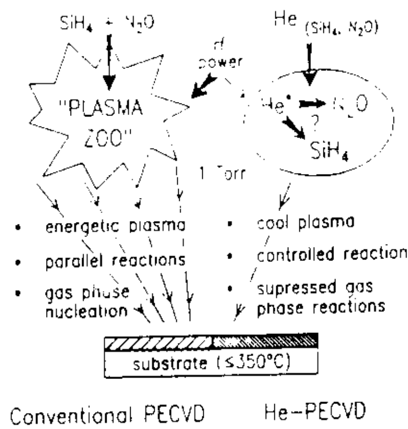
Low temperature LPCVD oxides are not suitable for gate oxide applications because of the deposition chemistry which leads to incorporation of hydroxyl species in the films.

benefit from the developpment of reactors for aSi:H processes (large surfaces available)

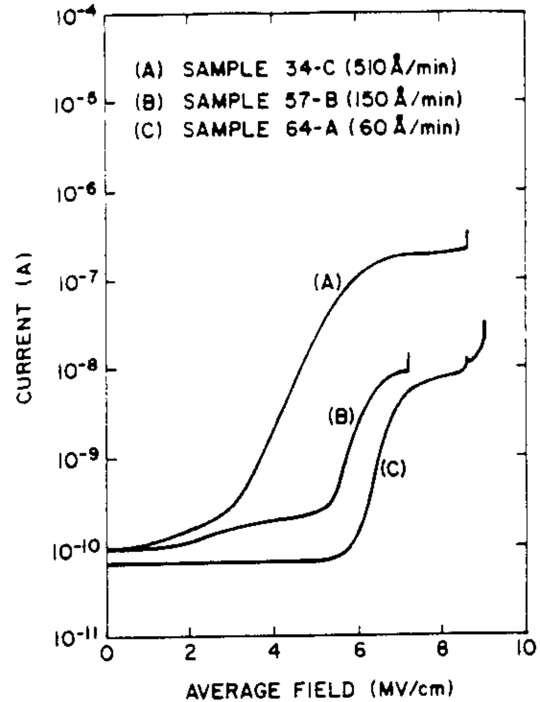
not used in Si IC's (possible use for intermetal but poor step coverage)

introduced in the mid 80's by IBM for TFT applications (J. Batey ASS 39 (1989) 1)
developpment based on the observation that standard PECVD SiO_2 is not suitable for gate oxide applications.

main characteristics : He dilution and low deposition rates



conventional versus He-diluted processes



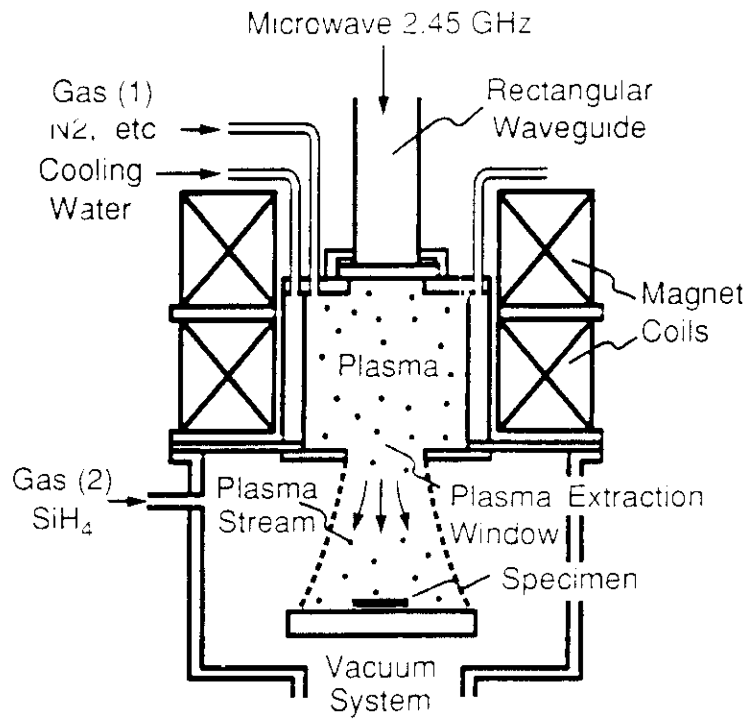
effect of deposition rate on I(V) characteristics

after a 400°C Post Metallisation Anneal under forming gas, $D_{it} < 4\ 10^{10}\ cm^{-2}eV^{-1}$

not suitable for aSi:H bottom gate TFT
not so used for poly-Si TFTs

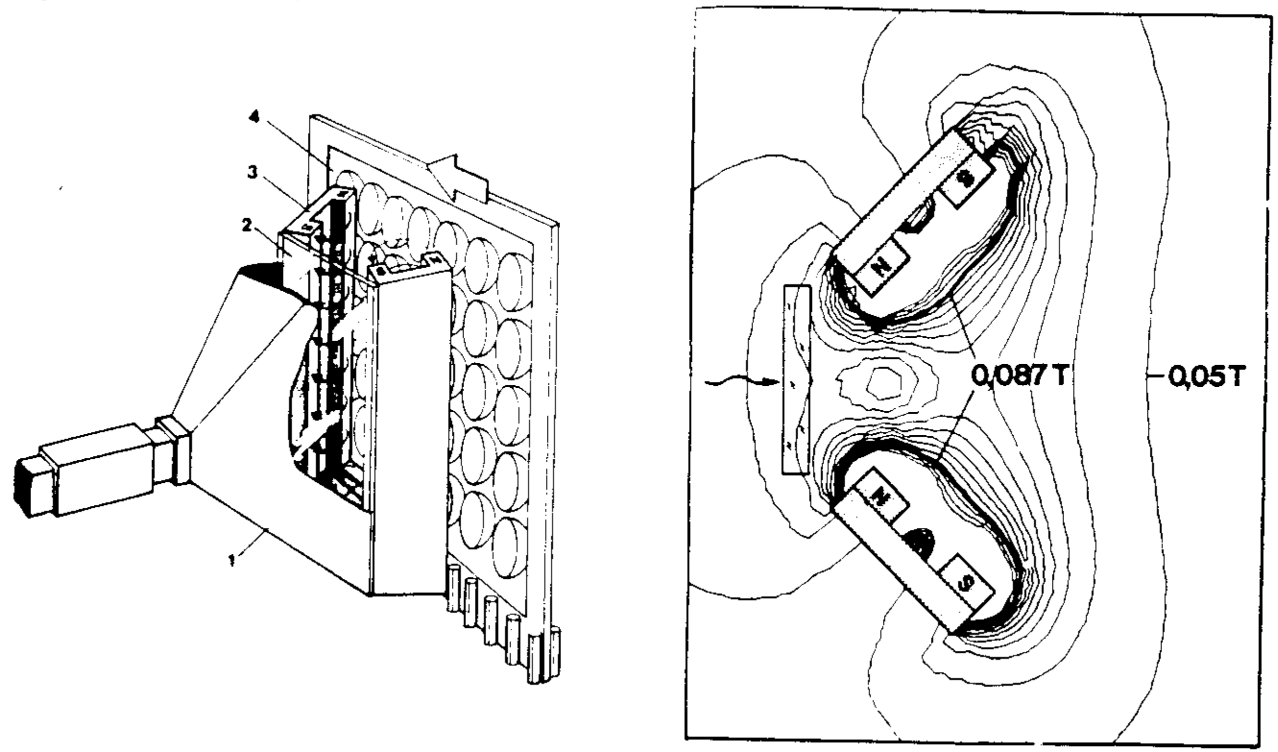
ECR deposition systems

Classical ECR source



Matsuo JJAP 22 (1983) L210

Elongated ECR source

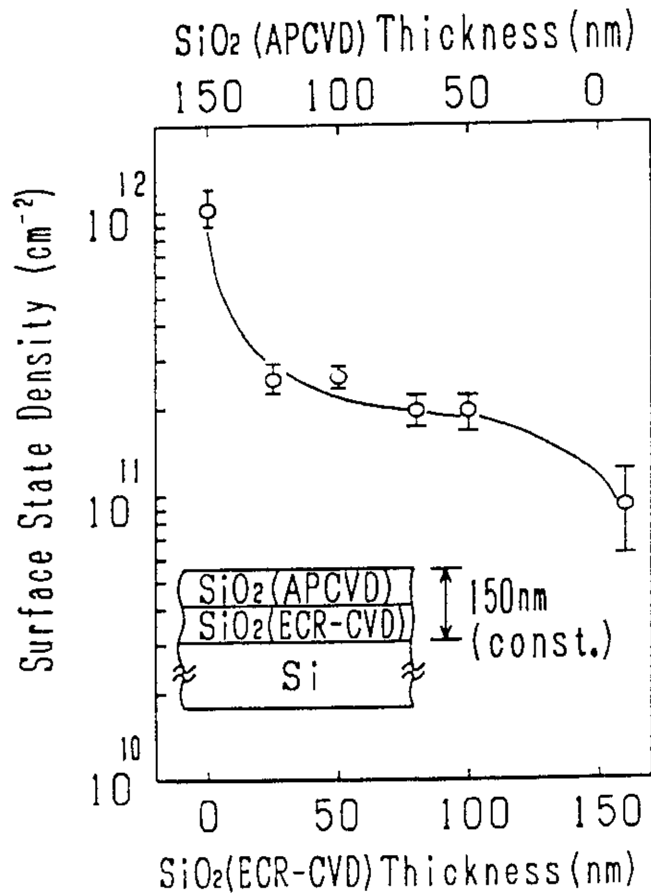


Geisler JVST A8 (1990) 908

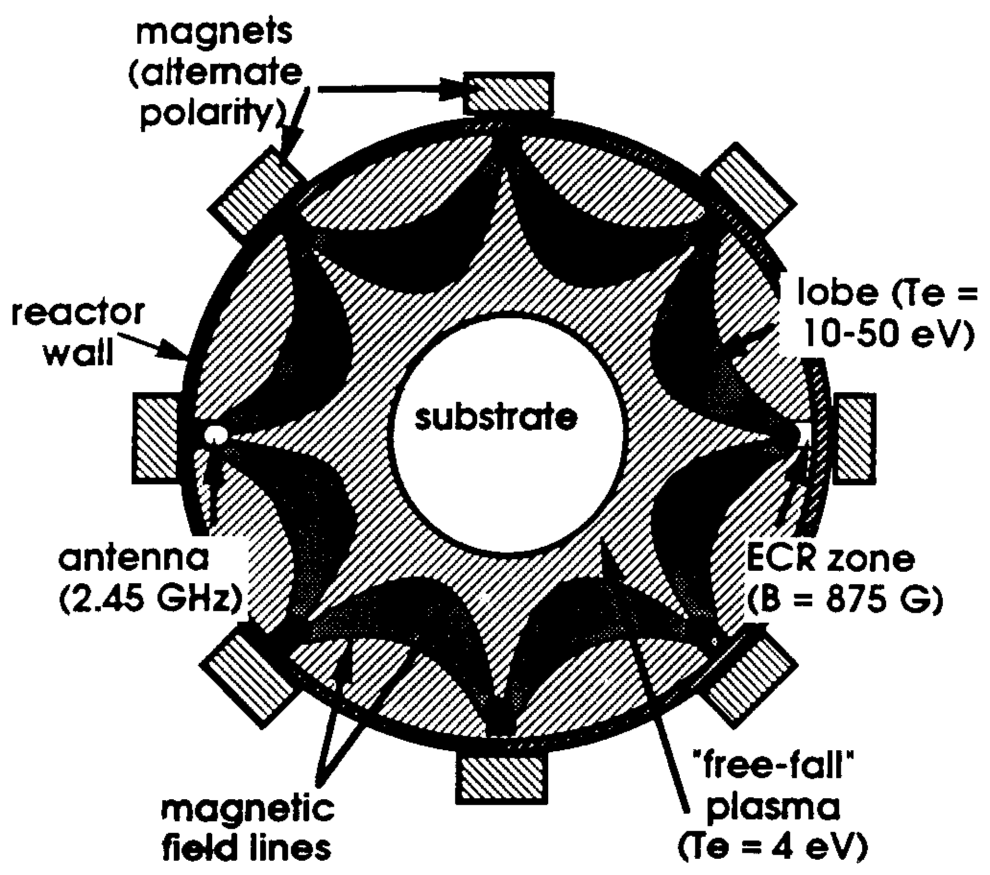
ECR PECVD oxide are used by Seiko Epson for the process of poly-Si TFTs

T. Little JJAP 30 (1991) 3724

Due to uniformity issues, a slide is used to select the most uniform zone of the plasma.
To increase the throughput, a double layer with APCVD oxide is used.



Classical DECR source for Si wafers up to 8"

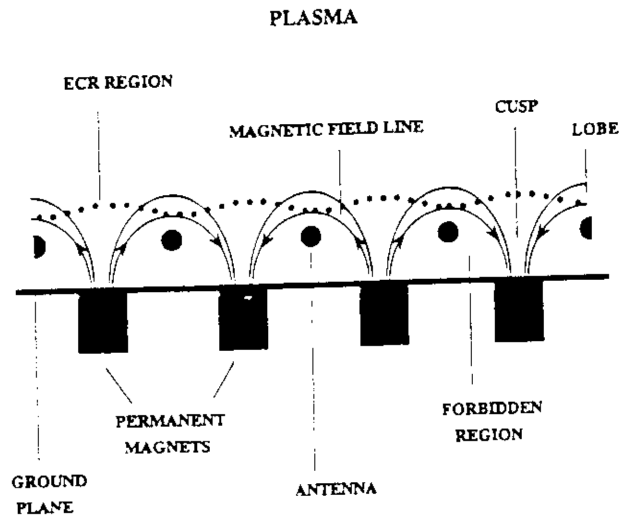


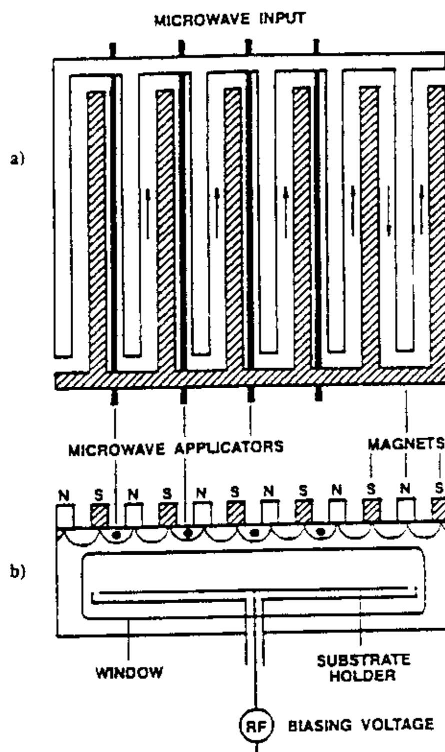
- ❶ microwave excitation + magnetic field
  → ECR conditions
- ❷ distributed antennas (14)
  → good uniformity on 8"
- ❸ low working pressure (10^{-3} mbar)
- ❹ high ionic density (10^{11} cm^{-3})
- ❺ low energy ions (20eV) and electrons (3eV)

→ **HIGH QUALITY THIN FILM DEPOSITION <u>WITHOUT SUBSTRATE HEATING</u>**

Improved Uniform DECR (UDECR) design for large area substrates

Pelletier TSF 270 (1995) 49





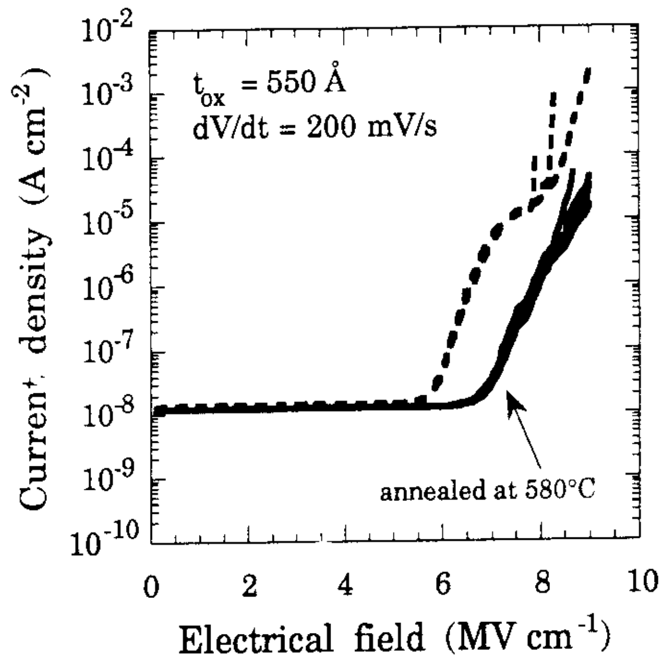
DECR oxide for gate insulation

- ALCATEL RCE200, 8" compatible
- Microwave plasma at low pressure
- Mixture of pure SiH_4 and O_2
- Deposition rate in the range of 1 Å/s
- Uniform on 8"

☞ <u>High quality Oxide at room temperature</u>

- "P-etch" rate < 4 Å/s as deposited
- $\rho > 2 \cdot 10^{16}\ \Omega cm$
- Ramp I(V) deviates from baseline for E > 5 MV/cm
- D_{it} on cSi(100) < 2 10^{10} cm^{-2} eV^{-1}

Bulk traps annealing



Poly-Si TFTs for large area electronics : summary

introduction

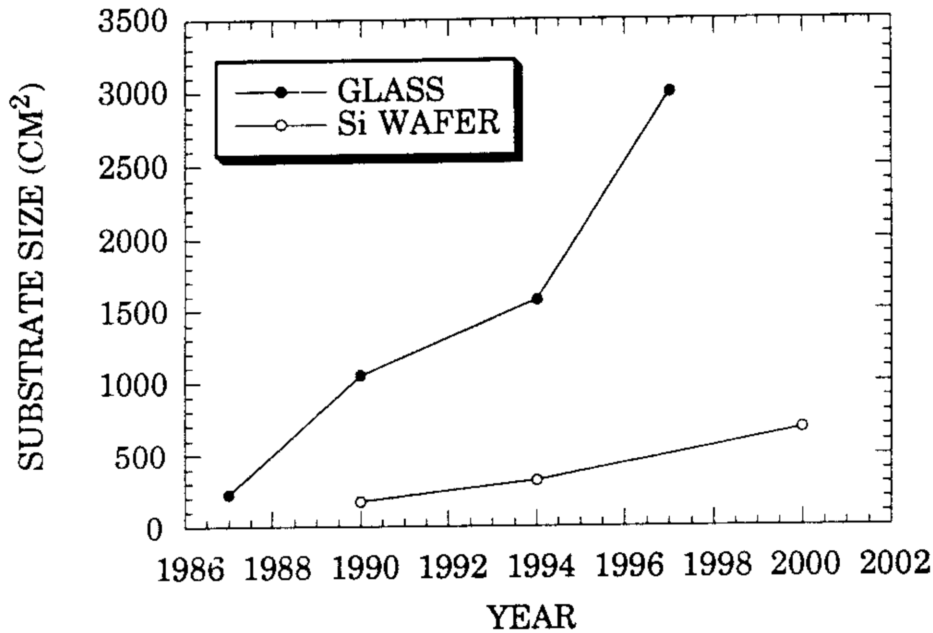
glass issues

device characteristics

device stability

circuits applications

large area electronics : up to now, mainly for displays applications



comparison of glass sheet and silicon wafer sizes

in the same time, the number of circuits (or displays) per sheet of glass

4 displays (14" diag.) in 50cm x 60 cm

is much lower than the number of circuits per Si wafer

more than 100 large (1 cm^2) circuits in 8" Si.

large area electronics : large substrates
large circuits

10 years ago, people thought it was crazy, just from a yield point of view

because of the use of glass, low temperature process (at least below 600 °C or less if possible) is necessary

Comparison of TFT characteristics for c-Si, poly-Si, a-Si:H and CdSe materials

c-Si :

material of reference because of ten's of years of experience in devices and circuits
not available on large area
transmittive displays not possible

a-Si:H :

presently used material for large area electronics (AMLCD)
some limitations for rapid circuits due to instability

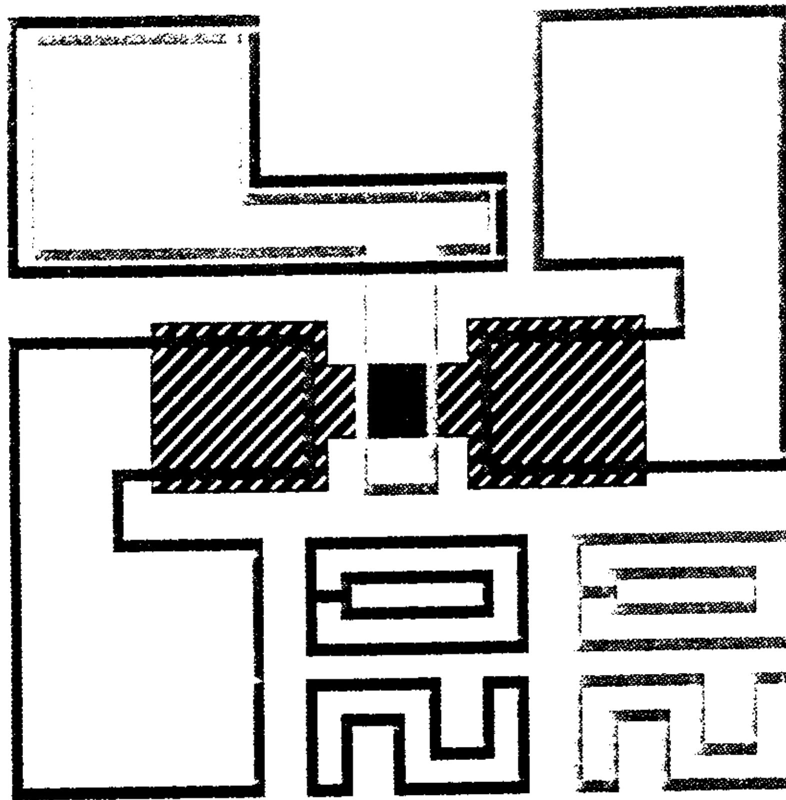
CdSe :

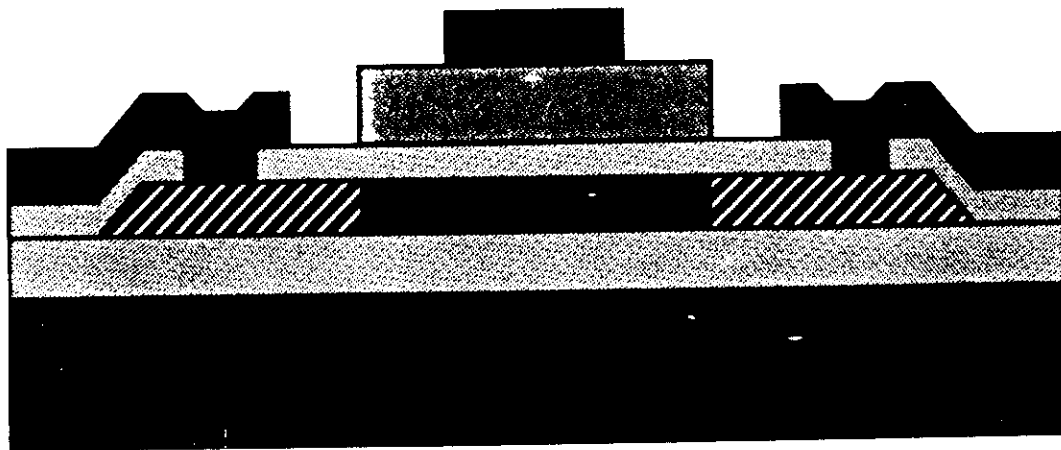
major drawback : it is not silicon

poly-Si :

now presented as a near future evolution for a-Si:H products
especially because of laser crystallisation

active layer	c-Si		poly-Si			a-Si:H	CdSe
	bulk	SOI	High-T	Low-T			
		SIMOX	SPC	SPC	Laser		
μfe, n-channel ($cm^2V^{-1}s^{-1}$)	400 to 700	300 to 600	40 to 120	20 to 70	50 to 400 *	0.2 to 1.5	50 to 400
μfe, p-channel ($cm^2V^{-1}s^{-1}$)	100 to 200	100 to 300	20 to 80	20 to 50	30 to 200		1 to 10
V_t (V) n-channel	0.25 to 1.75	0.2 to 1	1 to 5	2 to 8	1 to 5	0.5 to 5	0.5 to 5
V_t (V) p-channel	-0.25 to -1.75	-0.2 to -1	-2 to -8	-2 to -10	-1 to -5	-	-1 to -5



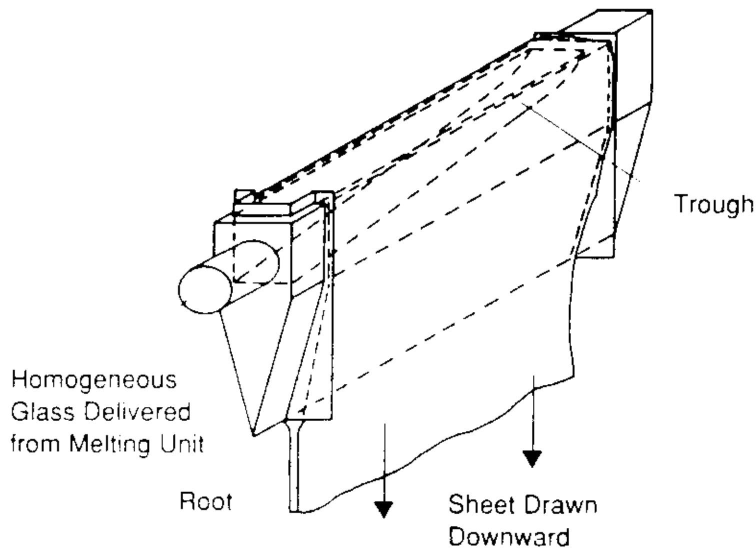


step	description	mask
1	hard glass capping layers	
2	active layer deposition (intrinsic)	
3	active layer crystallisation	
4	active layer definition	1
5	gate insulator deposition	
6	gate deposition	
7	gate definition	2
8	NMOS contacts implantation	3
9	PMOS contacts implantation	4
10	gate passivation	
11	implantation activation annealing	
12	contact windows opening	5
13	aluminum metallisations	
14	metallisation definition	6
15	metallisation sintering	
16	hydrogenation (if necessary)	
17	final passivation	

as for Silicon On Insulator (SOI) : no need for
- junction isolation (SiO_2)
- LOCOS (island)
- threshold voltage adjustement

enhancement mode NMOS and PMOS (normally off)

Poly-Si TFTs : glass issues..........glass fabrication



fusion down draw process from Corning

in competition with the float process (glass flow over an horizontal bath of melted tin)

depending on the constituents of the molten phase, different types of glass can be fabricated with different thermal properties.

T_S = strain-point temperature = temperature where viscosity = $10^{14.5}$ poises.

better if processing temperature (if long times are involved) kept below Ts - 100°C.

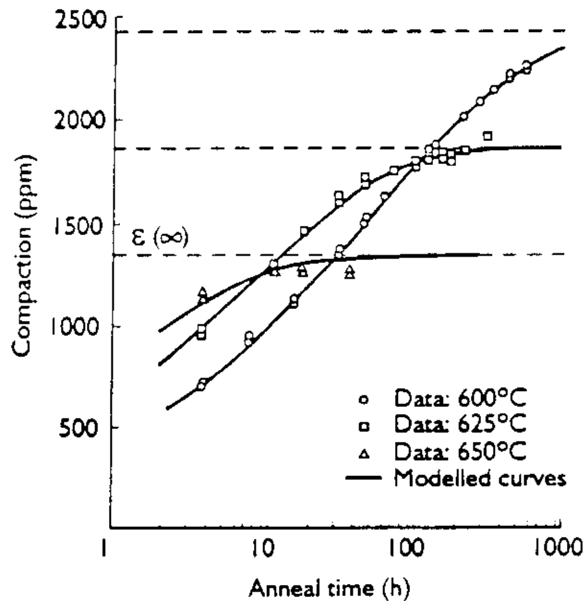
Glass code	composition	Strain-point temperature (°C)
Corning 7059	Barium aluminoborosilicate	593
Corning 1737	Alkaline-earth aluminosilicate	666
Hoya Na40	Alkaline-earth-zinc-lead aluminosilicate	655
NEG OA-2	Alkaline-earth-zinc aluminoborosilicate	645

near room temperature, glass is "considered" as a solid but it is in fact a very viscous liquid. → heating it will cause compaction or shrinkage.

compaction (C) versus anneal time

$$C(t) = C_{max} (1 - \exp(-t/\tau)^{\beta})$$

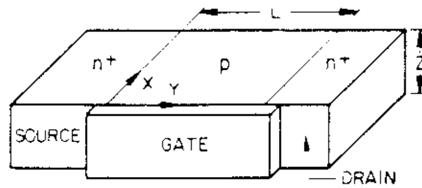
where τ and β present unique values for each glass



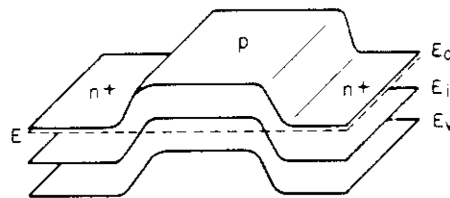
Glass compaction for Corning 1733

Brotherton, IDRC'94, 130

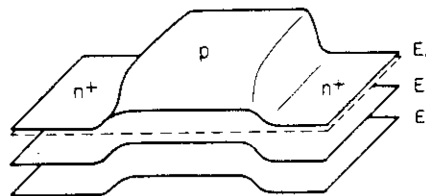
Two-dimensional band diagram of an n-channel MOSFET



Device configuration (n-channel, p-type substrate)



Flat-band equilibrium condition



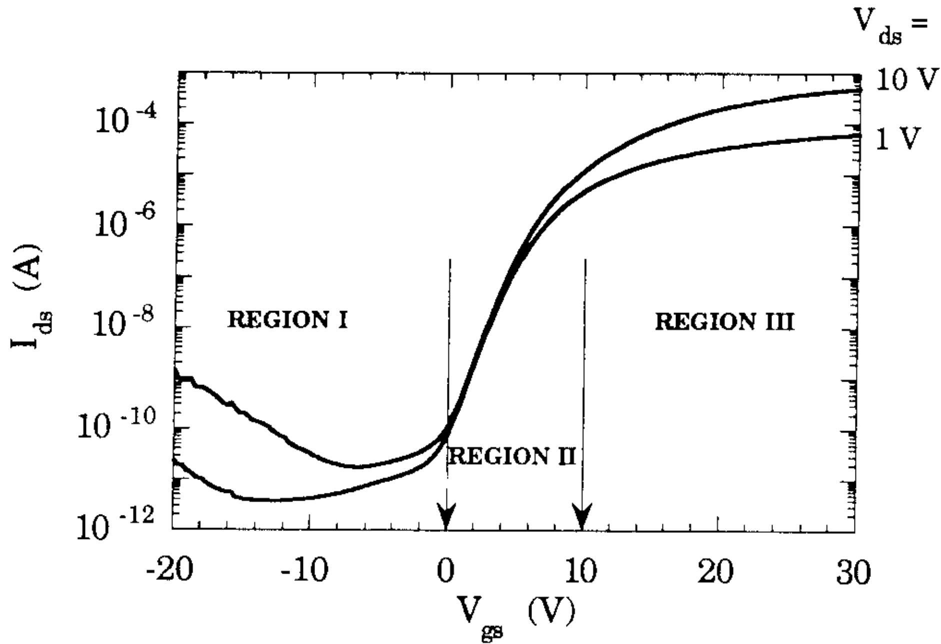
Positive gate-bias regime

Sze,Physics of semiconductor devices

particular of poly-Si MOSFET → channel undoped
→ electrically active defects which render gate control less efficient

transfer characteristics : $I_{ds} = f(V_{gs})$ for fixed V_{ds}

for an n-channel poly-Si MOSFET



REGION I : **the off-state region**

leakage current density (pA / µm of channel width)

REGION II : **the transition region**

subthreshold slope (V / dec)

REGION III : **the on-state region**

threshold voltage (V) and carrier mobility (V/cm^2 s)

all of these TFT characteristics are influenced by the presence of defects in the poly-Si active layer

Region II : the transition regime

using the same processing sequences, but starting from SOI material, give a subthreshold slope value of 0,1 V/dec.
→ defects in the poly-Si channel

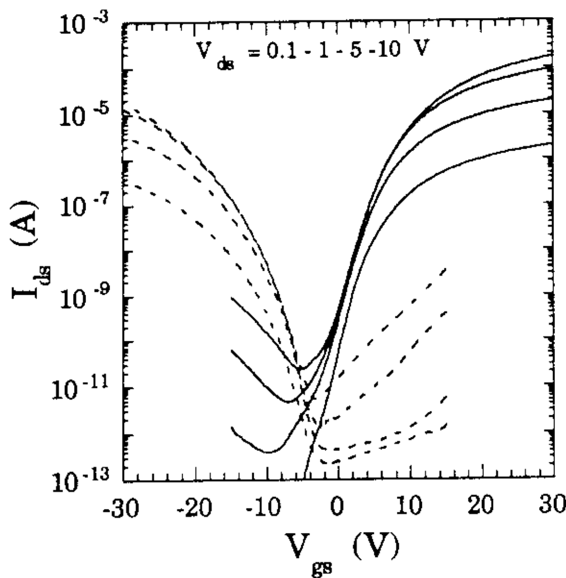
in SOI $S = S_0 (1 + C_{it}/C_{ox} + C_d/C_{ox}) \approx S_0$

where S_0 is a constant 65 mV/dec
C_{ox} : gate oxide capacitance
C_d : channel depletion capacitance
C_{it} : interface traps capacitance

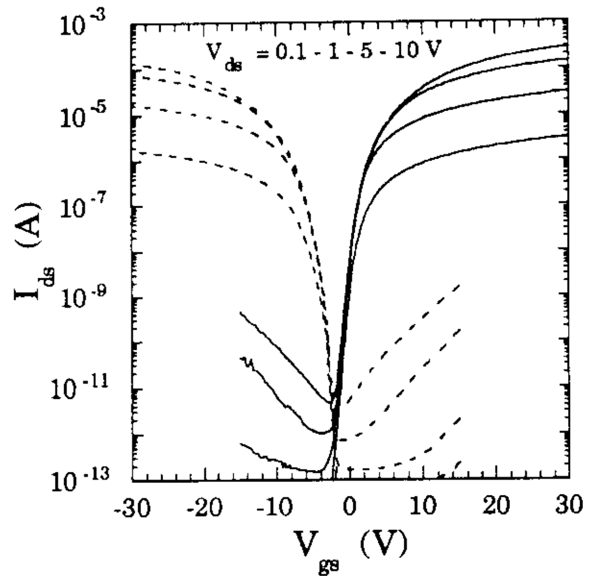
in poly-Si $S \approx S_0 (1 + C_t/C_{ox}) >> S_0$

where Ct : poly-Si traps capacitance (interface and bulk)

changing of crystallisation technique can greatly affect the S values (same processing)



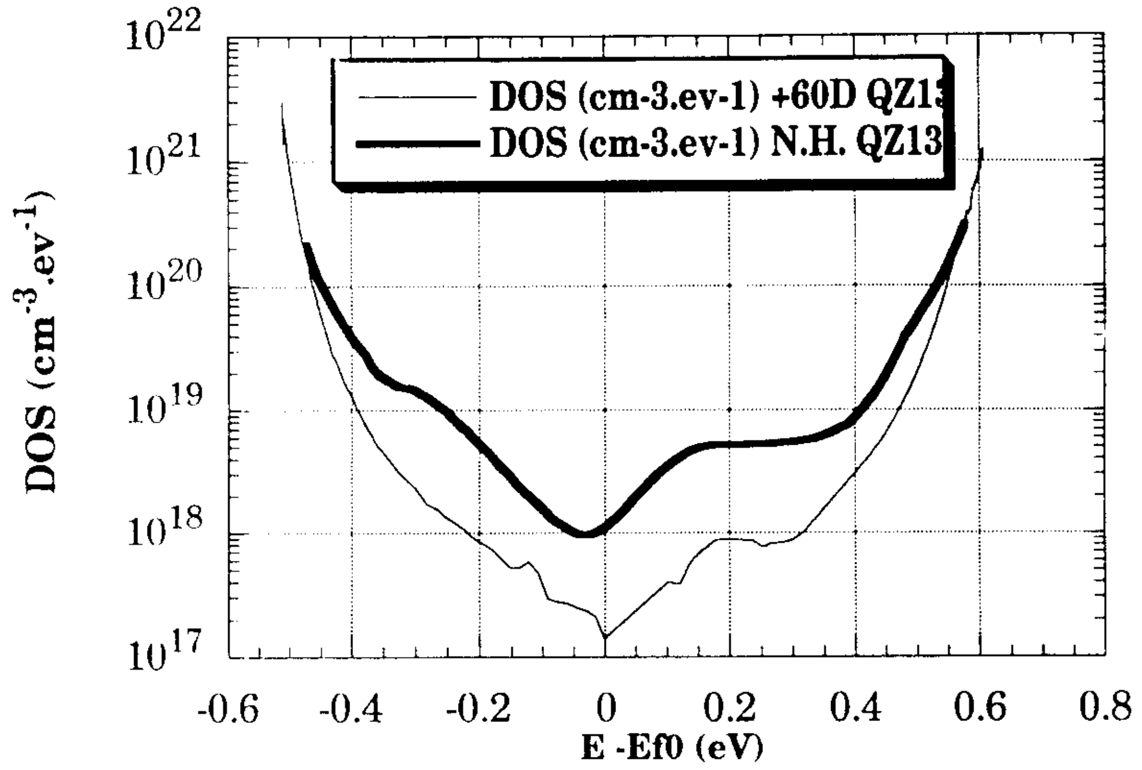
Transfer characteristics of TFTs fabricated using SPC (65h at 580°C).



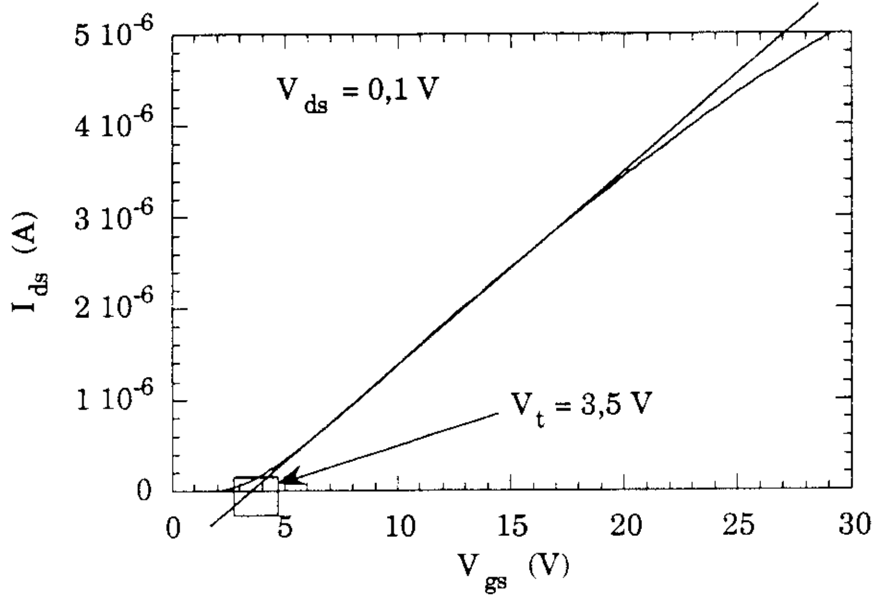
Transfer characteristics of TFTs fabricated using laser crystallisation (T=250°C, 220mJ cm^{-2}, SiO_2 coating).

Electrically active defects originate from cristalline defects in the poly-Si channel. Models involve a homogeneous concentration in the layer as grain size is usually much smaller than the debye length.

The density of states (DOS) in the band-gap of the poly-Si can be dramatically reduced by post fabrication hydrogenation treatment



Region III : the on-state region



Determination of threshold voltage from transfer characteristic (linear plot, linear regime).

In the linear regime (V_{ds} = 0,1 V)

$$I_{ds} = (W/L)\, \mu\, C_{ox}\, (V_{gs} - V_t)\, V_{ds}$$

μ is deduced from the slope of the linear transfer characteristics in that particular case, μ = 80 $cm^2\ V^{-1}\ s^{-1}$

Region I : the off-state region

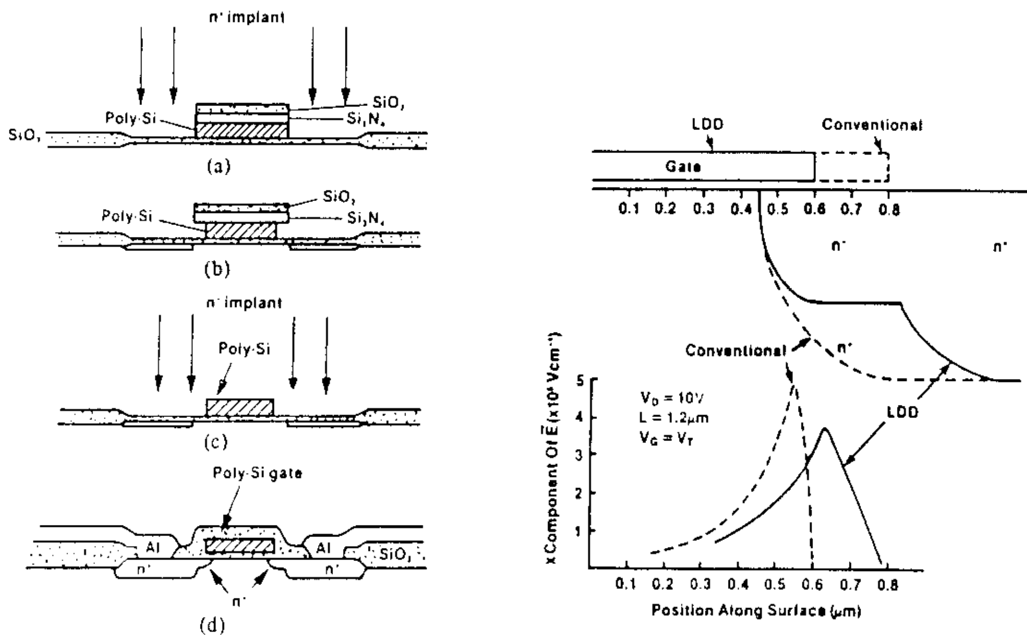
exponential dependence of leakage current on gate and drain biases (for high drain and gate biases

origin : high electrical field at the reverse-bias drain junction

high voltages and abrupt junction (self-alignment by implantation)

(also present in monocrystalline transistors)

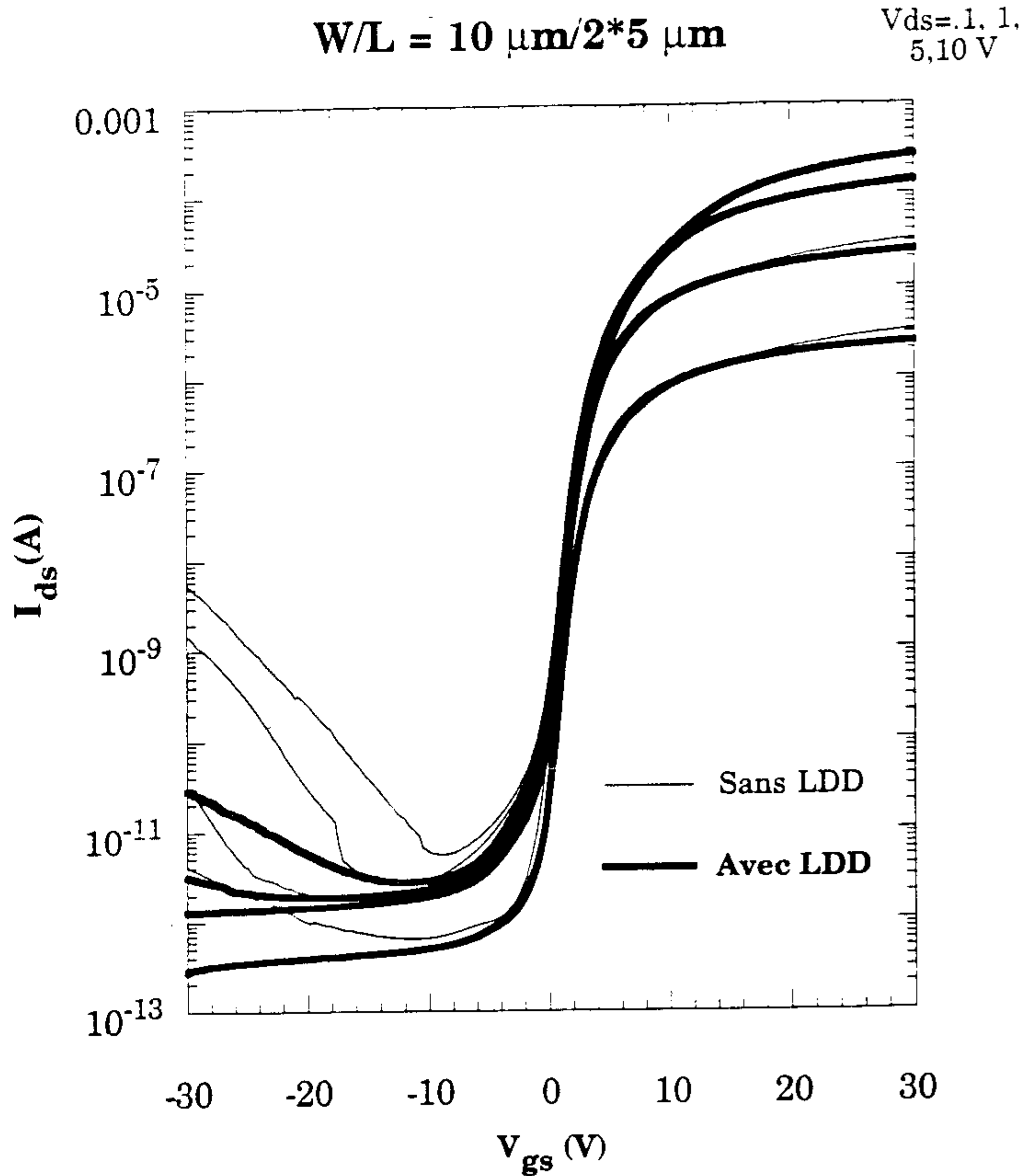
Control of leakage current is achieved by drain engineering (Lightly Doped Drain)



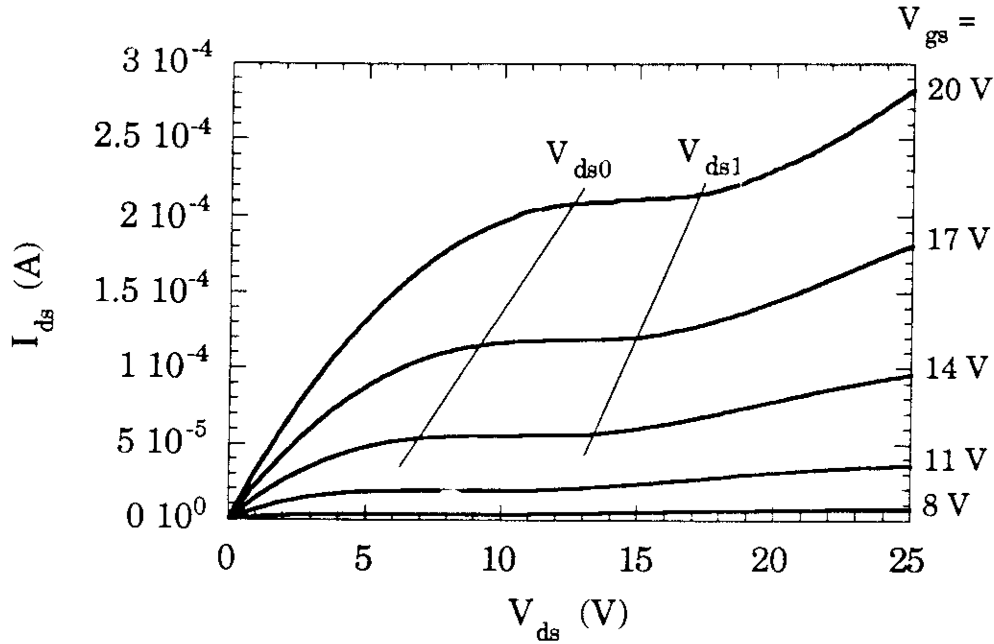
Ogura, IEEE TED (1980) 1359

Dramatic reduction of the off-current in poly-Si TFTs with the use of an LDD region

(extension 0,8 μm dose 2 $10^{13}cm^{-2}$)



output characteristics : $I_{ds} = f(V_{ds})$ for fixed V_{gs}



$V_{ds} > V_{ds0}$ (V_{ds0} depends on V_{gs})

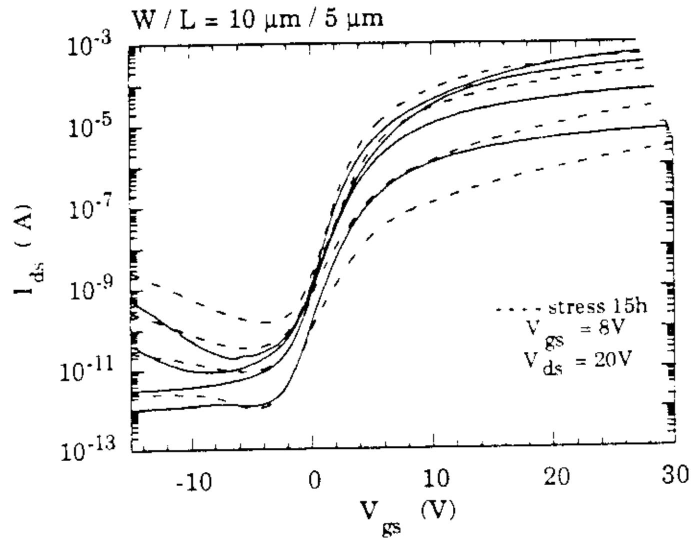
→ **saturation regime** (after the pinch-off point)

for a fixed V_{gs}, as V_{ds} increases, V_{gd} decreases : the pinch-off point is the point for which the channel depth is reduced to zero.

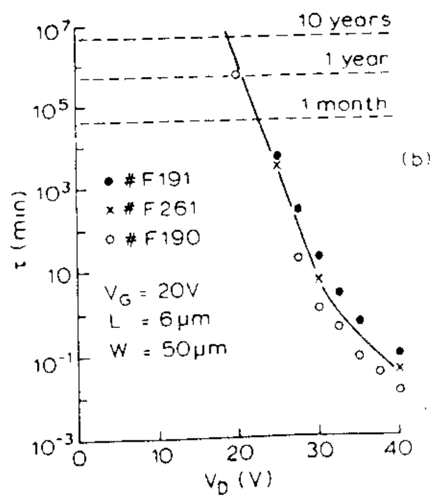
for Vds > Vds1 (Vds1 depends on Vgs)

→ **breakdown regime** due to impact ionization

working in or near the breakdown regime affect the device stability

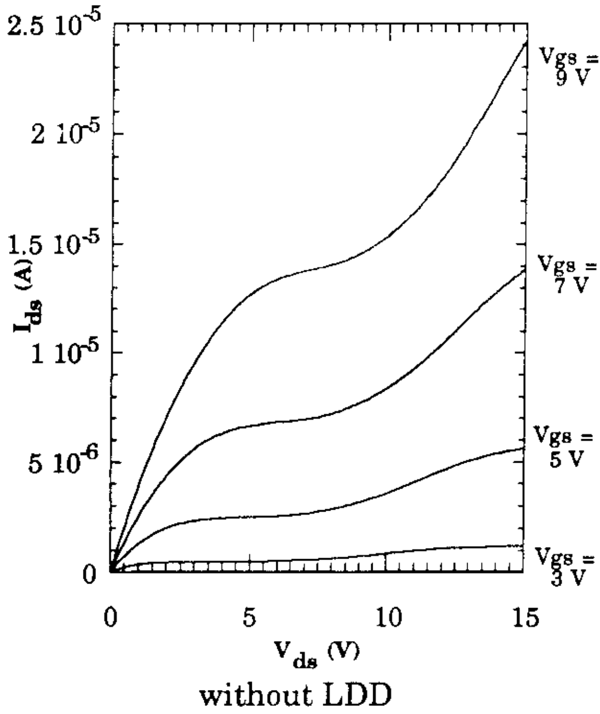


Reduction of the TFT on current by a dc bias stress in the breakdown regime

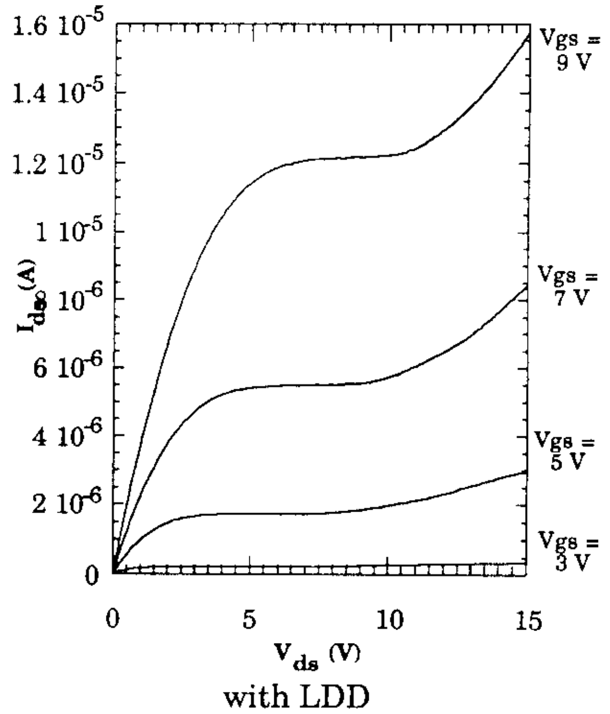


poly-Si TFT lifetime (reduction of on current by 30%)
as a function of drain voltage (Young SST 7 (1992) 1183).

LDD structures : the saturation regime is better defined.

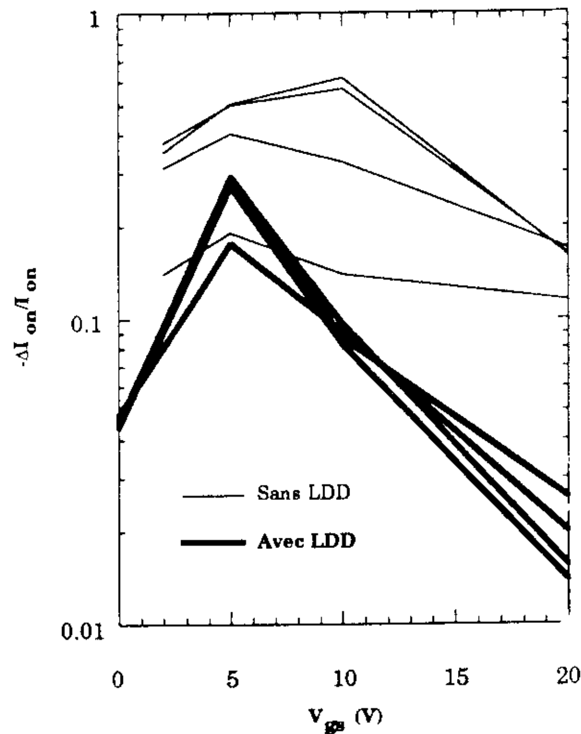


without LDD



with LDD

LDD structures improve the stability



Relative loss of on current as a function of Vg during stress, for structures with and without LDD

One can define a characteristic time, for a certain design :

$$\tau_P = \frac{L(L+L_{ov})}{\mu(V_{dd}-V_{ss}-V_{th})}$$

where

L : gate length
L_{ov} : gate-drain overlap

μ : mobility

V_{dd} - V_{ss} : supply voltage
V_{th} : threshold voltage

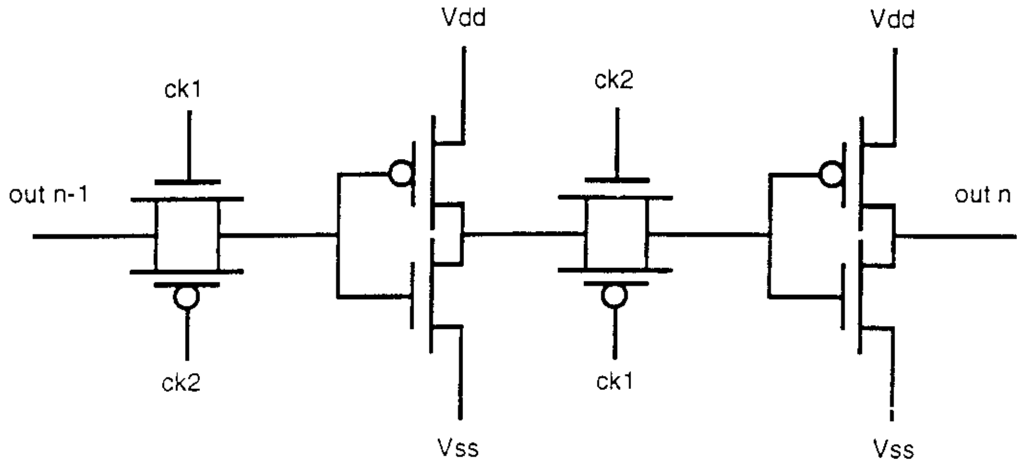
<u>time delay propagation of an inverter</u>

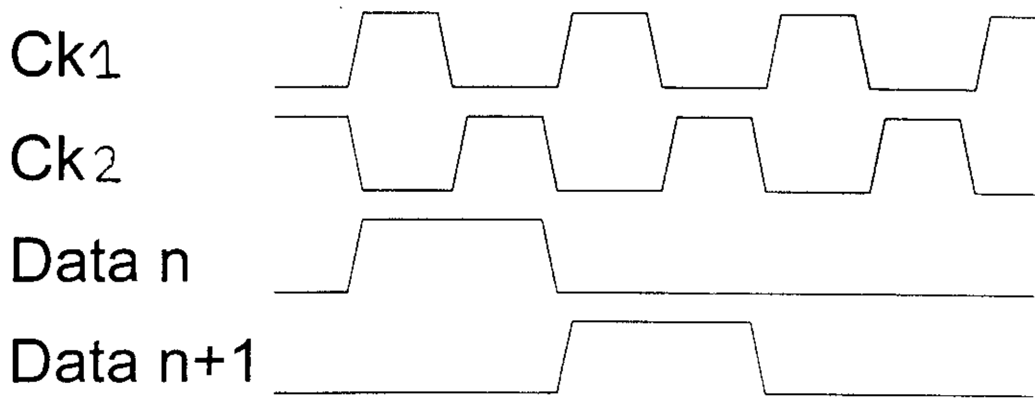
$\alpha\, t_p = 30\, t_p$

$L = 10\ \mu m$, $\mu = 50\ cm^2\ V^{-1}\ s^{-1}$, $V_{dd}-V_{ss}-V_t = 10\ V$

f_{max} (register) = $1 / 30\ t_p$ = 15 MHz

CMOS dynamic shift register





CMOS design improve circuit performances (Edwards, IEE CDS 141 (1994))

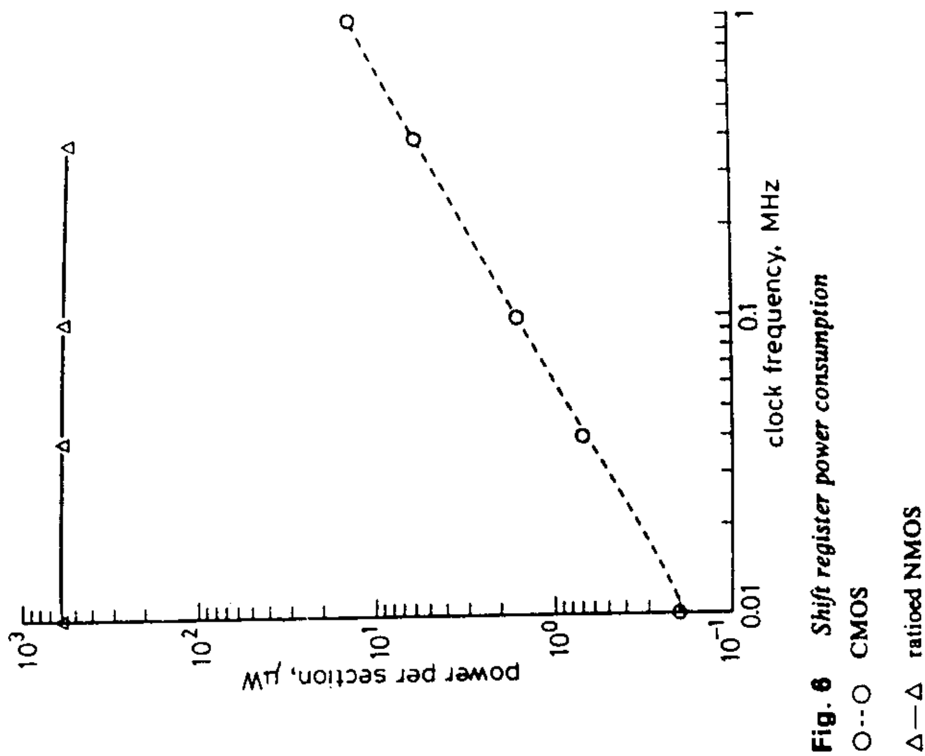


Fig. 6 *Shift register power consumption*
O--O CMOS
Δ—Δ ratioed NMOS

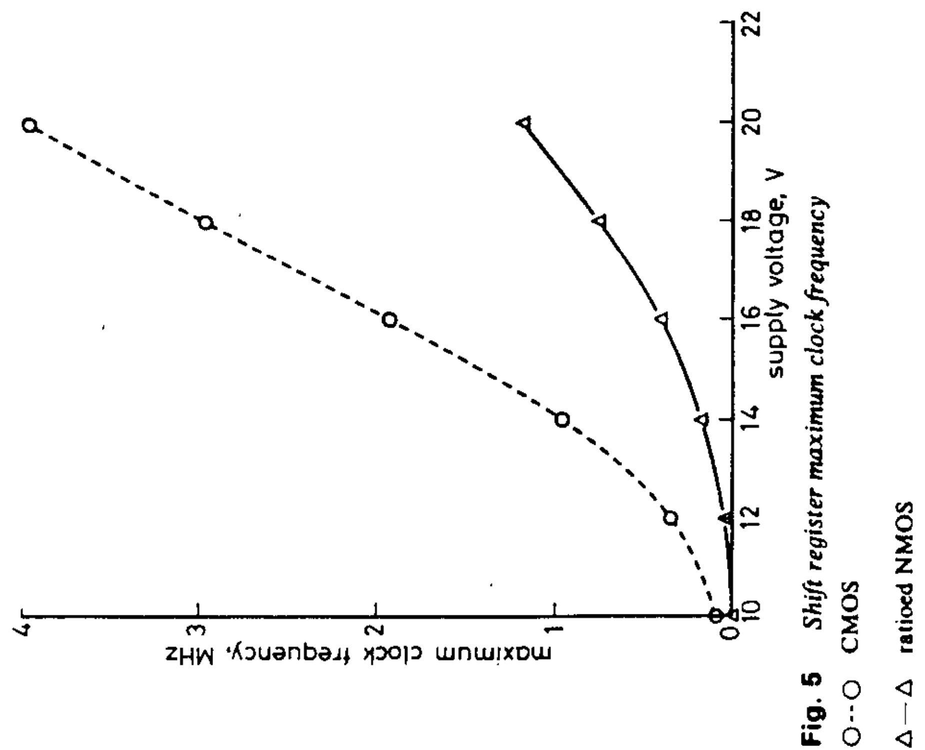
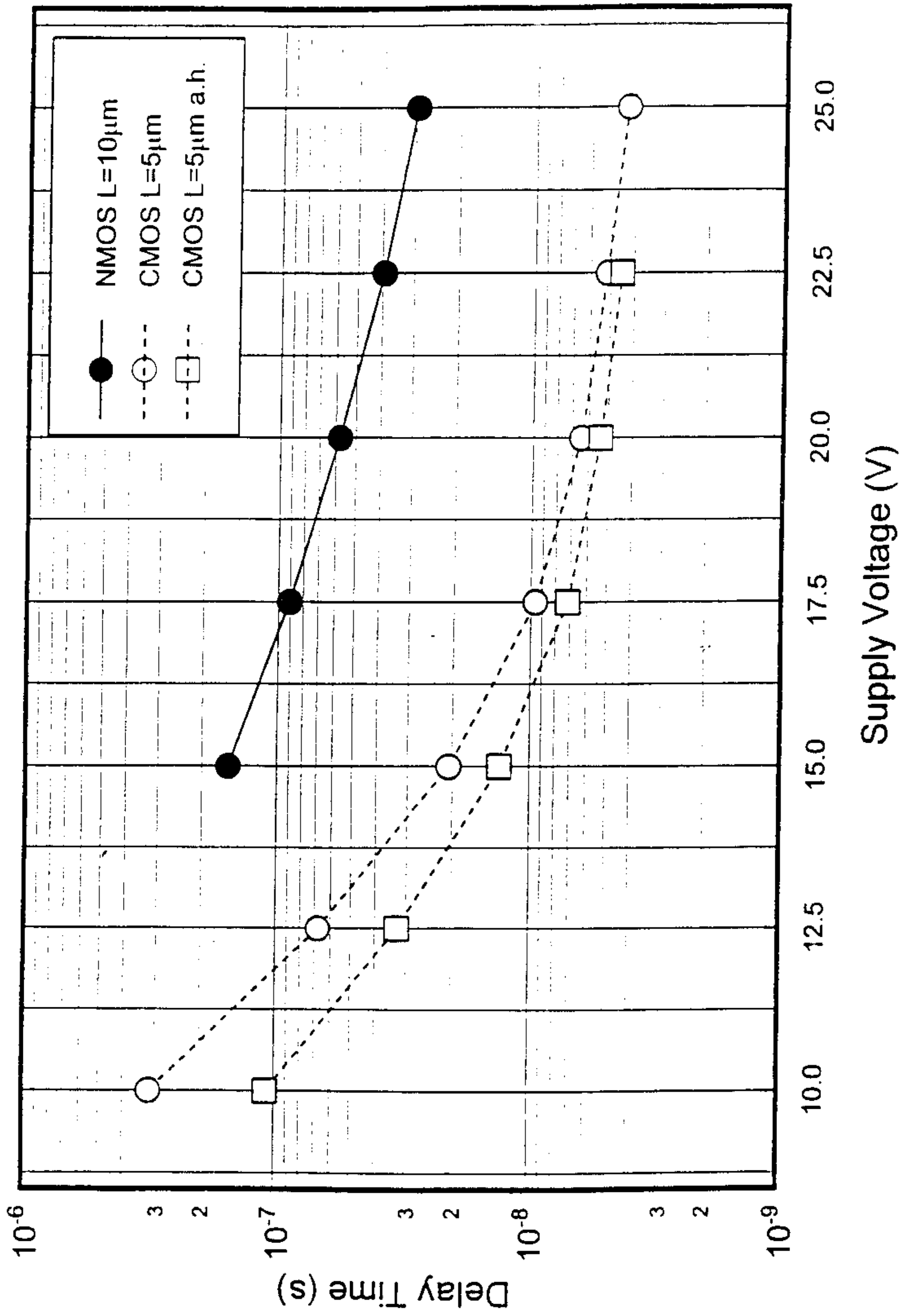


Fig. 5 *Shift register maximum clock frequency*
O--O CMOS
Δ—Δ ratioed NMOS

CMOS design improve circuit performances



CMOS design permit complex circuit operation

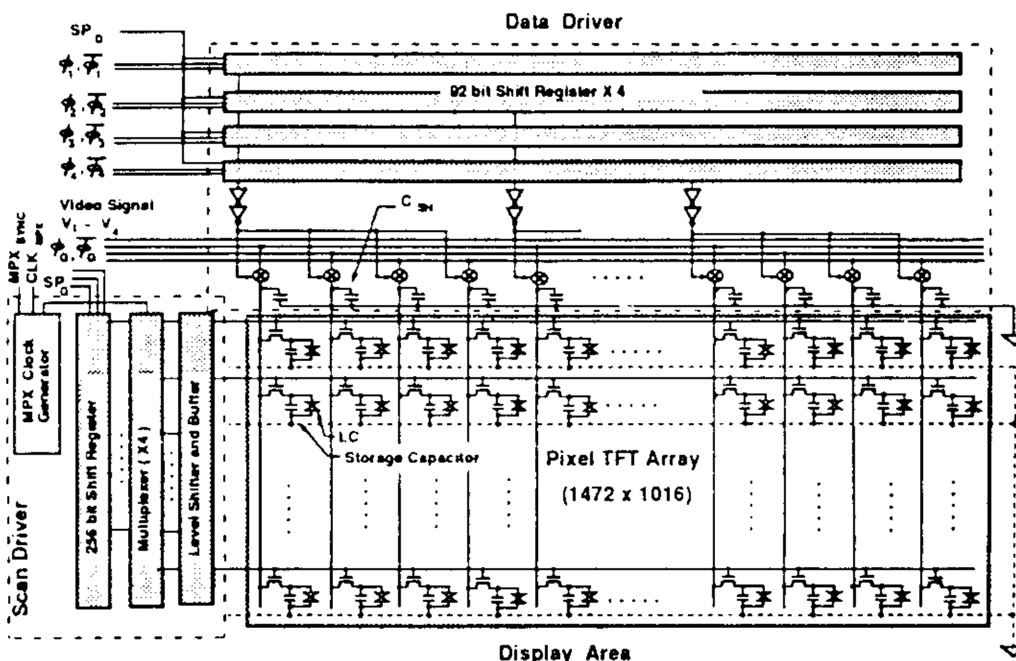


Figure 27 : Block diagram of poly-Si AMLCD for HDTV projector with integrated drivers. Clock frequency for data drivers is 1.8 MHz.