UNITED NATIONS EDUCATIONAL, SCIENTIFIC AND CULTURAL ORGANIZATION
INTERNATIONAL ATOMIC ENERGY AGENCY
INTERNATIONAL CENTRE FOR THEORETICAL PHYSICS

SMR/917 - 31

SECOND WORKSHOP ON
SCIENCE AND TECHNOLOGY OF THIN FILMS

(11 - 29 March 1996)

" Thin films for large area electronics "

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Thin films for large area electronics

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Abstract

In this chapter, the use of thin films for the fabrication of active devices and electronic circuits on large area, non refractory substrates is presented. Today, the major application of such films is in the field of active matrix for liquid crystal displays (AMLCDs), used for instance in portable computers. More than two million full-colour AMLCDs were produced in Japan in 1993 and the favorite material employed for their fabrication is hydrogenated amorphous silicon.

The first part of the chapter presents the various material aspects of the now mature amorphous silicon technology, based on the use of thin films of hydrogenated amorphous silicon, in intrinsic or doped forms, in association with insulators such as silicon nitride or silicon dioxide. Most of the thin film transistors and diodes which are manufactured today make extensive use of this technology. However, some instability problems exist, which are briefly described. Various applications are presented, including AMLCDs and image sensors. A special paragraph is devoted to the industry of AMLCDs since it is following a growth curve that closely resembles the one we have already witnessed for the integrated circuits industry.

In the second part, we present recent developments in the use of thin films of polycrystalline silicon, which exhibits much better transport properties. The various methods used to obtain the polysilicon films are described, together with the ones allowing the synthesis of the high quality gate dielectric materials which are necessary to realise good MOS devices and circuits. We also deal with the instability problem, which manifests itself differently in polysilicon transistors. Finally, given the performances of some recent devices and circuits some new fields of applications are outlined, in non-display areas.

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1. Introduction

Large-area electronics can be defined as the fabrication of electronic devices and circuits on large-area, non-refractory and chemically-stable substrates. The basic idea (or rather challenge) behind large-area electronics is to reproduce in thin films of semiconductors and dielectrics most of the physical properties which are necessary to make an electronic device work. So far, the major domain of application of large-area electronics has been in peripherals, i.e. in systems or components which allow us to communicate with electronic chips. In particular, the development of large-area electronics has been driven by the spectacular explosion of flat panel displays, and the prototype example of a large-area electronics product is the active matrix which is used in liquid crystal displays to switch the picture elements (pixels) that control light transmission through the display.

Although the idea had been around for some time [1], large-area electronics was probably born in 1975 when Spear and Le Comber from the University of Dundee demonstrated that the conductivity of hydrogenated amorphous silicon (a-Si:H) could be controlled over more than 8 orders of magnitude by doping [2]. The first a-Si:H thin film transistor (TFT) soon followed, together with the suggestion that such a device could be used as an electronic switch in an active matrix liquid crystal display (AMLCD) [3].

Since then, hundreds of millions of man-hours of research and development and a comparable amount of dollars (or rather their yen counterpart) have brought the a-Si:H technology and the AMLCD industry to a mature stage; according to some analysts, Japanese companies have so far invested about $3 billion in flat panel display development and manufacturing (with a large share in AMLCDs), and more than two million full-colour AMLCDs for portable computers were produced in Japan in 1993 [4]. It is predicted that by 1996, AMLCDs will account for 60% of the high information content (HIC) flat panel display market.

At the confines of silicon integrated circuits technology, polysilicon is currently being increasingly studied and employed, because of its superior transport properties over a-Si:H. Around the world, research laboratories are producing breathtaking results concerning carrier mobilities in laser-crystallised polysilicon films. Values as high as 600 $cm^2V^{-1}s^{-1}$ have been recently published, which compares with the ones currently obtained in monocrystalline silicon on insulator (SOI) material. Furthermore, polysilicon can produce n- and p-type devices, which opens up the possibility of realising complementary metal-oxide-semiconductor (CMOS) circuits. Although the original driving force for polysilicon development was the integration of the various addressing circuits of AMLCDs at the periphery of the glass plates, its next domain of application could well be in rapid circuitry, in competition with SOI, as polysilicon material and device features are increasingly being compared to monocrystalline silicon, rather than to hydrogenated amorphous silicon.

So once again, because of its relative simplicity compared to some contenders like CdSe for instance [1], silicon (even if non-monocrystalline, and thanks to hydrogen) appears to be the corner-stone of a new branch of the electronics industry.

This chapter is essentially divided into two parts; the first one deals with amorphous silicon material and technology, whereas the second is devoted to the various aspects of polysilicon features and fabrication techniques. In each part, we first describe materials' properties (including those of the essential gate insulators), in connection with the methods or processes used for their synthesis. We then present the basic TFT structures and characteristics and finally the major industrial applications, either present or potential.

2. Amorphous silicon thin films for large area electronics

2.1. a-Si:H material properties

2.1.1 Structure and density of states

As outlined in the introduction, amorphous silicon (a-Si) and hydrogenated amorphous silicon (a-Si:H) have been studied for more than two decades. Numerous papers and several books [5-7] have been published on the various aspects of growth, doping and structure of a-Si and a-Si:H, the resulting band structure of the materials and their density of electronic states. Concerning a-Si:H, the physics of various hetero-junctions has been investigated (in particular insulators / a-Si:H structures) and the feasibility of a number of devices has been demonstrated, including the most important for large area electronics, namely the thin film field effect transistor.

The structure of amorphous silicon can be described by a continuous random network (CRN) model in which covalent bonding is preserved [8,9]. This means that, compared to crystalline silicon (c-Si), there is no long range order in the amorphous solid, i.e., no translational symmetry, but locally, the coordination is on average the same, each silicon atom having four nearest neighbours, as in c-Si. However, a number of coordination defects are present in a-Si, corresponding to atoms with too many or too few bonds. The precise concentration of such defects depends on the particular method used to grow the a-Si material. The structural state of a-Si is essentially characterised by a tetrahedral bond-angle distortion, and there is practically no bond stretching [10]. This view is supported by the fact that the stored strain energy associated with a bond angle distortion of rms value around 10° (the actual value for a-Si) is comparable to the heat of crystallisation of a-Si [11].

Because the basic tetrahedral structure of a-Si is very similar to the one of c-Si (short range order), amorphous silicon is indeed a semiconductor [12], with a forbidden energy gap. However, the band edges are not abrupt as in c-Si, since the structural disorder of the CRN (bond-angle distortion) induces conduction and valence band tails which extend into the forbidden gap. Furthermore, the coordination defects (mainly threefold- coordinated

atoms which introduce unsatisfied bonds, called dangling bonds but also five-fold-coordinated ones representing floating bonds) give rise to deep levels around mid-gap.

Figure 1 schematically shows the distribution of the density of states in a-Si. The tail as well as the deep states (corresponding respectively to bonding disorder and coordination defects) are localised, which means that in these states the wave functions associated with electrons are confined to a small volume of semiconductor around particular defects, due to strong interaction potentials. In the conduction and valence bands, the states are considered as extended, but they are not Bloch states as in c-Si, because of the lack of periodicity of the amorphous solid. The transition from localised to extended states occurs at E_C for the conduction band and E_V for the valence band [13]. E_C and E_V are called the mobility edges, because at T = 0 K, the carrier mobilities go to zero below E_C and above E_V, even though the wave function of neighbouring states overlaps [13]. The quantity $E_g = E_C - E_V$ is called the mobility gap and it usually amounts to 1.7eV in hydrogenated material.

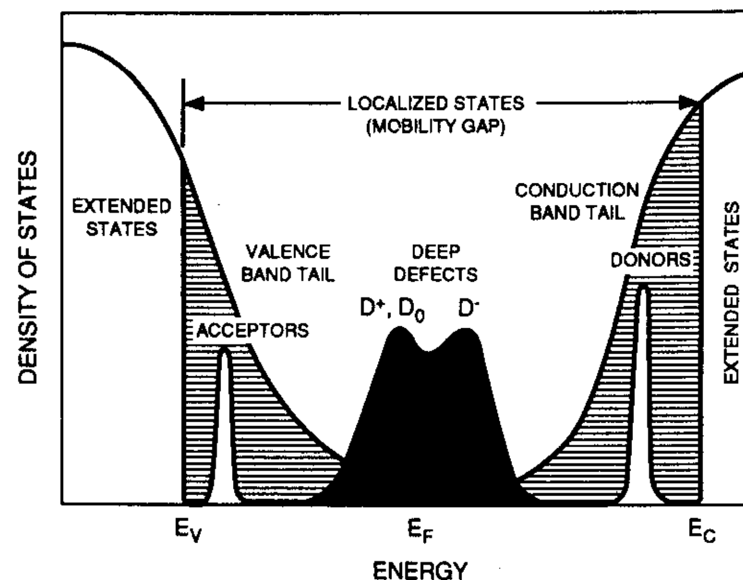


Figure 1 : The density of states in amorphous silicon. Bonding disorder induces conduction and valence band tails, whereas dangling bonds form states aroung mid-gap.

It is generally agreed that the density of tail states falls off exponentially from the mobility edges with characteristic slopes T_c (250-300K) and T_v (400-450K) [14]; the corresponding expressions are:

$N_c(E) = N_o \exp(E-E_c) / kT_c$, and

$$N_v(E) = N_o \exp (E_v-E) / kT_v$$

with $N_o = 10^{21}$ cm^{-3} eV^{-1}.

Dangling bonds are thought to be the major source of deep levels. A dangling bond can exhibit different charge states: it is positively charged when unoccupied (D^+), neutral when occupied by an electron (D^o), and negatively charged when occupied by two electrons with anti-parallel spins (D^-). In this latter case, the electronic level in the gap is shifted by the correlation energy (U ~ 0.4 eV) which corresponds to the repulsive Coulomb interaction between the two electrons. Hence, the energy levels associated with dangling bonds are spread over an appreciable energy range in the middle of the gap. The position of the Fermi level in undoped material adjusts itself around mid-gap in such a way as to preserve electrical neutrality (0.7-0.8 eV below the mobility edge of the conduction band depending on defect concentration). In pure amorphous silicon, the concentration of dangling bonds and associated deep traps is so high that the material cannot be used for device fabrication. Actually, the density of dangling bonds (D^o) as determined by electron spin resonance measurements can be of the order of 10^{19} cm^{-3} [15] and even over.

The incorporation of atomic hydrogen into a-Si has essentially two effects. First, hydrogen "cleans" the gap, by saturating most dangling bonds, thus creating stable Si-H covalent bonds. Second, atomic hydrogen breaks the highly strained or unstable Si-Si bonds, leading to either Si-H bonding or reconstructed strong Si-Si bonds. Consequently, the density of deep states can be reduced below 10^{15} cm^{-3} and the density of tail states can also be reduced and sharpened for an optimised growth process, in which atomic hydrogen is produced and introduced in the amorphous solid during growth. The effect of hydrogen on the density of states of a-Si was clearly demonstrated by Madan and coworkers twenty years ago [16].

2.1.2 Growth and doping

Although a-Si:H can be obtained by thermal evaporation or sputtering, followed by plasma hydrogenation [17], the most popular method used to prepare good quality a-Si:H films is the so-called plasma enhanced chemical vapour deposition (PECVD) process [18], whereby silane gas (SiH_4) is decomposed at low temperature in a low pressure radiofrequency plasma. Schematically, the SiH_n ($n < 4$) radicals which are formed in the plasma adsorb on the surface of the growing film and depending on their reactivity, i. e., on the value of n, they can either diffuse laterally to an available surface dangling bond or locally displace an hydrogen atom already bonded to the amorphous silicon network; the resulting texture of the film can be respectively dense or columnar. The best films, in terms of electrical properties, are the ones exhibiting the dense texture, and such films are obtained when SiH_4 is undiluted, at a pressure around 0.5 Torr, a substrate temperature around 250°C and with a low RF power (see e. g. [6], chapter 2); they contain typically around 10% of hydrogen (5.10^{21} cm^{-3}), which is about two orders of magnitude higher than the density of dangling bonds in non-hydrogenated material [15]. Infra-red absorption measurements show that most of this hydrogen is bonded (mainly Si-H bonds

for a material of good electrical quality), an observation which supports the view that hydrogen not only passivates dangling bonds, but also interacts with the silicon network, by breaking weak (strained) Si-Si bonds, thus "refining" the amorphous material. Another typical structural feature of a-Si:H is the existence of voids in the solid (even in the optimised dense one), with dimensions which can be reduced down to 0.5-1 nm for PECVD-prepared material. The surface of the voids is passivated by hydrogen (Si-H or $Si-H_2$ bonds), and the void density is a function of the precise deposition conditions.

As quoted in the introduction, doping of a-Si:H was first demonstrated in 1975 by the Dundee group [2] and Figure 2 reproduces the latter's historic curve on the conductivity of a-Si:H as a function of the fraction of phosphine or diborane in the gas phase.

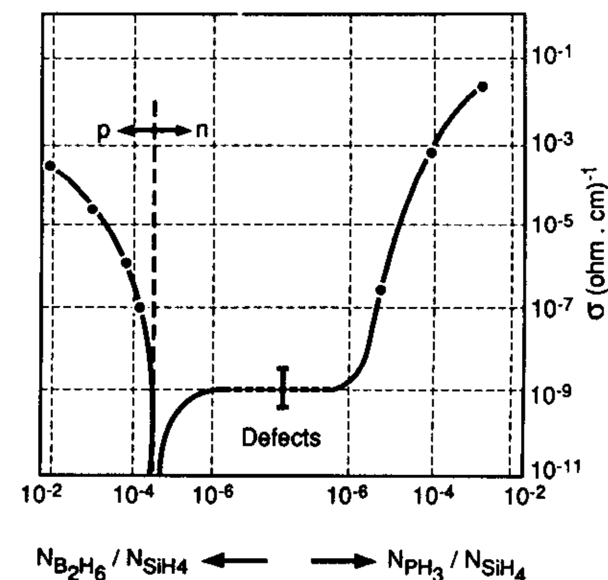
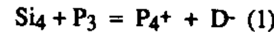


Figure 2 : Room temperature conductivity of a-Si:H as a function of the fraction of diborane or phosphine in the gas mixture feeding the deposition plasma (after Spear and Le Comber, [2])

As far as PECVD is concerned, doping is performed by controlling the addition of phosphine (PH_3) or diborane (B_2H_6) to the SiH_4 growth nutrient which is fed into the deposition plasma. The PH_3 or B_2H_6 molecules are decomposed into radicals by the RF deposition plasma, in much the same way as is SiH_4. The resulting radicals adsorb on the surface dangling bonds of the film, leading to "substitutional" dopant incorporation into the amorphous solid. Although this result comes as no surprise to anybody familiar with crystalline semiconductors, it represented an important breakthrough, since early attempts to dope amorphous semiconductors had been unsuccessful and it had been suggested that such a doping was impossible [19], because in a continuous random network, the

coordination of an atom adjusts itself so that all the bonding and lone pair states are fully occupied and the anti-bonding states are empty [20]. For P or B to be active dopants in a-Si:H, they must be four-fold-coordinated, whereas due to the above considerations on the energetics of bonding, they are only three-fold-coordinated, as in PH_3 or B_2H_6 for instance.

Nevertheless, it has been shown (see [6], chapters 5 and 6) that when ionised impurities such as e.g., B^- or P^+ (which, because of their charge states become four-fold-coordinated) are taken into consideration and associated with a charged dangling bond (respectively D^+ and D^-) the energy departure from the ideal random amorphous network is small. Thus, because of this low energy dopant-defect pair formation, a small fraction of the incorporated dopants can become four-fold-coordinated and hence electrically active. In other words, if for instance we consider the situation for phosphorous, the following equilibrium can be written :



$$Si_4 + P_3 = P_4^+ + D^- \quad (1)$$

where the subscripts refer to the coordination numbers. Since the formation of the (P_4^+, D^-) pair costs energy and the defects act as compensation centers, the doping efficiency is small : typically between 1 and 10% of the actual impurity content of the amorphous solid at low dopant (P or B) concentrations, dropping to 0.1% at high doping levels. For such high doping levels (typically around a few 10^{20} cm^{-3}), the minimum resistivity of a n^+ film is around 10^2 Ω.cm, i. e., more than 5 orders of magnitude greater than the one of mono or polycrystalline layers of similar dopings.

2.2. a-Si:H thin film transistors

Thin film transistors (TFTs) are field effect devices, and as such, their operating principle relies on the controlled modulation of the space charge in a semiconductor channel region which is inserted between doped contacts representing the source and drain regions. The oldest and probably most studied field effect device is the metal oxide semiconductor field effect transistor (MOSFET), well known to anybody in the electronics industry. In the MOS transistor, the control of the charge sheet in the channel is performed by the electric field which is induced in the semiconductor surface region by the capacitive coupling of the gate electrode through the gate oxide [21]. A-Si:H thin film transistors operate similarly, although the gate insulator is not necessarily silicon dioxide and there are some differences in behaviour due to the existence of the localised states in a-Si:H material.

Figure 3 shows typical TFT structures; the inverted staggered or bottom-gate one, (figure 3-a) i.e. the one with the gate electrode located underneath the channel, is the most commonly used, because when silicon nitride (SiN_x) is used as a gate dielectric (most common case as well), the a-Si:H / SiN_x interface is of better electrical quality [22]. The top gate structure (figure 3-b) has also been studied and developed, essentially for AMLCD applications; although low mobility values are anticipated, its advantage mainly relies on the fact that only two masking steps are necessary to fabricate an active panel [23]. The transistors shown in figure 3 are n-channel devices and they operate in the accumulation

mode. Inversion-mode devices cannot be used in practice, because due to the large defect density and associated deep levels induced by doping (see Eq. 1 above for n-type doping), a too large gate voltage would be needed to deplete, for instance, a n-doped channel region and appreciably move the Fermi level towards the intrinsic level around midgap.

In the off state, for moderate negative gate voltages (still for an n-channel device), the Fermi level is still pinned around mid-gap or slightly below, again because of the deep states and also because the tail states in the lower half of the band gap are not in thermal equilibrium with the extended states of the valence band (T_v ~ 400-450 K). Consequently, the current flow is inhibited by the large resistivity of the intrinsic a-Si:H material (see figure 2) rather than by the formation of a reverse biased p-n+ junction at the channel / drain interface. Typical values of leakage currents are of the order of a few 10^{-15} A per micron of width of the channel of the TFT, for a drain voltage of 10V.

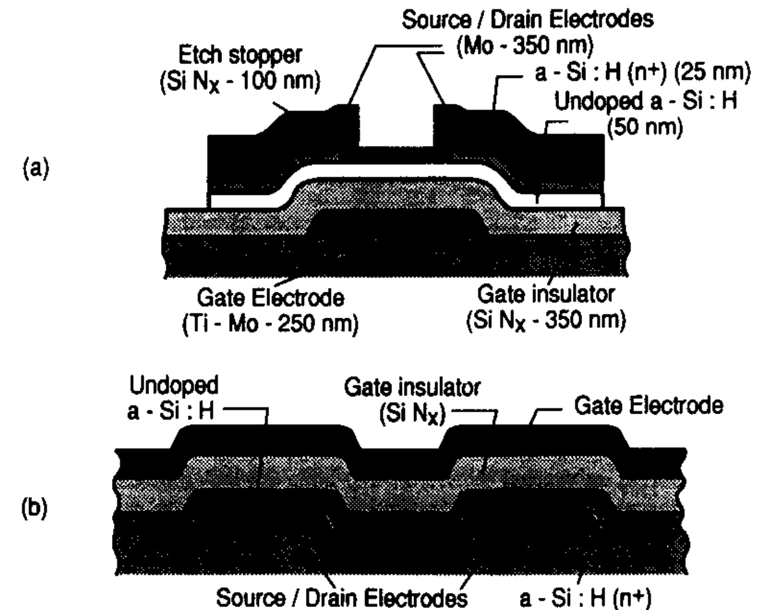


Figure 3 : Typical structures of a-Si:H Thin Film Transistors, (a) the inverted staggered structures, (b) the top-gate structures.

Figure 4 shows the band diagram and band alignment corresponding to the SiN_x / a-Si:H heterojunction, which is the most widely used to control the channel conduction of a-Si:H TFTs. The band offsets have been set in agreement with the values reported in the literature [24]. The band bending at the interface, due essentially to the density of interface states, depends on the deposition conditions and also on the order in which the SiN_x and

a-Si:H films are deposited [22]. In any case, the surface of the semiconductor is slightly accumulated, which implies that the flat band voltage is negative.

As a positive voltage is applied on the gate, a mirror charge is induced in the amorphous silicon; the bands start to bend downwards in the semiconductor surface region and the deep levels see their position move below the Fermi level. As a consequence, most of the induced charge becomes trapped in the deep levels which, in the upper half of the bandgap, behave as acceptors. As the gate voltage is made larger, the Fermi level at the interface rises and an increasing fraction of the deep levels is filled. For a certain gate voltage, the Fermi level enters the tail states, and since T_c, the characteristic temperature of the conduction band tail is of the order or below room temperature (see § 2.1.), most of the additionally induced charge is now located above the Fermi level [25]. Moreover, as the corresponding slope of the tail states is steep (kT_c of the order of 20-25 meV), these states behave as a single trapping level situated at E_t below the conduction band edge.

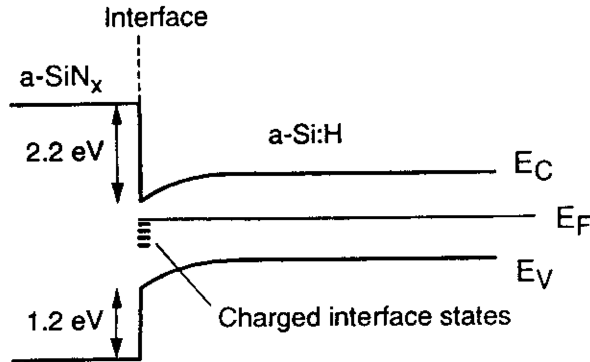


Figure 4 : Band structure of the a-Si:H / SiNx interface, showing the band offsets. The band bending in the a-Si:H surface region is due to charged interface states.

The transport in the channel is therefore trap-limited, which means that the drift of the carriers under the source-drain electric field is controlled by successive trapping and reemission between E_t and the extended states above the conduction band edge. As a consequence, the field-effect mobility is reduced from the extended state value of 10-15 $cm^2\ V^{-1}\ s^{-1}$ to 0.2-1 $cm^2\ V^{-1}\ s^{-1}$ and it is thermally activated, with an activation energy E_c-E_t of the order of 0.17 eV [26]. Figure 5 shows typical transfer characteristics for a n-type inverted staggered a-Si:H TFT with a structure similar to the one of figure 3-a.

The threshold voltage of the device can be defined as the voltage at which the Fermi level starts to enter into the tail states of the conduction band [25-26]. It is clear that the physical phenomenon which gives rise to the threshold voltage is completely different from the single crystal MOS situation.

The derivation of the current-voltage characteristics can be performed in much the same way as for the crystalline MOSFET. The charge induced in the conduction band tail can be expressed as :

$$Q(x) = C_g [V_g - V_t - V(x)] \quad (2)$$

where V_g is the gate voltage, V_t the threshold voltage, V(x) the additional voltage induced by the drain at a distance x from the source, along the channel and C_g is the gate insulator capacitance per unit area. The channel resistance of an elemental section dx is :

$$dR = dx / W\mu_{fe}Q(x) \quad (3)$$

where W is the channel width of the TFT and μ_{fe} is the field effect mobility.

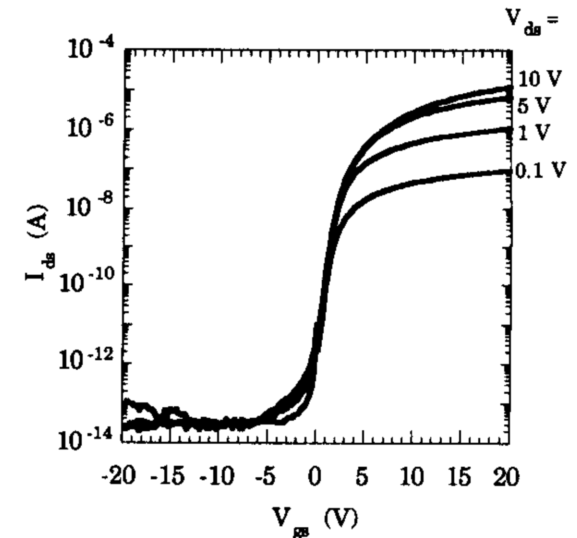


Figure 5 : Typical transfer characteristics of an inverted staggered a-Si:H TFT; channel width = 28 µm and gate length = 5 µm. (courtesy of Thomson LCD).

On the other hand, the voltage drop across this elemental section is:

$$dV(x) = I_{ds}.dR \quad (4)$$

where I_{ds} is the drain current which does not depend on x. After combining the three above expressions, separating variables and integrating between the source (x = 0, V(x) = 0) and the drain (x = L, V(x) = V_d), we obtain :

$$I_{ds} = (W/L)\, \mu_{fe}\, C_g\, [(V_{gs} - V_t)V_{ds} - V_{ds}^2/2] \quad (5)$$

The channel current saturates when $dI_{ds} / dV_{ds} = 0$, which occurs for $V_{ds} = V_{gs} - V_t$; the corresponding value of the channel current is :

$$I_{ds\ sat} = (W/2L)\, \mu_{fe}\, C_g\, (V_{gs} - V_t)^2 \quad (6)$$

Figure 6 shows the typical output characteristics of an inverted staggered TFT. These output characteristics correspond to the transfer characteristics shown in figure 5.

According to the above expressions, the field effect mobility and the threshold voltage can be determined either by using the measurements of I_{ds} as a function of V_{gs} at low V_{ds}, thus neglecting the V_{ds}^2 term (linear region) or using the values of I_{dssat} also as a function of V_{gs}. In the former case, a plot of I_{ds} versus V_{gs} results in a straight line (see figure 7-a) and from its slope, μ_{fe} can be determined, whereas in the latter case, a plot of $I_{dssat}^{1/2}$ versus V_g is also a straight line, with a slope proportional to $\mu_{fe}^{1/2}$ (figure 7-b). In either case, Vt is determined by the intercept with the voltage axis. This is also illustrated in figures 7-a and 7-b. In the present situation, V_t is ~2 V and μ_{fe} amounts to 0.5 $cm^2V^{-1}s^{-1}$ in the linear region and to 1 $cm^2V^{-1}s^{-1}$ in the saturation regime. This discrepancy in the value of μ_{fe} is probably due to the fact that saturation is not really reached (see figure 6) in such a-Si:H TFTs.

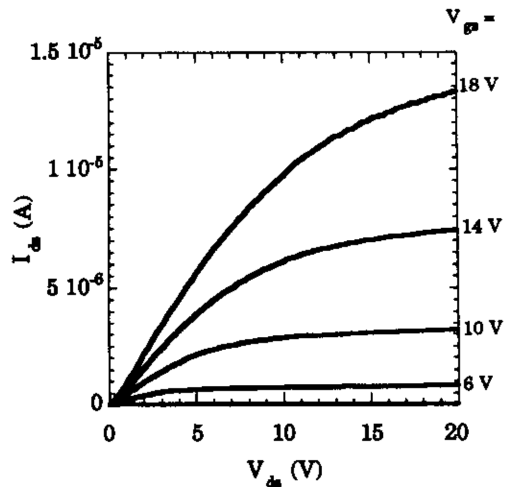


Figure 6 : Output characteristics of the inverted staggered a-Si:H TFT of figure 5; channel width = 28 μm and gate length = 5 μm. (courtesy of Thomson LCD).

For p-channel devices, the threshold voltage tends to be high, because of the large slope of the tail states (T_v ~ 400-450 K) and its definition would be different from the one given above for the n-channel device because the onset of conduction does not occur just as the Fermi level enters the tail states. Moreover, as the field effect mobility for holes is more than two orders of magnitude smaller than the one for electrons, p-channel TFTs are not used in practice.

Table 1 compares some properties of a-Si:H TFTs with those of single crystal Si MOSFETs, either in bulk or thin film (SOI) forms. Typical data for polycrystalline Si and CdSe are also shown.

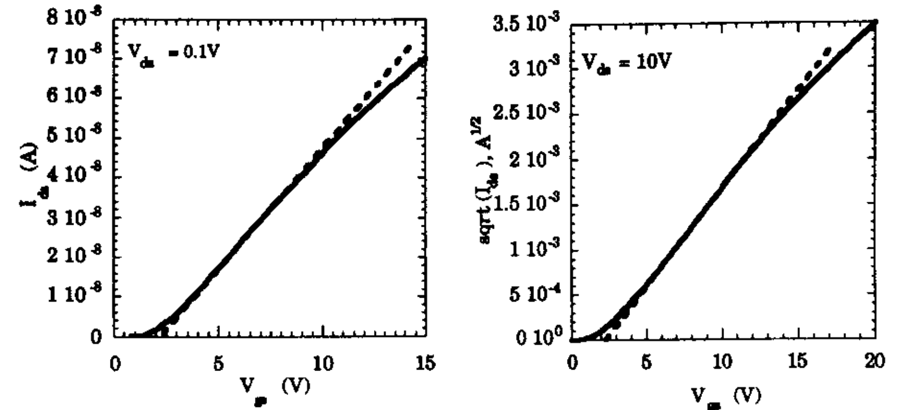


Figure 7-a : Derivation of the mobilty and threshold voltage values for a-Si:H TFT in the linear regime (see text). The dashed line represents the best linear fit.

Figure 7-b : Derivation of the mobilty and threshold voltage values for a-Si:H TFT in the saturation regime (see text). The dashed line represents the best linear fit.

Table 1 : Comparison of TFT characteristics for c-Si, poly-Si, a-Si:H and CdSe materials.

active layer	c-Si			poly-Si			a-Si:H	CdSe
	bulk	SOI		High-T	Low-T			
		SIMOX	SOS	SPC	SPC	Laser		
μ_{fe}, n-channel ($cm^2V^{-1}s^{-1}$)	400 to 700	300 to 600	300 to 500	40 to 120	20 to 70	50 to 400 *	0.2 to 1.5	50 to 400
μ_{fe}, p-channel ($cm^2V^{-1}s^{-1}$)	100 to 200	100 to 300	150 to 300	20 to 80	20 to 50	30 to 200		1 to 10
V_t (V) n-channel	0.25 to 1.75	0.2 to 1	0 to 0.5	1 to 5	2 to 8	1 to 5	0.5 to 5	0.5 to 5
V_t (V) p-channel	-0.25 to -1.75		0 to -0.5	-2 to -8	-2 to -10	-1 to -5	-	-1 to -5

* values up to 600 $cm^2V^{-1}s^{-1}$ have been obtained with special substrate thinning techniques (see § 3.3.)

The major drawback associated with a-Si:H is the structural instability of the material, which was first evidenced in solar cells almost twenty years ago and explained in terms of photon-induced defect creation [27]. In a-Si:H TFTs, the instability manifests itself by an appreciable change in the threshold voltage (and of course subthreshold slope),

after the application of a prolonged gate bias. However, in a TFT, this instability can originate either from defect creation in the a-Si:H material (i. e., change in the density of states by creation of dangling bonds as for solar cells) but also from charge trapping into the gate insulator. In fact, both mechanisms seem to be operative, state creation dominating for low to moderate gate bias stresses and charge trapping for high bias, at least for TFTs using SiN_x as gate insulator [28]. In particular, the threshold voltage shift at moderate gate bias has been interpreted on the basis of the defect pool model, in which the density of carriers in the tail states are in equilibrium with the density of deep. states [29]. Within the frame of this model, if for instance, the gate of a n-channel nitride TFT is positively stress-biased, which increases the electronic density in the conduction band tail, then, the a-Si:H material will respond by breaking weak Si-Si bonds, thus creating D-levels deep in the gap and modifying its density of deep states [28,30]. The threshold voltage shift would therefore reflect this change in the density of deep states. However, it has been pointed out recently that for the particular regime of low gate bias stress, the mechanism of deep state creation could hardly account for the large threshold voltage shifts observed and that trapping in the gate insulator also had to be considered, specially in those TFTs employing SiO_2 as gate insulator [31].

Despite the threshold voltage instability, and even if the exact mechanism is still debated, AMLCDs make extensive use of a-Si:H TFTs, because the duty cycle of the pixel switching element is low enough (1 / 500 to 1 / 2000, depending on the number of rows) to ensure satisfactory operation over the life time of the display [32].

TFTs such as the one shown in figure 3-a are fabricated using microlithographic techniques borrowed from the microelectronic industry. Typically, four mask levels are necessary, for the gate electrode, the a-Si:H mesa, the etch stopper (which can eventually be self-aligned by illumination from the back, thus suppressing one level) and finally the contact metal. However, this mask count can rise to 10 and even more, when for instance, image sensor arrays or AMLCDs with some form of integrated drivers are fabricated (see below). Table 2 summarises the major technological steps necessary for the fabrication of a bottom-gate TFT.

Table 2 : Major technological steps and number of masks necessary for the fabrication of a bottom-gate TFT.

step	description	mask
1	glass cleaning	
2	gate metal deposition	
3	gate patterning and etching	1
4	insulator / a-Si:H / etch stopper deposition	
5	etch stopper patterning and etching	2
6	a-Si:H mesa patterning and etching	3
7	a-Si:H (n^+) and source / drain metal deposition	
8	a-Si:H (n^+) and source / drain metal patterning and etching	4

2.3. Applications of a-Si:H and related materials

Solar cells

Chronologically, p-i-n diodes for solar cell applications were the first devices to be fabricated with combinations of doped and intrinsic films of a-Si:H deposited on a glass substrate [33]. At that time, the energy conversion efficiency was 2.4%. It is now around 13% at the laboratory level for single junction devices and the a-Si:H module production presently amounts to 21% of the world's photovoltaic module production of 62 MW [34]. The absorption spectra of a-Si:H is centred around 500 - 600 nm where the quantum efficiency reaches 95%. In p-i-n photodiodes, the n and p layers are about 10nm thick, whereas the thickness of the intrinsic layer is of the order of 0.6 µm. This intrinsic layer is depleted naturally and full collection is achieved without the need for a reverse bias. Figure 8 shows the structure of a single junction cell; a buffer layer (not shown here) is often added at the p-i interface, in order to reduce carrier recombination.

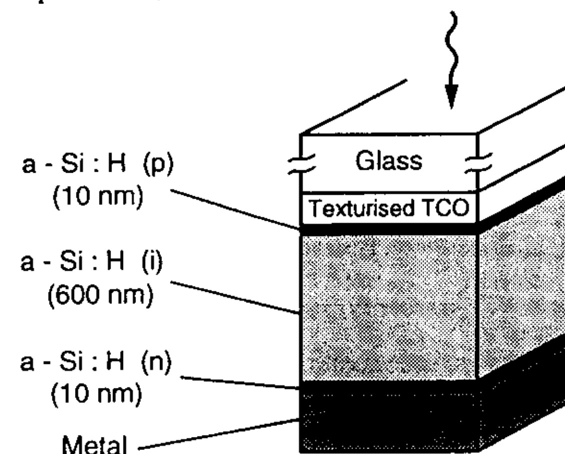


Figure 8 : Structure of a single junction p-i-n solar cell.

Multi-junction cells and artificially constructed junctions (i.e., cells making use of a combination of amorphous and polycrystalline Si materials) are actively being studied and developed, in order to increase the energy conversion efficiency [34].

Displays

Soon after the demonstration of the first a-Si:H transistor [2], several companies developed full colour active matrix liquid crystal displays (AMLCDs) capable of functioning at video rates. It is not the object of the present paper to review the field of AMLCDs, and for details on their operating principles the reader is referred to specialised book chapters [35-37].

Briefly, an AMLCD is made up of an array of liquid crystal cells which are sequentially addressed by non-linear switching elements. A liquid crystal cell is a voltage

dependent light modulator, whose principle is shown on figure 9 for a twisted nematic (TN) liquid crystal material.

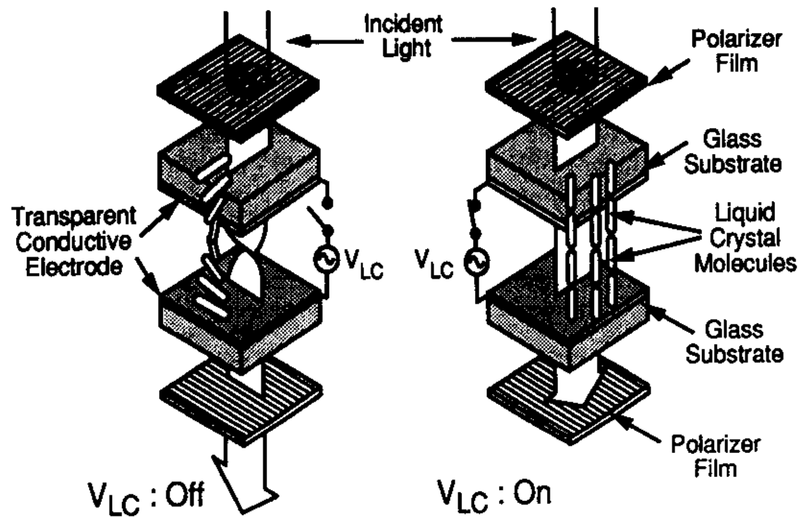


Figure 9 : Schematic structure and operating principle of a twisted nematic (TN) liquid crystal cell inserted between cross polarisers. In the unbiased state, light is transmitted, whereas when the cell is biased, light is blocked. The reverse holds true when the polarisers are parallel.

In this kind of cell, the molecules are aligned in such a way that their directors on the inside of the front and back glass plates make an angle of 90°. A rubbed polyimide film allows the anchoring of the molecules with the desired orientation on each glass plate. Thus, the molecules gradually rotate from the front to the back glass plate, inside a typically 5 µm-thick gap. The glass plates are inserted between cross polarisers, so that the incident light is transmitted due to the progressive rotation of its plane of polarisation by the liquid crystal molecules. When the cell is biased (using the transparent conductive electrodes), the liquid crystal molecules tend to align with the electric field, which first reduces the rotation of the plane of polarisation thus limiting light transmission and finally completely inhibiting it, when the applied voltage is high enough to bring the directors of the molecules perpendicular to the surface of the glass plates. The effect of light blocking is therefore progressive, which will allow the control of grey levels. The polarisers can also be parallel, in which case light is transmitted when the cell is biased and blocked when unbiased.

In an AMLCD, each individual liquid crystal cell represents a pixel, a denomination that comes from the contraction of picture element. Colour effects are obtained by interposing red, green and blue (RGB) filters on the light path controlled by each pixel. Images are produced by applying an adequate voltage (data voltage) on each pixel during

the fraction of the frame time where the non-linear switching element is in the on-state. When the switch is turned off, the data voltage is retained on the liquid crystal capacitance during the remaining of the frame. The switching elements can be two or three terminal devices, the data signals being decoupled from the select signal in the latter case. To date, the two terminal devices mostly used are metal / insulator / metal (MIM) structures and diodes made of various semiconductor materials including a-Si:H [36-38]. The advantage of two terminal devices is the reduced number of masking steps (usually three to four) that are necessary for the fabrication of the active plate. One of the drawbacks originates from the slight thickness non-uniformity of the different films (inherent to any deposition or oxidation method), over large surfaces, likely to induce appreciable variations of the current-voltage characteristics of the non-linear elements over an AMLCD plate. This is particularly true for the MIM devices, where the value of the current depends exponentially on the thickness of the insulating film [37].

The vast majority of AMLCDs make use of three terminal devices in the form of thin film transistors and among these, a-Si:H TFTs are the most widespread. One of the advantages of using a transistor as switching element probably comes from the fact that the thickness of the accumulation layer which is formed in the channel primarily depends on the gate voltage and not on the actual thickness of the active layer. Hence, even if there are some thickness variations due to the particular deposition process employed, the effect on device characteristics over an AMLCD plate is smoothed. In particular, the on-current fluctuations will be inversely proportional to thickness fluctuations of the gate insulator, instead of varying exponentially with the latter's, as is the case for MIM devices.

Figure 10 shows the electrical architecture of a TFT-addressed active matrix and figure 11 presents a perspective view of an AMLCD (active matrix plate, liquid crystal and counter plate). During operation, a peripheral shift register (line driver) sequentially applies a voltage pulse to each gate line, turning on all the corresponding TFTs. As these TFTs are switched on, the data voltages corresponding to the selected line are transferred from the peripheral driving circuits (data driver) to one of the pixel electrodes, through the TFTs, the other pixel electrode being grounded or held at a fixed potential during the frame time (see the inset in figure 11). The various driving circuits which are schematically located at the periphery of the active plate on figure 10 are usually single crystal silicon chips which are mounted either directly on the glass plate or on separated printed circuit boards and connected to the array of line and columns [38,39]. However, such drivers may also be integrated, which means that they are fabricated with the same TFTs as for the pixel switches, if suitable semiconductor material properties and device characteristics can be obtained.

AMLCDs were primarily developed for direct view applications and a 21" diagonal display was demonstrated in 1994 by Sharp. However, with the advent of high definition television (HDTV), larger diagonals are becoming necessary, in order to take full advantage of image quality and sharpness. Due to a variety of technological and manufacturing problems, direct view displays, with diagonals of up to 40" are not expected

in production until the beginning of the next century. In order to fill the gap, video projectors are actively being developed [40].

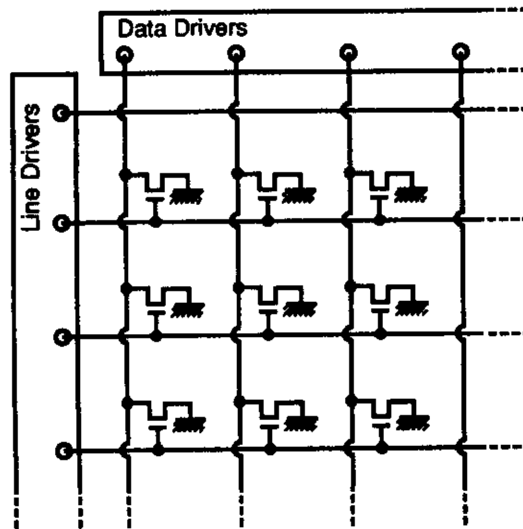


Figure 10 : Electrical architecture of a TFT-addressed active matrix.

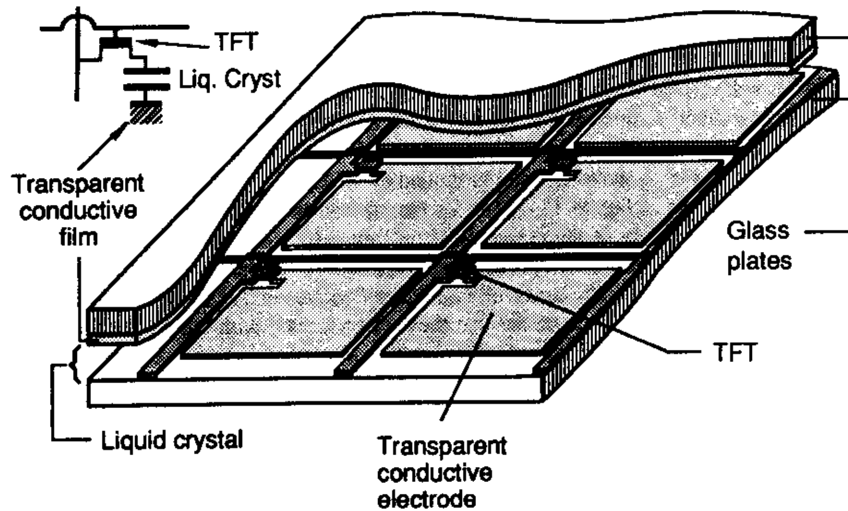


Figure 11 : A perspective view schematically showing the structure of an AMLCD panel.

These projectors which work in the same way as slide projectors, make use of small AMLCDs, with diagonals ranging from typically 2 to 4" and they have an accordingly high pixel density in the active matrix. Figure 12 shows a photograph of an actual active matrix for projection, with a repetition step (pitch) of 50 μm.

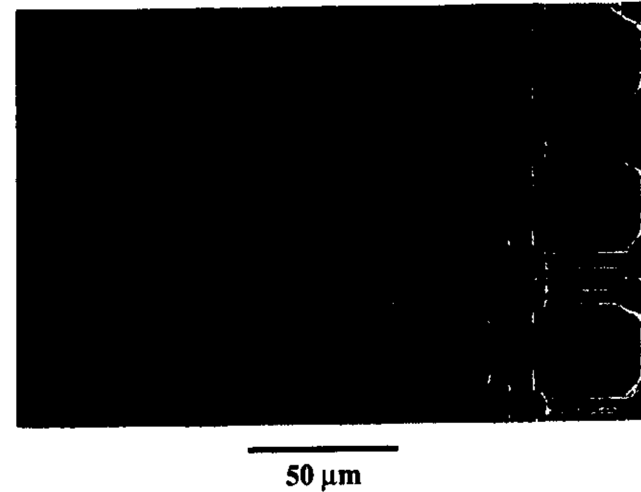


Figure 12 : Photograph of a projection active matrix, showing the array of lines and columns and the pixel structure with its switching transistors (courtesy of Thomson LCD).

Because of the reduced cell size, the mounting of the peripheral circuitry with a pitch of the order of 50 μm or even below is a major issue, assuming that an acceptable yield is to be maintained. There is hence an interest in integrating the peripheral circuitry on the active plate.

Ideally, integrated drivers should be capable of treating the standard video signal and dispatch it over the whole panel, once the correct voltage levels generated. These vary between -5 and +5V, as the pixel polarity is reversed after each frame, in order to avoid electrochemical effects at the interfaces between the conductive electrodes and the liquid crystal material. Schematically, the liquid crystal panel requirements are the line scanning and the conversion of the serial RGB signal to the (parallel) voltages to be applied to the data columns. While line scanning requires typical frequencies of several tens of kHz (depending on panel resolution), which can be achieved with low mobility devices, the conversion of the serial RGB signal is much more difficult, because both the frequency and RGB signal levels have been developed for cathode ray tubes and they are not matched to the peculiar features of AMLCDs. The frequency of the analogue RGB varies between 4 and 75 MHz depending on the desired resolution, and for correct driver operation at such frequencies, high quality TFTs must be used, with high mobility values. Furthermore, the amplitude of the video signal has to be raised to the adequate level between 0 and 5V

(instead of between 0 and 1V) and reversed after each frame, which means that the effective voltage to be treated is 10V.

As far as a-Si:H is concerned, the low carrier mobility severely limits the potential speed of circuits. Moreover, as usually the source and drain contact regions of the TFT are not self-aligned, the parasitic capacitances are important, decreasing further the maximum attainable speed. A self-aligned doping process [41] requires the use of ion implantation (which is costly), together with the self-aligment of the contact metal itself, in order to limit the source and drain series resistance due to the high resistivity of the doped a-Si:H material (see § 2.1.). Although currently studied, this kind of process is, to our knowledge not yet totally developed, the formation of the source / drain "salicide" at low temperature being difficult to control. Furthermore, circuit architectures are limited by the non-availability of p-type devices and the instability of the TFTs (see § 2.2.) turns out to be a problem, because in data driving circuits, the duty cycle is high (1 / 10 to 1) leading to a rapid performance degradation [42]. In spite of the above drawbacks and problems, and because the idea is just too attractive, a-Si:H scanning circuits have been fabricated [43,44] and solutions for data drivers (although with a necessary large number of parallel video inputs) are currently being investigated. This being said, the safer solution to driver integration is probably the use of polysilicon material, as will be discussed below.

Image sensors

Another application of a-Si:H-based large area electronics is in the field of image sensors. These make use of combinations of photodiodes, with a structure identical to the one shown in figure 8 and switching elements, i.e. TFTs, which are organised in linear or matrix arrays. A reverse-biased photodiode may be considered as a parallel combination of a ligh-controlled current source and a capacitance. Thus, the carriers which are generated upon illumination and separated by the internal electric field of the reverse-biased device can be stored by this capacitance. The corresponding charge which is proportional to the density of photons incident on the photodiode can be sampled and measured by some external circuitry.

Page-width linear image sensors have been developed for image or document scanners, where their use greatly simplifies the overall optical architecture of the system; the sensing elements can practically be placed in contact with the document to be imaged, which yields a much more compact optical arrangement than the conventional one with the CCD imager [45]. Furthermore, contact scanning allows an increase in the resolution, since there is no need to reduce the document, in order to comply with the limited size of the CCD array. Scanners exhibiting a resolution of 300 dots-per-inch can be made with a-Si:H sensor arrays [45]. Also, it should be emphasised that some form of signal processing could in principle be integrated on the sensors' substrate (using for instance polysilicon circuitry), which could (and probably soon will) further extend the domain of application of large area electronics.

While such sensors today account for more than one half of the market of image sensors in fax machines, the next challenge is to develop and industrialise page-size two-

dimensional imaging arrays. Such arrays are organised in much the same way as the AMLCDs are, the liquid crystal element being replaced by a reverse-biased photodiode. When a line is activated, the charge stored in the photodiode in each pixel of the line is transferred through the columns to the data drivers where it is measured and coded. The different lines are sequentially scanned so as to read out the whole array in a frame time. The most ambitious application of these two-dimensional sensor arrays is today x-ray medical imaging [46], where pannel size has to compare with parts of the human body and a spatial resolution of 200 µm or less is required. For this kind of application, a phosphor film is used to convert x-ray photons to visible ones and the array is placed in contact with the phosphor, in order to allow for direct imaging (see figure 13).

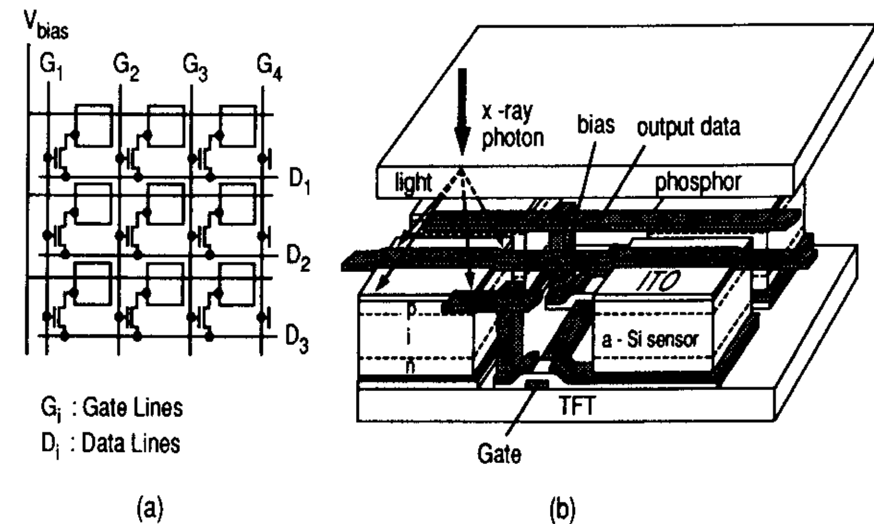


Figure 13 : X-ray image sensor, (a) electrical architecture of the array of photodiodes and TFTs, (b) a schematic and simplified perspective view of the structure of the sensor panel (after [46]).

Here, the use of a-Si:H for both the photodiodes and TFTs is well suited, because of its high tolerance to ionising radiations. The University of Michigan and Xerox have recently developed a prototype array of 19.5 by 24.4 cm^2, comprising 1536x1920 pixels, with a pitch of 127 µm [47]. Such arrays are presently available from Xerox as evaluation kits. Thomson-CSF has also announced the development of a 1000x1000 array, with a pitch of 200µm. However, these x-ray sensors are at present time at an early stage of development and they are not expected on the market before the end of the century.

To conclude on the application aspects of a-Si:H material and technology, it should be mentioned that Tuan [48] has described the use of amorphous silicon TFTs (including high voltage devices) to drive the printing transducers of ionographic, electrographic and

liquid crystal shutter printers, whereas Böhm and coworkers have described the fabrication of amorphous silicon logic integrated circuits [49].

2. 4. *The industry of AMLCDs*

As stated in the introduction, the production of AMLCDs is to day a big business and it is mainly concentrated in Japan. Table 3 from W. O'Mara [50] shows the investments in second-generation production machinery undertaken by the major japanese and korean manufacturers. In Europe, a joint-venture between Philips, Thomson CE, Sagem and Merck (Flat Panel Displays, FPD) was set up at the end of 1992 and more than 300 M$ have been invested so far by the various partners. FPD intends to take a 8% share of the AMLCD market. In the US, Optical Imaging Systems was set up at the end of 1994 with an investment of 100 M$ and the US intend to have a 15% share of the flat panel displays market by the year 2000 (see e.g. the Flamm report available from SEMI in the US).

Table 4, taken from a recent paper of L. Tannas [51] shows the trends in display and substrate size. The very large substrate sizes envisaged in the near future explain partially the high level of investments, as specific fabrication equipments are necessary.

Table 3 : Current investments in the field of AMLCD (after [50]) .

COMPANY	Investment $ Million
Sharp	1.000
NEC	650
Fujistu	390
Toshiba / DTI	300
Hitachi	300
Hoshiden	200
Goldstar	430
Samsung	400
Hyundai	150
Total	**3.820**
	Source : Nikkei Microdevices O'Mara § Associates

The industrial fabrication of an AMLCD can be separated into three main tasks. First the realisation of the "front" glass plate, which comprises the color filters, the black matrix, the transparent conductive electrode and the polyimide alignment layer. Second, the preparation of the active plate (a glass substrate as well), which supports the array of lines, columns, TFTs, pixel electrodes, pixel storage capacitors etc... and finally, the assembly of the two plates and the liquid crystal filling between them.

As far as the fabrication of the active matrix is concerned, the major production equipments are sputtering machines, for the deposition of the metal conductors and transparent electrodes (usually made of indium tin oxide-ITO), PECVD reactors for the growth of SiO_2 or SiN_x and a-Si:H (usually in the same pump-down), lithography

equipments (steppers or mirror projection units) and dry etching machines. While for first generation PECVD equipments, the glass substrates were moved sequentially through in-line chambers tens of meters long evoking stainless steel cathedrals, the tendency for the second generation is towards the use of multichamber systems. This trend was clearly illustrated in O'Mara's SID seminar [50], where a variety of cluster tool PECVD and sputtering machines were presented. A similar cluster tool concept is also being developed by TEL America on the East coast, for PECVD machines [52]. In second-generation machines, the deposition rates have been increased (particularly for a-Si:H films), to values over 100 nm min^{-1} and typical throughputs are around 30-45 substrates per hour.

Table 4 : Trends in display and substrate sizes (after [51]).

Generation	Zero	1st	2nd	3rd	4th
Year start	1987 LSI	1990 New generation	1993-1994 Installation	1996 Planning	1999? Future
Glass sheet size (mm)	150 x 150 150 x 200	320 x 400 300 x 350 300 x 400	360 x 465 380 x 480 (1994)	500 x 700 500 x 600 450 x 550	TBD
Display size in inch. (number per plate)	6 (1) 9 (1)	8 (4) 6 (4) 10 (2)	10 (4) 14 (2) 7 (6)	14 (4) 30 (1)	
Cycle time	Variable	Normalised to 1	2x		
Productivity		Normalised to 1	3x to 5x		
Yield	< 10% iniatlly	> 50%	> 70%		
Major market	Portable TV	Notebook PC	Desktop PC Subnotebook PC	Engineering workstation	HDTV ?
Machine technology life, 3 years Machine production life, 7 years				Source : Tannas Electronics, Orange, California	

The purity of the deposited films has also been greatly improved, and Balzers has recently introduced the plasma box concept (see figure 14), where the plasma volume is confined in a gas-tight enclosure installed inside a conventional high vacuum vessel. With the above arrangement, the measured oxygen and carbon concentrations in a-Si:H films are always below 10^{18} cm^{-3} and the plasma box has been shown to be practically immune to post-cleaning contamination, as evidenced by the very low residual level of sulfur which is measured in the films just after a SF_6-based plasma cleaning of the deposition chamber [53]. Particle formation during deposition is one of the major problems associated with PECVD and sputtering processes and its deleterious consequences on the fabrication yield of the active plate are well documented [50,51].

However, here again, things have been improved with second-generation equipments, since the substrates are now moved by robot arms, rather than being displaced on conveyor belts where particles are easily generated by friction on supporting rolls, side walls, etc... Furthermore, in-situ plasma cleaning which can be performed quite often,

even after each deposition run, allows to avoid the peeling and flaking-off from the walls of the deposition chambers of excessively thick deposits. For all these reasons, fabrication yields around 90% are now claimed in Japan for the TFT plates and NEC has a new factory where a 100% yield is expected [54].

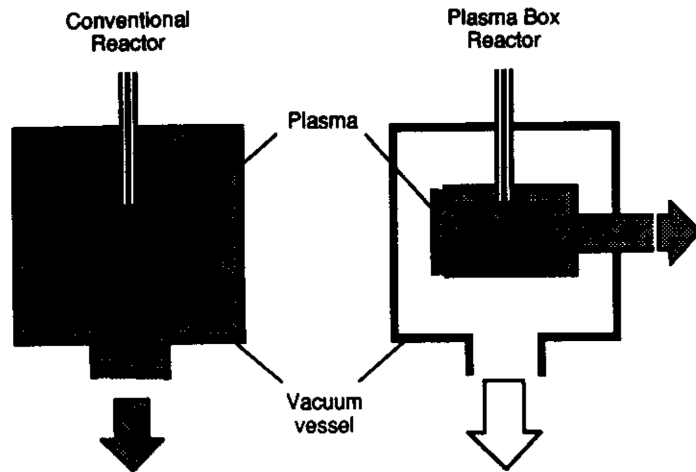


Figure 14 : Plasma-box reactor compared to a conventional reactor. Grey: process gas zone (pressure ~ 0.1-1 mBar). White: Low pressure zone (<< 0.1 mbar). (Courtesy of Balzers).

3. Polycrystalline silicon thin films for large area electronics

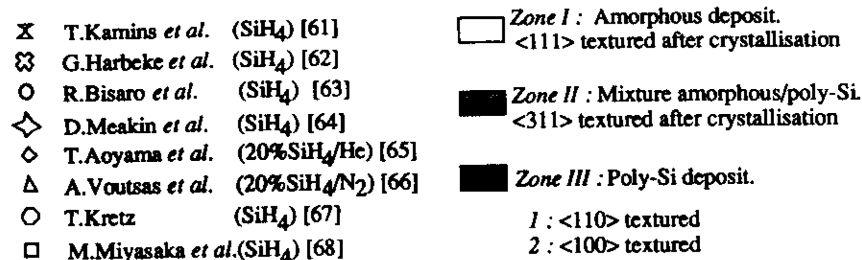
Poly-Si technology has been studied for some years, essentially for three-dimensional integrated circuit applications [55]. As the substrates in this case are silicon wafers, standard high temperature processes (> 900°C) have been used for the fabrication of TFTs, in particular concerning gate oxide synthesis and damage annealing after ion implantation of the source and drain regions. More recently, active matrix liquid crystal displays (AMLCDs) with integrated drivers have been fabricated on refractory quartz substrates, also using a high temperature poly-Si technology, for applications in the field of video projectors [56]. In Japan, six inch CMOS fabrication lines are used to manufacture viewfinders with integrated drivers, using a high temperature poly-Si technology on quartz substrates. However, as far as LCDs are concerned, the elevated cost of quartz substrates, compared to that of glass plates, makes this high temperature technology relatively unattractive. As a consequence, much effort has been devoted, in recent years, to reducing processing temperatures around 600°C, thus permitting the use of cheap glass substrates. Moreover, most of the research work has been directed towards the increase of the grain size of polysilicon material, since the results have always confirmed intuition : the larger the grain size, the better the electrical properties of TFTs.

3.1. Low temperature polysilicon material synthesis

Over the last fifteen years, various deposition methods have been studied in order to obtain polysilicon layers leading to high quality thin film transistors. For this purpose, two main approaches have been used. One is to directly deposit a polycrystalline film, also called direct-poly, the other is to crystallise an amorphous silicon precursor. In either case, the most widely used method to obtain such films is the so-called low pressure chemical vapour deposition (LPCVD) technique where silane (SiH_4) or disilane (Si_2H_6) gas can be pyrolyzed at various temperatures. In addition to this method, which will be described below, atmospheric pressure CVD (APCVD), plasma enhanced CVD (PECVD) and (ultra high) vacuum evaporation have also been studied in order to deposit amorphous layers. Evaporated films contain voids which adsorb contaminants (oxygen, carbon,...) upon exposure to air [57,58]. PECVD layers are very sensitive to the residual atmosphere during deposition, since the incorporation of the background impurities is also enhanced by the plasma [59]. It is important to note that, for these two methods, the impurity content alters the subsequent crystallisation of the films and thus the characteristics of TFTs fabricated with such films [59]. Also, it has been shown that polysilicon material obtained by crystallisation of APCVD films exhibits a lower crystalline quality, compared to films obtained by LPCVD [60,63]. For these reasons, the LPCVD technique has been extensively studied and used throughout the world. Since the use of Si_2H_6 precursor gas appeared only quite recently, we will first discuss the properties of LPCVD films obtained from SiH_4 gas.

When SiH_4 is used as gas precursor, depending on the operating conditions, a polysilicon (direct-poly) or an amorphous film can be obtained. In this latter case, a subsequent crystallisation is performed. A synthesis of the results published in the literature over the last fifteen years [61-68] is presented in figure 15 which shows the crystalline state and crystalline structure of silicon films as a function of the deposition pressure (P_d) and temperature (T_d).

This type of representation, used first by Bisaro *et al.* [63] and later by Joubert *et al.* [69], Voutsas and Hatalis [66], and Kretz [67], permits a clear definition of three different zones, I, II and III, corresponding respectively to operating conditions leading to amorphous, mixtures of amorphous and polycrystalline and completely polycrystalline silicon films. This last zone (III) can also be divided in two sub-zones corresponding to <110> and <100> textures as shown by Meakin *et al.* [64] and mainly by Miyasaka *et al.* [68] who have used pure SiH_4 as precursor gas. As suggested by Joubert *et al.* [69], the <110>/<100> transition seems to depend on the partial pressure of SiH_4 (P_{SiH_4}) and not on the total deposition pressure, since this author obtains similar results for P_{SiH_4} in the same range as Meakin *et al.* and Miyasaka *et al.*, but with 10% SiH_4 diluted in H_2. This being said, the phase diagram of figure 15 is not universal, as the carrier gas, deposition rate and residual atmosphere are likely to highly influence the kinetics of direct crystallisation, particularly in the high pressure regime [66].



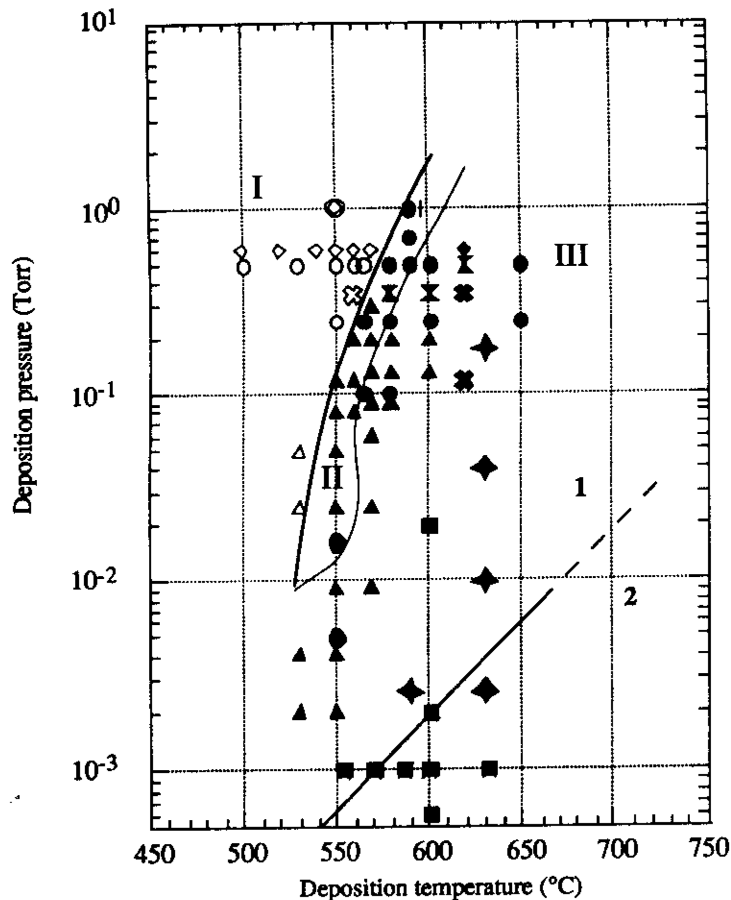


Figure 15 : Crystalline state and structure of as-deposited silicon films as a function of deposition temperature and deposition pressure, when the gas precursor is SiH_4. For each author, we have indicated in the legend whether SiH_4 was diluted or not.

3.1.1 Direct-poly deposition

The first studies on polysilicon thin films were driven by their use as electrodes and interconnects in silicon integrated circuit processes [55]. In conventional ICs processes, polysilicon is deposited undoped and subsequently doped using either diffusion or ion implantation. The deposition pressure is generally fixed around 0.2 Torr and the deposition temperature is typically 630°C, in order to obtain deposition rates above 10 nm/min (see A. C. Adams, chapter 6 in [70]).

In order to obtain direct-poly at temperatures compatible with glass substrates (T≤600°C), silicon deposition has been studied in the low deposition pressure range (P_d≤40 mTorr). New methods have appeared such as the very low pressure CVD [64] and the infra low pressure CVD [68] which, due to the use of efficient turbomolecular pumping systems, can operate respectively in the mTorr and the submTorr range with pure SiH_4 gas. It has been shown [64,68] that, as far as material's crystalline quality is concerned, reducing the pressure leads to the same improvements as increasing the temperature. At 630°C, Meakin *et al.* [64] have obtained for a deposition pressure of 40 mTorr a striated <110> structure with no streaks in the diffraction pattern and no lattice parameter distortion compared to the films obtained at 180 mTorr. However, the electron mobility of TFTs fabricated with such films is 8 $cm^2V^{-1}s^{-1}$, which is quite low. Reducing the deposition pressure to 2.5 mTorr leads to a change from a striated <110> to a columnar, tooth-shaped, <100> film with elongated grains throughout the thickness. This crystalline change occurs at different functioning points : (630°C, ~5mTorr) after Meakin *et al.* [64], (600°C, 2mTorr) or (570°C, 1mTorr) after Miyasaka *et al.* [68]. The crystalline quality of tooth-shaped layers increases with the thickness of the films, and the size of the crystallites near the surface is around 0.2 µm for a film thickness of 0.6 µm. These crystallites contain few defects but the surface of the films is very rough. Consequently, only very thin films (50 nm) are compatible with TFT fabrication, with the disadvantage that the first 50 nm grown contain a high density of micro twins. Miyasaka *et al.* [68] have fabricated TFTs with a 25-nm thick polysilicon channel for P_d = 1 mTorr and for deposition temperatures of the channel varying from 550°C to 630°C. The mobility (in $cm^2V^{-1}s^{-1}$) of such TFTs was found to increase from 9 (T_d=550°C) to 16 (T_d=615°C) and then decrease to 13 (T_d=630°C). The 615°C deposition temperature appears as the best compromise between the increase of the crystalline quality of the film and the roughening of the surface, this latter phenomen beeing a direct consequence of the increase of the size of the crystallites. This roughening phenomenon alters the channel-SiO_2 interface and thus the mobility of the TFTs. At this point, it should be borne in mind that the actual thickness of inversion or accumulation layers in MOS transistors is of the order of 10 nm [21].

In order to further improve the crystalline quality of direct-poly Si films, a new method has been recently investigated : the ultra high vacuum CVD. This system combines the advantages of the techniques of CVD and UHV and allows the use of gaseous precursors together with the obtaining of a low residual pressure in the reactor (10^{-9} Torr). It was first introduced by Meyerson [71] to realise homoepitaxial silicon films at low temperature. The idea is that the impurities (H_2O, O_2, CO, CO_2, C_xH_y) present in

classical LPCVD systems promote defect nucleation and can inhibit the crystalline growth, thus leading to epitaxial films with a high defect density. Using an UHVCVD system to deposit the channel layer at 550°C and for a deposition pressure of 1 mTorr, Lin *et al.* [72] have claimed a hole mobility of up to 28 $cm^2V^{-1}s^{-1}$ in p-channel TFTs which is, to our knowledge, the best published value for direct-poly films. No mention is made of electron mobility values. However the deposition time is around three hours for a 100-nm thick film (T_d=550°C) and the grain size is limited to 50 nm.

As a conclusion, direct-poly films obtained either by ILPCVD or UHVCVD are characterised by small grains with a high density of micro twins for thin layers (around 50 nm) and by a surface roughness associated with the grain size, which alters the electrical quality of the channel-gate oxide interface.

3.1.2 Deposition of an amorphous precursor by LPCVD

Poly Si obtained by solid phase crystallisation (SPC) of an amorphous precursor (a-Si) has been shown, over the last few years, to yield to a perfectly smooth surface. Moreover, a grain size of up to 0.5 µm, i.e. one order of magnitude larger than that of direct-poly films, can be obtained after SPC. In fact, this method allows one to disconnect the mechanism which determines the grain size from the one determining the roughness of the films. Usually, the amorphous films are obtained in deposition conditions where there is very little surface mobility (T_d~550°C and P_d~0.5 Torr). The corresponding surface roughness of the as-deposited films is therefore small. This roughness is preserved upon solid phase crystallisation (SPC), because (i) SPC proceeds from the substrate / a-Si interface [63] and (ii) the a-Si surface is usually self passivated by a film of native oxide [73] which blocks surface diffusion.

The deposition of the a-Si precursor is performed either with pure or hydrogen-diluted SiH_4. As shown in figure 15, the usual partial pressure of SiH_4 is in the range of 0.2 to 1 Torr and the deposition temperature is generally between 500 and 570°C. Figure 16 shows the deposition rate plotted versus the reciprocal deposition temperature (1/T) obtained in a LPCVD system using SiH_4 diluted in hydrogen [74].

Generally, for CVD processes, the deposition rate can be limited by three types of mechanisms which are (i) homogeneous gas phase decomposition of the growth nutrient (e.g. SiH_4), (ii) surface catalytic reactions and (iii) diffusion of the active species through a boundary layer (mass transport limitation). However, this latter mechanism occurs only in the high temperature range (T>800°C) [75]. In the low temperature range (T<650°C) and when pure SiH_4 is used at pressures ranging from 0.1 to 1 Torr, the limitation of the deposition rate is usually attributed to the decomposition of SiH_4 in SiH_2, either in the gas phase or on the silicon surface. In this case, the corresponding activation energy of the deposition rate is found to lie between 1.30 and 1.69 eV [60,63,76-78,79]. On the other hand, values of 1.74 to 2.2 and 2 eV have been reported for respectively atmospheric [60,63,75] and low pressure (2 Torr, see figure 16) deposition performed with SiH_4 diluted in all cases in H_2, and values of 1.9 to 2 eV for the deposition from pure SiH_4 but

in the mTorr range [72,80]. For the above situations of higher activation energies, the limiting step is thought to be the desorption of hydrogen from the surface.

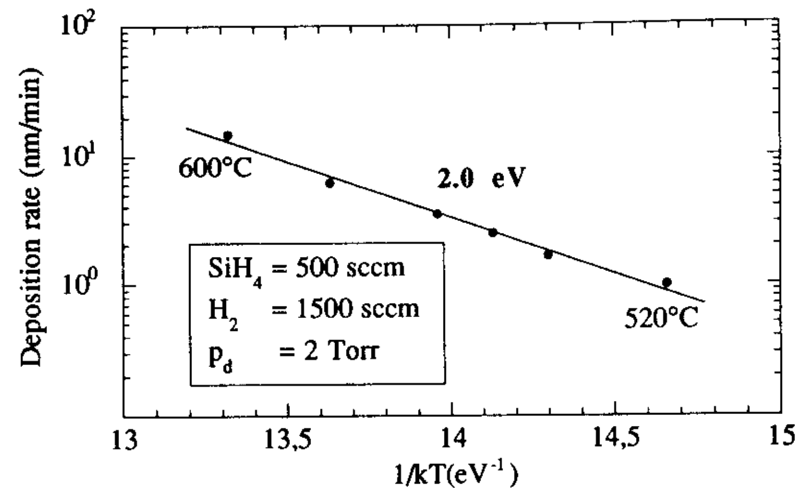


Figure 16 : Deposition rate versus reciprocal deposition temperature for SiH_4 precursor [74].

Several authors [60,63,65,79,81,82] have performed extensive studies of the solid phase crystallisation of amorphous silicon obtained by LPCVD of SiH_4 (see below) and have shown that a deposition temperature of about 550°C is an optimum value which leads to a grain size of up to 0.5 µm for thin films (0.1 to 0.2 µm) after SPC.

As a conclusion, polysilicon films obtained by solid phase crystallisation of a-Si exhibit grain sizes one order of magnitude larger than that of direct polycrystalline films. Moreover, the obtained films are perfectly smooth, as they keep the near perfect surface quality of as-deposited amorphous films. N-type polysilicon field effect mobility can reach values up to 55 $cm^2V^{-1}s^{-1}$ [83] showing the higher quality, compared to direct-poly Si, of the polycrystalline material obtained in this manner.

In order to further increase the carrier mobility in polysilicon TFTs, much effort has been devoted to enlarging polysilicon grain size, eventually using sophisticated post-deposition procedures based on high dose ion implantation / amorphisation techniques [84,85]. Recently, the use of disilane (Si_2H_6) gas in replacement of SiH_4 for the LPCVD operation has attracted attention, because very large grains (up to 5µm) have been obtained directly after SPC [74,76,77,82,86,87].

Hence, as for SiH_4, the deposition rate for Si_2H_6 has been studied for various different deposition conditions. Figure 17 shows this deposition rate versus 1/T for a Si_2H_6 flow rate of 40 sccm in four different cases: non diluted in hydrogen, diluted in 210, 960 and 1960 sccm of H_2. The corresponding total pressures (P_d) used are 0.04, 0.25, 1

and 2 Torr leading to a constant partial pressure of Si_2H_6 (40 mTorr) in each case. Moreover, for comparison, the deposition rate obtained in the infra low pressure regime (P_d=2 mTorr) is also plotted.

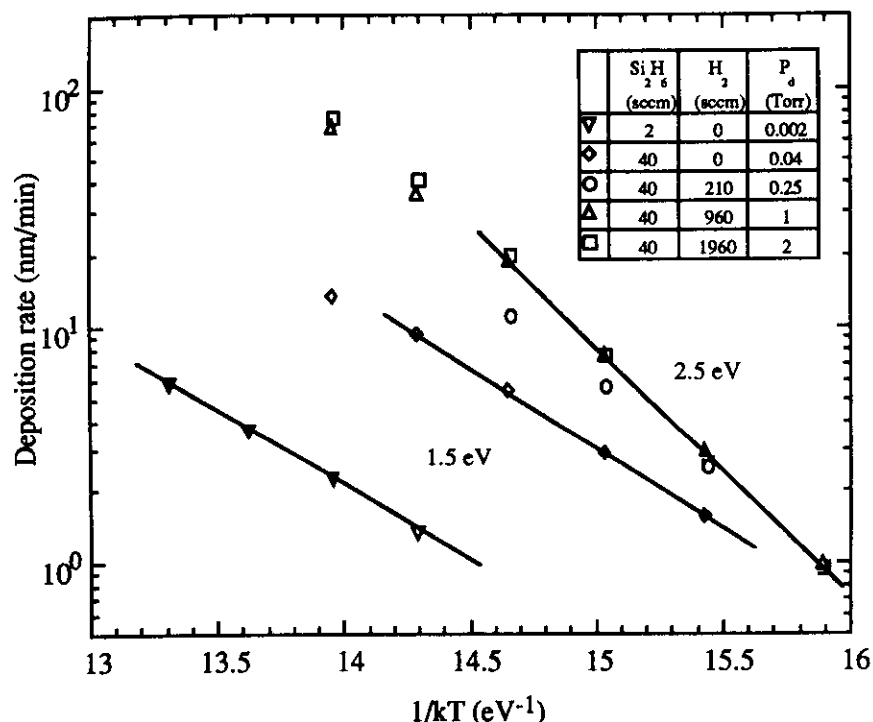


Figure 17 : Deposition rate versus reciprocal deposition temperature for Si_2H_6 gas precursor.

The activation energy is 1.5 eV for P_d equal to 2 and 40 mTorr and 2.5 eV for P_d equal to 1 or 2 Torr. Concerning this activation energy, one can find in the literature very different values depending on process conditions. Hong *et al.* [77] have found 1.35 eV for pure Si_2H_6 at a deposition pressure of 0.64 Torr, Voutsas and Hatalis [86] 0.69 and 0.91 eV with respectively 200 and 300 sccm of Si_2H_6 diluted in helium at 1 Torr, and finally Scheid *et al.* [88] 0.82 to 2.30 eV when increasing the deposition pressure from 0.035 to 0.2 Torr. Consequently, the activation energy for the deposition rate seems to depend on the carrier gas, the process pressure and the gas flowing rate in the LPCVD tube.

Most studies concerning the deposition mechanism of Si from Si_2H_6 have been performed in gas source molecular beam epitaxy systems (GSMBE) i.e. for pressures ranging between 10^{-6} and 10^{-4} Torr. For $T_d \leq 600°C$, high-order hydrides such as SiH_3 are present on the surface [89,90]. Gates and Kulkarni [90] have shown that the hydrogen coverage θ_H can go over unity and is saturated for $T_d \leq 520°C$ at $\theta_H \sim 1.7$. However, chemisorption of Si_2H_6 molecules on -SiH (-Si represents a surface Si atom) species

seems to be possible [91]. Usually, the hydrogen desorption is the limiting mechanism, inducing an activation energy for V_d of 2 eV after Werner *et al.* [92] or 1.8 eV after Mokler *et al.* [93]. On the contrary, easy H_2 desorption has also been observed. Activation energies as low as 1.2 eV for atomic layer epitaxy [89], and 0.95 eV for H_2 desorption from paired monohydre on a single surface dimer have been obtained [94]. Except for this last value, such activation energies can be compared to the ones found for the decomposition kinetics of the following adsorbed species : -SiH (2 eV), -SiH_2 (1.85 eV) and -SiH_3 (1.3 eV) [95]. From these experiments, one can conclude that the deposition mechanism from Si_2H_6 precursor is rather complicated and highly depends on the surface structure during growth.

As far as our own results are concerned, the deposition rate is apparently limited by two different mechanisms, depending on the gas mixture and on the pressure. For P_d=2 mTorr, the activation energy for V_d is 1.5 eV and can be compared to the one found for Si_2H_6 adsorption on Si(100) by Buss *et al.* at P_d=0.34 mTorr [96]. For P_d between 2 and 40 mTorr and for $T_d \leq 520°C$, even if the surface is saturated by hydrogen [90], V_d highly depends on the pressure and thus is not limited by the hydrogen desorption. Since, in this range of deposition pressure, the activation energy is roughly constant (1.5 eV), the limiting mechanism seems to be the Si_2H_6 adsorption rate. Easy H_2 desorption as described above can explain this behaviour.

An increase of the total pressure from 0.25 to 1 and 2 Torr, while maintaining the Si_2H_6 partial pressure at 40 mTorr, improves the deposition rate V_d (see figure 17). This finding is rather surprising since it has been shown that the addition of hydrogen in the gas phase tends to decrease V_d, due to mass transfer kinetics [97]. As observed by Johannes and Ekerdt [98], SiH_2, obtained by gas phase decomposition of Si_2H_6, is the major growth nutrient in the Torr pressure range. Consequently, the deposition rate (V_d) seems to be limited by the supply of SiH_2 molecules on the surface, until the total pressure reaches about 1 Torr. For P_d=1-2 Torr, and for $T_d \leq 520°C$, V_d follows an arrhenius behaviour with an activation energy of 2.5 eV. Since V_d does not depend on the pressure and thus on SiH_2 content in the gas phase, it is very likely that the desorption of H_2 from the surface is the limiting mechanism in that case. This value (2.5 eV) is close to the one calculated by Jing and Whitten (2.3 eV) for the activation barrier of H_2 desorption from -SiH_2 for a $Si_{12}H_{20}$ three layer cluster [99]. Once more, these mechanisms seem to depend on the surface structure since values as high as 2.5 and 2.8 eV have been obtained for H_2 desorption from surface -SiH species respectively for Si(100) [100] and for porous silicon [101].

For deposition at 480°C and at a pressure of 1 Torr, solid phase crystallisation of Si_2H_6 thin films (0.1 µm) leads to grain sizes of up to 5 µm, i.e. one order of magnitude larger than for similar SiH_4 films with the same thickness [76,77,82]. It must be emphasized that the grain size increases with the thickness (in the 50-200 nm range) for both type of films [67,79]. Figure 18 shows transmission electron microscope (TEM) plan views of 80 nm-thick films after crystallisation at 540°C of SiH_4 and Si_2H_6 originated films.

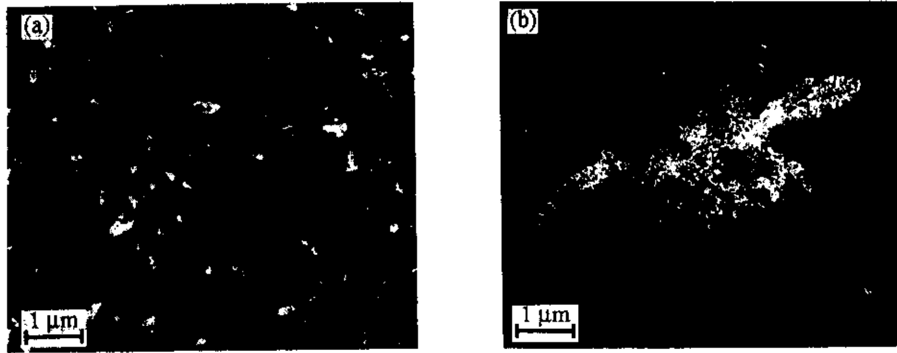


Figure 18 : Dark-field TEM plan views of 80 nm-thick films crystallised at 540°C for 65h; (a) SiH_4 originated film and (b) Si_2H_6 originated film.

3.1.3 The kinetics of solid phase crystallisation

In order to explain the differences in grain size and shape, after SPC, depending on the type of gas precursor gas used, we have performed an extensive study of the crystallisation of both type of films [82]. The solid phase crystallisation of an amorphous silicon film takes place by nucleation of clusters, which grow spontaneously when a critical size is attained. The growth proceeds by displacement of atoms from the amorphous phase to the crystalline phase. Within the framework of this theory [102], nucleation and growth rates, v_n and v_g, are assumed to be constant and thermally activated, and may hence be written as :

$$v_n = v_{no} \exp\left(-\frac{E_n}{kT}\right) \quad \text{and} \quad v_g = v_{go} \exp\left(-\frac{E_g}{kT}\right) \qquad (7)$$

where E_n and E_g are respectively the activation energy for the nucleation and growth rates.

Once the nucleus has reached its critical size, the growth of crystalline silicon in the amorphous matrix occurs by bond breaking and rearrangement at the a-Si / c-Si interface. The generally accepted atomistic model of solid phase growth in an impurity-free matrix relies on the a-Si / c-Si interface structure and mechanism proposed by Spaepen [103] and refined by Spaepen and Turnbull [104]. This interface consists of (111)-type terraces separated by [110]-type ledges. Crystal growth occurs by the movement of a broken bond running along the ledge, and a single broken bond allows for the reconstruction of a large number of crystalline sites. Hence, crystal growth can be viewed as resulting from a lateral motion of [110] ledges, leading to a layer by layer stacking of (111) planes. The activation enthalpy for the growth rate (E_g) is, in that case, the energy required to break a strained Si-Si bond at the interface. Williams and Elliman [105] and Williams [106] have extended the above picture, in order to take into account the effect of impurities. In their model, the growth sites at the a-Si/c-Si interface are kink-like steps on the [110] ledge and the growth process is controlled by the motion of such kinks along the ledge. As a result of the formation of strong bonds between certain impurity atoms and silicon (e.g. a Si-0 bond), the kink becomes pinned and ledge motion is therefore inhibited, leading to a slower growth rate. If most ledges are plagued by oxygen atoms, it is conceivable that the activation enthalpy of the growth process is increased to the energy necessary to break a (strained) Si-O bond.

The grain size of crystallised films depends on the maximum free enthalpy of the formation of a cluster $\Delta H^*=E_n-E_g$ and on the enthalpy of the growth process $\Delta h^*=E_g$ [102]. Different methods has been used to determine E_n and E_g : optical reflectivity [107], X-ray diffraction [85,108], transmission electron microscopy [109,110] and conductivity measurements [73]. We have used a combination of *in situ* electrical conductance analysis and grain size measurements by transmission electron microscopy, in order to precisely determine the above crystallisation parameters (E_n and E_g) [82]. The main results are presented below. Table 5 shows the data obtained for SiH_4 (T_d=550°C) and Si_2H_6 (T_d=480°C) thin films (80 nm) deposited at P_d=2 Torr in an UHVCVD system.

Table 5 : Crystallisation parameters for UHVCVD silane and disilane originated layers (after Kretz *et al.* [82])

	E_n [eV]	$\Delta h^*=E_g$ [eV]	$\Delta H^*=E_n-E_g$ [eV]
SiH_4	3.27 ± 0.06	2.67 ± 0.03	0.60 ± 0.07
Si_2H_6	4.78 ± 0.19	2.29 ± 0.16	2.49 ± 0.25

The Si_2H_6 films exhibit higher values of E_n compared to SiH_4 films (4.78 versus 3.27 eV). The values of E_g for both the silane and the disilane films are similarly low, and comparable with the ones obtained for electron beam deposited amorphous silicon in UHV conditions [107]. A possible explanation is the low contamination density of the layers [111], because activation energies of more than 3eV are typical [63,84,85] for classical LPCVD conditions, where much higher oxygen concentrations are present [112]. In order to confirm this assumption, secondary ion mass spectrometry (SIMS) measurements have been performed on SiH_4 and Si_2H_6 films obtained by UHVCVD. Table 6 summarises the oxygen and carbon concentrations in these layers as a function of the deposition temperature.

First, we note that these values are 2 to 3 orders of magnitude lower than those found in classical amorphous LPCVD or evaporated Si films [86,109]. Second, the oxygen content in Si_2H_6 films (~5.10^{16} at.cm^{-3}) deposited between 480 and 520°C is ten times lower than that in SiH_4 films (T_d=550°C). Finally, for Si_2H_6 films and T_d>520°C, one can see a significant increase in the concentration of oxygen and carbon. For example, films deposited at 560°C contains 2.10^{17} O atoms/cm^3 and 4.10^{17} C atoms/cm^3. This finding is rather surprising, since the purity of the films should be improved as the growth rate increases (75 nm/min at 560°C) for the same quantity of gas and therefore of impurities introduced in the reactor and also for the same background residual pressure. However, as

the surface is passivated by hydrogen atoms and since the surface Si-H bond is stable for T<520°C [95,101], there is an inhibition of oxygen and carbon adsorption at the surface of the films being deposited at low temperature. Hence, films deposited below 520°C contain less O and C atoms than films deposited at higher temperatures in spite of the increase of the deposition rate in the latter case.

Table 6 : Impurity concentrations of amorphous UHVCVD silicon films for various gas precursors and deposition conditions [74].

SiH_4 (sccm)	Si_2H_6 (sccm)	H_2 (sccm)	T_d (°C)	V_d (nm/min)	Oxygen ($at.cm^{-3}$)	Carbon ($at.cm^{-3}$)
500	0	1500	550	2.5	4.10^{17}	$\sim 10^{17}$
0	40	1960	460-520	1-20	$3\text{-}6.10^{16}$	10^{17}
0	40	1960	540	40	6.10^{16}	2.10^{17}
0	40	1960	560	75	2.10^{17}	4.10^{17}

As one can see on table 5, for Si_2H_6 films, ΔH^* is larger and Δh^* is lower than the corresponding values for SiH_4. Those energies, inducing slower nucleation and faster growth in the disilane case, are the reason for the larger grains compared to the silane films. The grains can grow to larger sizes before they impinge on their neighbours. The effect of impurities on the growth rate has already been stressed above. Similarly, a low impurity content will affect the nucleation rate, since it is well known that impurities are preferred nucleation sites. On the other hand, the disorder which exists in the amorphous films after deposition can also partially explain this behaviour [76,77,79] : at higher deposition temperature (i.e. 550°C as is necessary in order to obtain deposition from SiH_4 with an appreciable rate), the surface Si-H bond is not stable and the silicon species have a higher surface diffusivity and consequently, a local arrangement of silicon atoms close to the one of the crystal may be produced in the amorphous films. Such "more ordered" regions have a structure that resembles that of a stable nucleus and present favourable sites for nucleation during the annealing, resulting in a smaller ΔH^*, i.e. in a higher nucleation rate (see table 5). This idea has been confirmed by Kretz *et al.* who have studied the crystallisation of amorphous Si_2H_6 films deposited at 520 and 540°C in the mTorr range [113]. The films exhibit grain shapes (microstructure and size) which are very similar to the ones of SiH_4 films. Moreover, the activation energy for growth and nucleation are also very comparable to the ones of SiH_4 (E_g=2.7 eV and E_n=2.9 to 3.7 eV). Consequently, the parameters that govern the crystallisation of an amorphous film depend more on the deposition conditions (essentially the temperature and the pressure) than on the chemistry of the precursor gas [114].

As a conclusion, Si_2H_6 films, which can be deposited at a low temperature (480°C), exhibit a very large grain size after solid phase crystallisation (up to 5 µm). This property allows the fabrication of polysilicon TFTs with mobilities of up to 70 $cm^2v^{-1}s^{-1}$ [115], even without hydrogenation (see § 3.3).

3.1.4 Pulsed-laser crystallisation

Initiated by Soviet scientists [116], laser processing of semiconductors has emerged during the second half of the 1970s, and several conference proceedings underline the "explosive" developments of the field between 1978 and 1983 [117-123]. Pulsed laser annealing was first used to activate ion-implanted dopants in silicon and remove the corresponding lattice damage.

During irradiation of semiconductor materials with photons of energy $h\nu > E_g$ (E_g is the energy gap of the semiconductor), absorption takes place by excitation of electron-hole pairs across the gap. After a rapid thermal equilibration (10^{-14}s) of the photoexcited carriers, the energy is transferred to the lattice by phonon emission on a time scale of the order of 10^{-12}s [122].

The unique feature of pulsed laser processing is that the beam energy is deposited within roughly the absorption depth (α^{-1}) of the irradiated material during the pulse duration (τ). For the practical applications considered here, α^{-1} is smaller than the heat diffusion length in the irradiated material. This latter quantity is estimated by $(D\tau)^{1/2}$, where D is the thermal diffusivity which is temperature dependent ($D = \kappa/\rho C_p$ where κ is the thermal conductivity, C_p is the specific heat and ρ is the density of the semiconductor material under consideration). Hence, if the laser pulse duration is short (typically a few tens of ns for Q-switched solid-state lasers and excimer lasers), the heat diffusion length during irradiation will be small and the absorbed energy will be highly localised under the very surface of the irradiated film. In such conditions, melting can be induced in thin surface layers, whereas the underlying substrate remains practically unaffected by thermal effects.

For example, at UV wavelengths, the absorption depth in silicon is ~ 10^{-6}cm, whatever its structural state (crystalline, amorphous or even liquid). For a pulse duration of say, 20 ns, $(D\tau)^{1/2}$ in crystalline silicon would amount to ~ 450 nm (assuming D ~ 0.1 cm^2s^{-1} at an average temperature of 1000°C).

Thus, $\alpha^{-1} << (D\tau)^{1/2}$, and a rough estimate of the temperature rise in the $(D\tau)^{1/2}$ -thick layer is given by:

$$\Delta T = (1-R)I\tau / \rho C_p (D\tau)^{1/2} \quad (8)$$

where R is the reflection coefficient of the silicon surface at the wavelength of concern (~ 70% in the UV) and I is the laser power density. With the above values, a laser energy density ($I\tau$) of 0.37 J cm^{-2} would be needed to melt the 450 nm-thick surface layer of c-Si. Although on the low side, this value gives the correct order of magnitude. Detailed models based on the numerical resolution of the heat flow equation have been developed, which allow more precise evaluations [122,123]. In particular, the temperature variations of the different physical and thermodynamic constants are accounted for.

Although much of the early work on pulsed laser processing of semiconductors has been performed with solid-state lasers (e.g. Q-switched Ruby or Nd-YAG lasers), the technology is now clearly in favour of gas lasers and particularly the rare-gas halide excimer lasers. Solid-state lasers present large spatial inhomogeneities in the energy density of the beam; as a consequence, some kind of beam homogenisation is necessary (usually a light pipe) which produces high transmission losses. Also, the working distance from the output of the homogeniser has to be small and constant, as the homogenised beam is usually highly diverging. The overall process is therefore more complex, particularly when some form of beam scanning is necessary (in large area application for instance). Moreover, due to heat dissipation problems with YAG or Ruby crystals, the beam diameter cannot be made very large and for the same reason, the repetition rate is limited. Finally, solid-state lasers are highly coherent and interference effects can arise due to light scattering on dust particles, surface irregularities etc. (speckle phenomenon).

Excimer lasers (the denomination comes from the contraction of excited dimers) and particularly the rare-gas halide excimer lasers (which should actually be called exciplexes, from the contraction of excited complexes; examples are ArF, KrF, XeCl ...) excited by self-sustained electric discharges, offer the advantages of high average energy (up to 10 J/pulse [124]) and high efficiency. The beam energy density can be made uniform within 5% and even below over an area of more than 10 x 10 cm^2. Moreover, unlike solid-state lasers, excimer lasers exhibit very poor spatial coherence; as a consequence, the speckle effects are almost eliminated, which is an add-on advantage. Depending on the type of gaseous mixture used, the wavelength can be varied from 193 nm for ArF to 350 nm for XeF. Intermediate wavelengths at 249 and 308 nm can be obtained with KrF and XeCl complexes.

Excimer laser processing of thin films of a-Si is very attractive, because the a-Si material can be crystallised from the melt, without thermally affecting the underlying substrate [125,126]. Models have been established [122,123], which describe laser melting of silicon and its subsequent crystallisation by the downward penetration of the melt front, followed by an upward planar regrowth after heterogeneous nucleation at the maximum depth of penetration of the melt. However, the situation might not always be so simple, in particular when a-Si is of concern.

For instance, a thin a-Si layer on top of c-Si is transformed into c-Si after melting and regrowth only if the laser energy density is high enough to melt the entire a-Si layer throughout. For lower laser fluences, when the melt front penetrates only part-way through the a-Si layer, an unusual microstructure is observed, consisting of large-grained, rather columnar poly-Si in the near-surface region, standing on top of fine-grained, equiaxed and randomly oriented material [127,128].

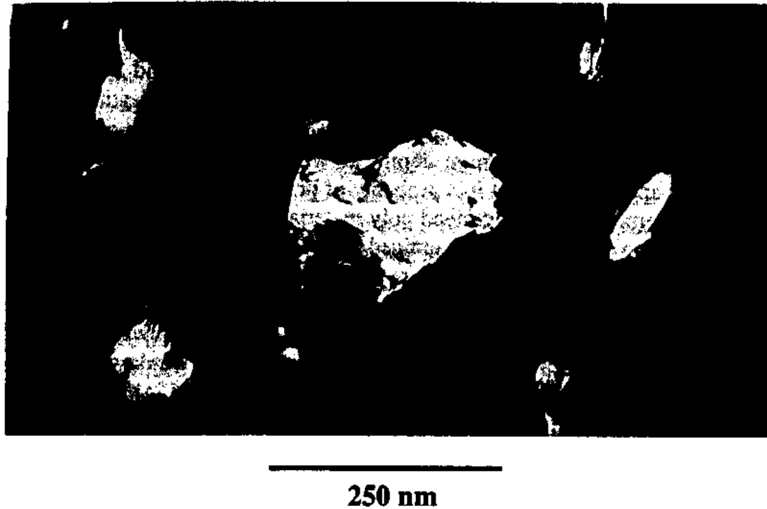
This behavior had originally been explained by the onset of an explosive crystallisation phenomenon initiated at the stationary liquid / amorphous solid interface as it stops to turn around [129]. Because the melting temperature of a-Si is 200-250°C below the one of c-Si [129,130], the latent heat of crystallisation released upon solidification of c-Si from the melt induces melting of a-Si. Since the latent heat of melting of c-Si is larger than the one of a-Si, the melting of a-Si can be self-sustained or explosive [131]. While

there is ample evidence of this self-propagating interior melting phenomenon [132], the nucleation mechanism of the fine-grained poly material appears to be rather unusual, as it has been proposed that c-Si would be nucleated at the moving liquid Si / a-Si interface [131]. Furthermore, it has also been shown that the explosive crystallisation phenomenon was in fact preceding the downward melt propagation [133], rather than occuring after the melt front had reached its maximum depth, as was originally beleived [129]. This distinction could appear futile, but it is probably of prime importance, because if the a-Si film is first transformed into fine-grained poly material by explosive crystallisation, then further melting has to occur in this fine-grained polysilicon. This could have some serious consequences on the melting models, because the thermodynamic and physical constants of a-Si are quite different from the ones of c-Si. Moreover, this explosive crystallisation is also probably at the origin of the phenomenon of "super lateral growth", by which very large polysilicon grains can be obtained in a narrow laser energy window, after irradiation and melting of thin a-Si layers on quartz or oxidised Si substrates [134].

The laser energy window leading to the obtaining of very large grains is very narrow, because it corresponds to a situation where most of the grains belonging to the original fine poly (first synthesised by explosive crystallisation) have been dissolved by the liquid and the few surviving clusters, which act as seeds, are sufficiently spatially separated to allow a large lateral regrowth to take place [134]. Grain sizes around 500 nm are obtained in 100 nm-thick poly-Si layers, after irradiation and melting, the substrate being held at room temperature. Larger grains can be obtained if the substrate temperature is raised during irradiation. If the laser energy density is slightly increased over the critical energy corresponding to the obtainment of very large grains, then the whole fine-grained poly is dissolved, no more surviving clusters are present and homogeneous nucleation occurs in the highly supercooled liquid. Actually, supercooling values of 500°C have been reported, leading to nucleation rates as high as 10^{29} $m^{-3}s^{-1}$ [135]; when this situation occurs, the corresponding grain size is of course very small [134].

Multishot irradiation has also been investigated, and even larger grain sizes have been obtained, still in a narrow laser energy window[136]. It is likely that in this case, the same mechanism of super lateral growth holds, but as the smaller grains are probably dissolved more rapidly than the large ones upon repetitive melting, large grains tend to grow at the expense of small grains.

When compared to a poly material obtained by SPC (particularly the ones crystallised from a Si_2H_6-originated a-Si precursor - see figure 18 and § 3.1.2), laser crystallised polysilicon tend to exhibit smaller grain sizes (except perhaps for multishot crystallisation), but the grains are very "clean", which means that there are few intragrain defects such as dislocations, stacking faults and twins. This is illustrated on figure 19, which shows a TEM plan view of a laser crystallised film with a thickness of 50 nm. This high crystalline quality is reflected by the performances of TFTs fabricated in laser crystallised polysilicon. Electron mobilities of 450 $cm^2V^{-1}s^{-1}$ have been reported by several laboratories (see § 3.3).



250 nm

Figure 19: TEM plan view of a poly-Si thin film (50 nm) obtained by laser crystallisation.

3.2. Low temperature silicon dioxide synthesis

The gate insulator material mainly used for the fabrication of polysilicon TFTs is silicon dioxide, because compared to Si_3N_4 for instance, it exhibits a lower density of interface states on crystalline silicon, together with a lower bulk trap density. For a device-grade material and process, it is necessary to obtain a moderate value of the interface state density (typically < 10^{11} cm^{-2} eV^{-1} measured on (100) monocrystalline silicon) and a high dielectric strength of the insulator (injection current <1 nA cm^{-2} for an electric field E < 4 MV cm^{-1}).

Various methods have been used, in order to obtain device-grade silicon dioxide at low temperatures, i.e. 650°C or below. These are essentially (i) oxidation (low temperature thermal or plasma) (ii) thermal chemical vapor deposition (thermal-CVD) and (iii) plasma enhanced chemical vapor deposition (PECVD). Additional methods which have been reported, such as reactive magnetron sputtering [137,138], evaporation [139] or liquid phase deposition [140] will not be discussed in this section as they are not in wide use.

Oxidation

Polysilicon thermal oxidation is directly borrowed from the monocrystalline MOS technology. As the integration level was increased, the gate insulator thickness of the elementary MOS transistor was continuously decreased, concomitantly with channel length and operating voltage. For sub-10 nm thickness, low temperature oxidation at about 850°C, under steam atmosphere, is commonly used for a better thickness control and repeatability. However, at temperatures compatible with the use of glass substrates, very long oxidation times are necessary, even in steam atmosphere, in order to obtain the gate oxide (typically about 30h and more [141]). In these conditions, the thermal shrinkage of the glass substrates becomes a major issue, especially for large surface processing. A pre-compaction anneal of the glass has to be performed at the maximum temperature of the process, for 200h or more [142].

In an effort to reduce the thermal budget (process temperature multiplied by process time) of the oxidation, several rate enhancement techniques such as high pressure oxidation, fluorine enhanced oxidation and plasma oxidation have been proposed.

In the analytical expression of the oxidation rate of silicon, the parabolic constant B is directly proportional to the partial pressure (P_{ox}) of the oxidising species in the gas phase (see L. E. Katz, chapter 3 in [70]). Thus, the oxide growth rate is proportional to P_{ox} for short oxidation times and to $P_{ox}^{1/2}$ for long ones. In any case, a substantial acceleration in the oxide growth rate is obtained as the pressure is increased. Mitra *et al.* have reported a growth rate of about 3.5 nm h^{-1} for polysilicon oxidation in pyrogenic steam at 15 atm and 650°C [143]. A dry oxygen anneal (2h at 15 atm) of the gate oxide was shown to improve the subthreshold slope value of TFTs by roughly a factor of four, from 0.74 V dec^{-1} to 0.18 V dec^{-1}, for a 100 nm-thick oxide. Moreover, Mitra *et al.* have claimed that the effect of oxidation enhancement along the polysilicon grain boundaries (described in [144]) could reduce the density of electrically active defects, thus improving the TFT characteristics [145]. However, although recently introduced for local oxidation of silicon in MOS technology [146] (LOCOS process), this high pressure oxidation method is probably not easy to adapt to large area substrates for safety and throughput reasons.

The addition of 30-600 ppm of NF_3 to O_2 has also been shown to increase the oxidation rate of silicon, approaching the one of wet oxidation. At 650°C, with 300 ppm of NF_3 in O_2, a 26 nm oxide can be grown on polysilicon in 10h [147]. However, TFT results have been reported only for an oxidation temperature of 800°C (80 nm thickness in 5h); in such conditions, an improvement of the electron mobility (38 cm^2 V^{-1} s^{-1} instead of 28) was observed as a consequence of the fluorine addition [147].

At this point, it must be stressed that for thermal oxidation processes, the oxidation rate is orientation dependent. Hence, since polysilicon thin films are textured, thermal oxidation can result in severe non-uniformities of the oxide and active layer thicknesses, together with a roughening of the SiO_2-active Si interface. As far as TFTs are concerned, this induces carrier scattering and a corresponding decrease in the field effect mobility. Also, grain boundaries in polysilicon, which have been shown to locally enhance the oxidation rate [144], are likely to induce more thickness non-uniformity and interface roughness.

Plasma oxidation is an electrochemical (field-assisted) oxidation method. In the anodic mode, the linear growth rate is limited by the ionic transport of the O^- species through the oxide, rather than by the surface reaction as is the case with thermal oxidation [148]. As this transport-limited mechanism does not seem to be thermally activated [149], larger growth rates can be obtained at low temperature (T < 400°C) compared to thermal

oxidation. Moreover, the oxidation rate is not orientation dependent which is an add-on advantage over thermal oxidation.

Using an electron cyclotron resonance (ECR) plasma, an oxide thickness of 60 nm has been obtained in one hour at 450°C for a microwave power of 400W [150]. ECR plasma enhanced oxidation has been used for the fabrication of polysilicon TFTs which exhibit high carrier mobilites, 80 $cm^2 V^{-1} s^{-1}$ for electrons and 69 $cm^2 V^{-1} s^{-1}$ for holes. The 45 nm-thick oxide was grown at 400°C, in pure O_2 for 2h [151]. At low electrical field, I(V) ramp characteristics are comparable to the ones of thermal oxides. However they show a higher injection current for electrical fields larger than 4 MV cm^{-1}.

The oxidation of the interface (1-5nm) can be coupled with a deposition technique [152,153] to reach the 100nm thickness range requested for most of the large area applications. This oxidation step can also be integrated in the crystallization procedure [137] .

Thermal chemical vapor deposition

Thermal chemical vapor deposition is the most widely used deposition process for the obtaining of thin films, whatever their nature (metals, semiconductors or insulators). As already stated, this process is based on the decomposition of one or more gaseous precursor(s) either in the gas phase (partial decomposition) or at the surface of the substrate. The growth mechanism is thermally activated and the deposition temperatures range from about room temperature to more than 1000°C [154]. Deposition can proceed under atmospheric pressure (APCVD) or low pressure (LPCVD) conditions. The major advances in the last decade have concerned the comprehension and the modelling of the deposition processes and as a consequence, the design tools to fabricate efficient production systems.

Silicon dioxide thin films can be obtained using SiH_4-O_2 mixtures in the practical temperature range of 350-450°C. The deposition rate is optimum for an O_2 / SiH_4 ratio of about 10 at 400°C. This ratio is strongly temperature and reactor dependent. Although CVD is not the optimal process from the point of view of interface and bulk qualities, it has been used by most companies and research laboratories involved in polysilicon TFT development [155-161]. The major reasons for its wide use are the availability of high throughput / large area deposition systems and the larger up-time of the CVD systems, when compared to the one of PECVD systems.

Figure 20 presents the oxide deposition rate versus pressure and temperature for a fixed O_2 to SiH_4 ratio of 15 [162]. The results have been obtained in quite ideal conditions (loadlock chamber, UHV-grade background pressure, cold wall chamber...). At high pressure (p > 1 Torr) the obtaining of reasonable deposition rates (d_r > 10 nm min^{-1}) is rendered difficult by the homogeneous gas phase reactions. CVD oxides deposited at low temperature (400-450°C) exhibit poor electrical quality with high leakage currents, low breakdown fields and strong carrier trapping [155,162]. The incorporation of hydroxyl groups (OH) due to the partial reaction of SiH_4 and O_2 in the gas phase could explain this poor quality. However, the electrical characteristics can be improved by increasing the

deposition temperature (575°C) [162] or by implementing a subsequent high temperature anneal, typically at 600°C for a few hours [155,163]. This improvement can be explained as a result of weak hydrogen bond breaking resulting in material densification and the elimination of hydroxyl groups. The high temperature anneal can be performed just after oxide deposition [159] or it can be the dopant activation anneal when ion implanted poly-Si TFTs are of concern [155]. After annealing at much higher temperature (950°C), CVD oxides can well compete with thermal oxides obtained at similar temperature [164], but this range of temperature is out of interest for the subject reviewed in the present paper. Such improvements are also observed, though to a lesser extent, for PECVD oxides [165], deposited by using radiofrequency plasma excitation.

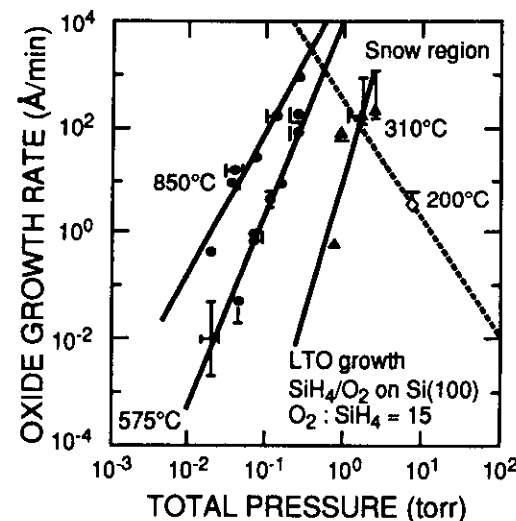


Figure 20 : LPCVD oxide deposition rate in the SiH_4-O_2 system (after Liehr and Cohen [162]).

Plasma enhanced chemical vapor deposition

The enhancement of CVD reactions using plasma excitation allows a reduction of the processing temperature, typically by a few hundreds of °C. CVD reactions such as the deposition of Si_3N_4 (using SiH_4-NH_3 or SiH_4-N_2 mixtures) or the deposition of SiO_2 (using SiH_4-N_2O mixture), which were not compatible with the low temperature requirements of glass substrates, become possible when the plasma enhances the dissociation of the gas molecules [18]. The development of large area PECVD systems has been boosted by the increasing demand from the a-Si:H TFT AMLCDs manufacturers (see § 2.4). As quoted above, industrial deposition systems are now available for at least 350mm x 450mm glass plates [50,52]. Materials concerned are mainly a-Si:H and Si_3N_4 (see § 2.3.) but the deposition of SiO_2 is also possible. Uniformity and quality can be achieved at high deposition rate (a few tens of nm min^{-1}) through the use of shower head

gas injection systems. Also, the quality of layers deposited at high rates can benefit from the use of higher plasma excitation frequencies (up to 60 MHz) [52].

The deposition of SiO_2 for primary insulation of a-Si:H TFTs has been introduced by IBM in the mid 80's [165]. The two main characteristics are (i) the use of an He-diluted gas mixture to prevent homogeneous reactions between N_2O and SiH_4 in the gas phase and (ii) the reduction of the deposition rates down to the 6 nm min^{-1} range, in order to allow the complete oxidation of the silicon atoms incorporated in the films. The density of electrical defects is therefore reduced because of the corresponding reduction in the density of dangling and stray bonds. It has been shown that, as far as physical properties - stoichiometry, density - are concerned, high quality layers can be obtained at a substrate temperature of 350°C. However, a 400°C anneal in forming gas (10% H_2 in N_2) is necessary in order to achieve low values of interface state density (< 4 10^{10} cm^{-2} eV^{-1} on (100) Si).

Although this technique presents an obvious interest, especially in terms of electrical properties, it is, to our knowledge, not widely used in spite of some recent reports concerning a-Si:H [166] as well as poly-Si [167] TFTs. In the former case, it has been shown that the silicon dioxide surface stoichiometry was modified by the exposition to the H-containing plasma during the first stages of a-Si:H deposition [168] (see § 2.2. for the description of the bottom-gate TFT). Furthermore, this He-diluted PECVD process has also been used with some success for the fabrication of MOSFETs on monocrystalline Si [169] but in that case, the advantage over thermal oxidation is not obvious. A recent report shows the possible use of tetraethylorthosilicate (TEOS) in combination with O_2 at 315°C for the deposition of device-grade quality SiO_2 [170].

Over the last few years, microwave excitation of plasmas has been introduced in order to improve etching and deposition processes [171]. Of particular interest is the electron cyclotron resonance (ECR) plasma, which allows the deposition of high quality dielectric layers. This method was first introduced by NTT in Japan [172]. Figure 21 presents a schematic side view of the ECR-type plasma system used by Matsuo and Kiuchi [172]. The plasma chamber is a monomode microwave cavity which absorbs the microwave energy transfered from the waveguide through a quartz window. The simultaneous presence of the high magnetic field and microwave energy with the proper values for ECR conditions (875 G - 2.45 GHz) allows the obtaining of very high electron densities in the source (about 10^{12} cm^{-3}). However, the magnetic field lines diverge from the source to the substrate which could affect the process uniformity, as they determine the trajectories of the high energy electrons. Some improvements have been achieved either by placing the substrate in the ECR zone [173] or by adding a second magnetic coil around the substrate to render the magnetic field lines more parallel [174].

The specific mass of the dielectric films (Si_3N_4 and SiO_2) deposited by ECR-PECVD can be comparable to that of films obtained by CVD at much higher temperatures. This can be deduced from wet etch rate measurements [172]. Among the advantages of the ECR SiO_2 layers is their resistance to the diffusion of water into the devices, with a corresponding increase in the resistance to hot carrier stressing [175].

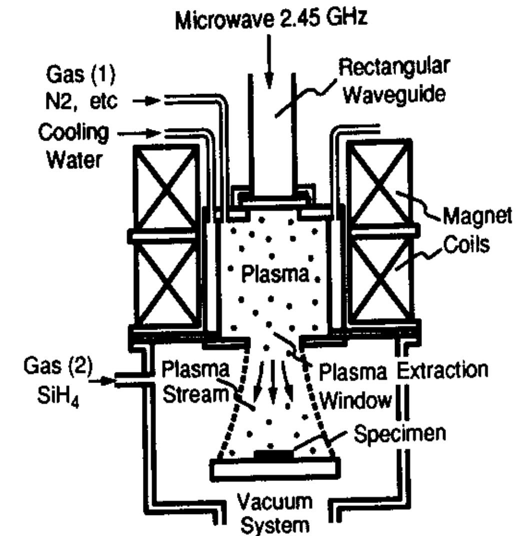


Figure 21: Schematic side view of an ECR-type plasma system (after Matsuo and Kiuchi, [172])

The ECR system has been used for the first time by Seiko-Epson for the fabrication of polysilicon TFTs and AMLCDs [176]. The interface state density on silicon was reduced by one order of magnitude moving from APCVD-SiO_2 (10^{12} cm^{-2}) to ECR-SiO_2 (10^{11} cm^{-2}). Because of the low deposition rate of the ECR system, a dual layer insulator was used, with an APCVD-SiO_2 layer on top of the ECR-SiO_2 one [176]. A recent publication from the same group reports on the use of a single ECR-SiO_2 layer for low-temperature TFT fabrication, confirming the interest of the method [177]. A very large ECR source (250mm) has been commercially available from Astex for a few years, but to our knowledge, it has not yet been implemented in a large area deposition system.

The distributed electron cyclotron resonance (DECR) sources have been introduced to eliminate some of the drawbacks of the ECR sources, including the uniformity problems. Figure 22 presents the schematic top-view of a DECR-type plasma chamber. In the distributed configuration, magnetic field lines are not diverging from the plasma source to the substrate as in the ECR case. The multipolar magnetic field traps the energetic electrons produced in each ECR zone at the periphery of the reactor. The complete description of the DECR plasma principle can be found in the literature [178].

High quality SiO_2 layers can be deposited without the need for substrate heating [179,180]; this is a key point as far as the developement of a large area deposition

industrial machine is concerned. The deposition of SiO_2 layers on A5 substrates with a uniformity of ± 5% has been reported [181].

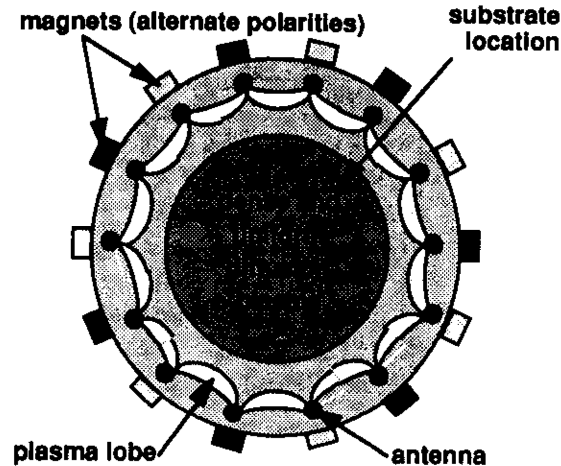


Figure 22 : Schematic top view of a DECR-type plasma chamber.

Quasistatic-ramp I(V) characteristics have been used to assess the electrical integrity of the oxide. Figure 23 compares the characteristics measured on several Al - DECR SiO_2 - Si diodes which are biased in the accumulation regime. The films were obtained without intentional heating of the substrate. In one case, the SiO_2 layer was annealed for 20h at 580°C under O_2 atmosphere before metallisation and in both cases, the diodes were annealed at 450°C for 1 hour in forming gas, after aluminum evaporation. I(V) characteristics deviate from the capacitive current level for an electrical field larger than 7 and 6 MV cm^{-1} respectively. These two values, obtained for 55 nm- thick films show that DECR oxide competes well with thermal oxide even with a much reduced thermal budget (T_{max}=450°C).

Several reasons can be invoked to explain the high electrical quality of the DECR SiO_2 films;

(i) first, it is emphasised that the deposition under high fluxes of low energy ions and electrons densifies the films without inducing defects.

(ii) Second, it is noted that the DECR discharge can be sustained in a mixture of pure SiH_4 and O_2, thus reducing the incorporation of nitrogen impurities. Considering the efficiency of the DECR plasma excitation, the Si radicals and atoms are readily oxidised at the surface of the film, which reduces the number of stray bonds (Si-Si, Si-H) and dangling bonds within the SiO_2 films.

(iii) Third, the experiments presented above have been performed in a clean deposition system using a load lock chamber associated with a high speed turbomolecular pump. This prevents contamination of the films by the background residual pressure.

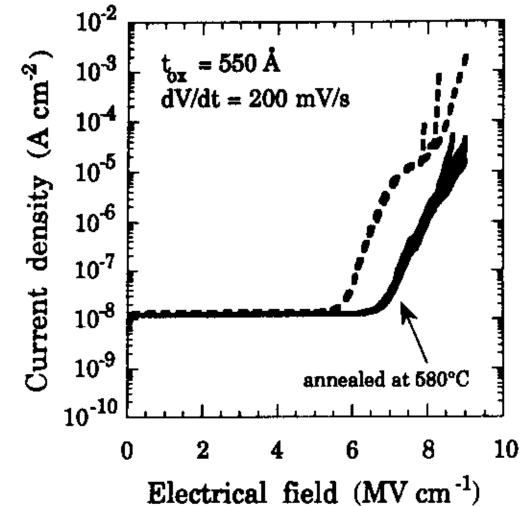


Figure 23: Quasistatic I(V) ramps of Al - DECR SiO_2 -Si diodes. See text for comments.

TFTs have been fabricated, using the DECR SiO_2 film as gate insulator. Monocrystalline silicon on insulator (SOI) MOSFETs exhibit an electron mobility of 640 $cm^2 V^{-1} s^{-1}$ [182]. This represents a state of the art value for SOI transistors on SIMOX substrates [183]. Polysilicon TFTs have also been fabricated with an electron mobility of 70 $cm^2 V^{-1} s^{-1}$ and a hole mobility of 40 $cm^2 V^{-1} s^{-1}$ [115]. Again these are state of the art values for the solid-phase crystallisation (SPC) process considered (see table 9).

2.3. Polysilicon TFTs

The polysilicon thin film transistor (poly-Si TFT) operates very much like the MOSFET on monocrystalline silicon. Compared to bulk Si or SOI, the substrate cannot be biased as it is an insulator for most of the large area electronics applications.

The non-perfect crystalline nature of the poly-Si material introduces electronic states in the forbidden gap that produce peculiar features in the devices. These states originate from localised defects such as grain boundaries, but also intragrain defects including dislocations, stacking faults and twins. The electrical behaviour of polysilicon in TFTs can be adequately described by assuming that an effective density of states (DOS) exists [184,185], as is the case with a-Si:H, and that this DOS is spatially uniform across the entire material. The fact that the defects tend to be more localised than in a-Si:H can be

neglected, considering that the grain size is, usually, much smaller than the gate size of the TFT and that the intra-grain defect density (which definitely has to be accounted for) can be considered as constant and reproducible from grain to grain. On the basis of this assumption, it is possible to extract the effective DOS from I-V measurements on TFTs and the results agree quite well with results obtained by DLTS in the energy range were they can be compared [186]. Furthermore, it is possible to develop device and circuit simulators whose accuracy is much higher and implementation much simpler than those based on pure grain boundary models. The mid-gap density of deep levels in poly-Si is higher than in a-Si:H. For this reason, the threshold voltage values in poly-Si TFTs also tend to be larger, even if the energy excursion from mid-gap to the bottom of the conduction (or the top of the valence) band is smaller.

In poly-Si TFTs, the source and drain are electrically reversible which means that the channel current (I_{ds}) can flow from source to drain or drain to source depending on the polarity of V_{ds}. The processing sequences and performances should be compared to their SOI counterparts [187].

Processing sequences

The most frequently used structure for poly-Si TFTs is the top gate self-aligned one (see figure 24).

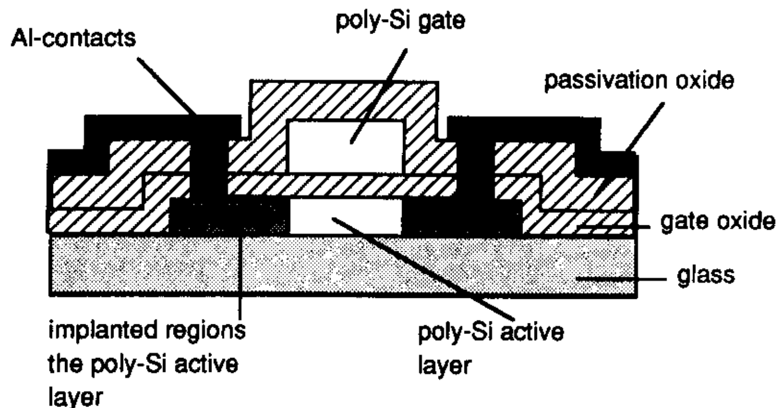


Figure 24: Cross-section of a self-aligned top gate polysilicon TFT.

This is because of the compatibility of the materials used (hard glasses, polysilicon, silicon dioxide) with the highest necessary temperature step, namely the activation annealing of the ion implanted source and drain regions. This activation is still satisfactory even for a 600°C furnace annealing [155]. As the channel resistance in the on-state ($V_{gs} - V_t > 10V$) is of the order of 50 kΩ/square, source and drain resistance values below 1 kΩ/square are typically required and easily obtained. As compared to a-Si:H TFTs, the absence of gate-to-source and gate-to-drain overlaps (due to the self-aligned implantation)

reduces the values of parasitics C_{gs} and C_{gd} capacitances which improves the TFT operation speed.

Depending on the ion species implanted for source and drain doping, n-type or p-type operation is achieved (NMOS or PMOS TFT). The devices always operate in the accumulation mode.

The glass substrates used in low-temperature poly-Si technology are somewhat different from those employed for a-Si:H technology. Their strain-point temperature, T_s (temperature at which the viscosity of the glass is $10^{14.5}$ poises), is about 50°C larger. In fact, even if the processing temperature is kept below T_s - 100°C, a significant compaction of the glass is observed, which affects the alignement from mask to mask. It should be emphasised that the glass compaction is not reproducible and not isotropic and cannot be easily compensated for by currently available steppers. This compaction is usually reduced as much as possible by using pre-compacted glass (very long time anneal at the maximum temperature of the process) [142].

Table 7 indicates the common glasses used for poly-Si technology and compares them with the most popular glass used for a-SiH TFTs and AMLCDs, i.e. the Corning 7059. All the glasses mentioned in table 7 are labelled "sodium-free". However, they usually contain a few hundreds ppm of Na_2O.

Table 7: Composition of the major "hard glasses" used for poly-Si TFT processing, compared to 7059.

Glass code	composition	Strain-point temperature (°C)
Corning 7059	Barium aluminoborosilicate	593
Corning 1737	Alkaline-earth aluminosilicate	666
Hoya Na40	Alkaline-earth-zinc-lead aluminosilicate	655
NEG OA-2	Alkaline-earth-zinc aluminoborosilicate	645

In order to avoid outdiffusion of impurities (particularly sodium and potassium compounds) from the glass substrates during processing, these are usually capped with Si_3N_4 or SiO_2 layers.

TFTs (n-type or p-type) are obtained using a four mask sequence. Table 8 lists the fabrication steps of the "standard" SPC process.

Compared to the processing flow chart of a-Si:H TFTs (see table 2), the poly-Si TFT fabrication in its "standard" version, is associated with repeated steps at high temperature (T_{sub} > 450°C). The high temperature steps are the deposition of the active layer and its crystallisation (steps 2 and 3), the deposition of the gate polysilicon material (step 6), the deposition of the gate oxide and of the gate passivation (steps 5 and 9) and the implantation activation annealing (step 10). The "standard" version of the poly-Si TFT fabrication sequence mainly uses equipments developed for Si-integrated circuits fabrication.

Table 8: technological flow chart of the standard SPC poly-Si TFT process.

step	description	mask
1	hard glass capping layers deposition	
2	active layer deposition using SiH_4-LPCVD at 550°C	
3	crystallisation at 600°C for at least 10h	
4	active layer definition	1
5	gate insulator deposition using APCVD at 450°C	
6	polysilicon gate deposition	
7	gate definition	2
8	contact implantation using an ion implanter	
9	gate passivation using APCVD oxide	
10	implantation activation annealing at 600°C (for a few hours)	
11	contact windows opening	3
12	aluminum evaporation	
13	aluminum contacts definition	4
14	aluminum sintering	
15	hydrogenation using H_2 plasma at 300°C (for a few hours)	

In order to compete with a-Si:H TFT-based products, which means that process cost and complexity should be comparable, much efforts have been devoted to the reduction of the thermal budget. From that point of view, the techniques listed below have been introduced for a few years:

a) the use of Si_2H_6 instead of SiH_4 as precursor for the deposition of amorphous silicon by LPCVD (steps 2 and 6). The deposition temperature can be reduced to about 450°C (compare figures 16 and 17);

b) the use of specific low pressure deposition processes. As-deposited polysilicon films (direct poly) can be obtained, which suppresses step 3 (see § 3.1.1). Another possibility is to deposit amorphous thin films which exhibit very short incubation and crystallisation times, which reduces step 3 to a few hours [113];

c) the use of rapid thermal annealing (RTA). The crystallisation time (step 3) can be reduced to about one minute but at higher temperature, 750°C [188] or to a few seconds using very rapid thermal processing (VRTP) under non-equilibrium conditions [189]. However, as the nucleation rate is increased at high temperatures, small grain sizes are obtained which is likely to reduce carrier mobilities in devices. An interesting point concerning RTA is that it can be used for rapid activation annealing of implanted dopants;

d) the use of pulsed laser crystallisation (see § 3.1.4). Here, the energy is deposited during a very short time, in a small thickness (corresponding to the absorbtion depth) and thermal equilibration is not attained during the irradiation. With a pulse duration τ of a few 10^{-8} s and given the thermal diffusivity of glass (~ 8 10^{-3} cm^2s^{-1}) the thermal diffusion length is around 100 nm. Hence, the glass is not thermally affected, whereas silicon is melted. Such a process can be used for crystallisation as well as for dopant activation;

e) the use of ion shower implantation, where PH_x or B_xH_y ions produced by a plasma discharge are accelerated by a negatively biased grid. A very low temperature activation annealing (300°C) have been reported [177] for this process, which suppresses step 10. Moreover, it has recently been shown that the implantation damage could be self-recovered [190] by the so-called ion beam induced epitaxial crystallisation phenemenon [191] if the dose is high enough. Such ion shower systems are becoming large area compatible as they benefit from the evolution of PECVD systems. Using the same implantation apparatus, laser activation anneal of the contacts has also been reported [192] ;

f) the use of ECR or DECR - deposited oxides. The temperature of step 5 is reduced to about 100°C and it should be emphasised that these particular oxides do not need a post-deposition densification anneal which is of interest for e.g. a very low temperature laser process.

Device characteristics

The way to describe the poly-Si TFT device characteristics is similar to that presented for a-Si:H TFTs (see § 2.2). The main features of poly-Si TFTs will be described and compared to those of a-Si:H TFTs.

Figure 25 presents the transfer characteristics $I_{ds}=f(V_{gs})$ for constant values of V_{ds}, of a n-type poly-Si TFT. The channel width and length are respectively 40 µm and 20 µm (two 10 µm-length gates in serie). I_{ds} can be controlled over 6 to 7 decades depending on the V_{ds} value, as can be seen in figure 25.

Three different regions can be identified :

- for $V_{gs} < 0V$, the "off-state" region.

It can be observed that the leakage current density (per µm of channel width) depends largely on V_{ds} and V_{gs} for $V_{ds} > 3V$. In the off-state, the current flow is inhibited by the formation of a reversed-biased p^+-n^+ junction at the channel drain interface. The leakage current is induced at this junction by the simultaneous presence of electrically active defects and high electrical fields. The leakage mechanism has been assigned to phonon-assisted tunneling from traps [193].

For n-type TFTs, off-current densities measured at room temperature in a "dark" box, are often reported for V_{ds} = 5V and V_{gs} = -10V. The values lie between 0.1 and 10 pA μm^{-1} (see table 9). The leakage current density is about one or two decades larger than that of a-Si:H TFTs, because of the different leakage mechanism. In particular a large drain voltage dependence is observed for poly-Si TFTs as opposed to a-Si:H TFTs (see figure 25). However, when operating in a system like an AMLCD, extrinsic parameters like temperature and light flux can influence the leakage current and the comparison between a-Si:H and poly-Si TFT leakage performances has to be made carrefully. A

spectacular reduction of leakage current density in poly-Si TFTs is obtained through the use of lightly doped drain (LDD) structures which reduce the electrical field value at the channel / drain junction and then flattens the I_{ds} versus V_{gs} curve in the off-state [145].

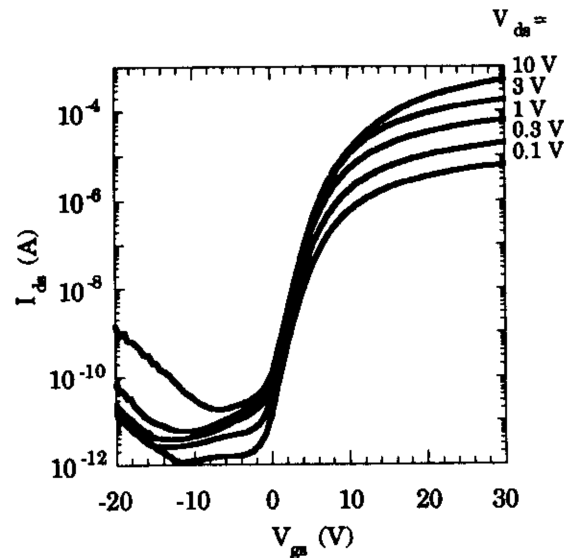


Figure 25: Typical transfer characteristics of a poly-Si TFT; channel width = 40 μm and channel length = 20 μm (2 x 10 μm).

- for V_{gs} > 10 V, the "on-state" region.

As with a-Si:H TFTs, the electron mobility value can be extracted from the slope of I_{ds} (linear scale) versus V_{gs} at low drain voltage (0.1V) in the linear regime or from the slope of $I_{ds}^{1/2}$ (linear scale) versus V_{gs} at high drain voltage (10V) in the saturation regime. The intersection of the linear fit with the voltage axis gives the threshold voltage (V_t). Again, the determination procedure is the same as for a-Si TFTs (see § 2.2).

Electron mobility values obtained in low-temperature TFTs lie between 25 and 450 $cm^2V^{-1}s^{-1}$ depending on the process conditions (see table 9) while those of holes are about 30-50% lower. The threshold voltages for n-type TFTs are between 2 and 7 V. This dispersion of the data indicates the weigth of the process and of the material quality in the obtaining of good values. The carrier mobilities in poly-Si TFTs are reduced, as compared to the ones in monocrystalline Si, by the presence of traps. The best values are achieved in high crystalline quality poly-Si layers, i.e. in laser-crystallised poly-Si.

- for $0<V_{gs}<V_t$, the "sub-threshold" region.

The I_{ds} current increases exponentially with the gate voltage. The subthreshold slope S can be expressed as:

$$S= S_o\ (1 + C_d / C_{ox} + C_t / C_{ox}) \qquad (9)$$

where S_o = 2.3 kT/q, C_d is the differential depletion layer capacitance and C_t the overall defect differential capacitance (these defects are either located at the interface between SiO_2 and poly-Si, at the grain boundaries in the poly-Si layer or inside the poly-Si grains).

The reported values of S for poly-Si TFTs are between 0.2 V dec^{-1} and 2 V dec^{-1} depending on the active layer and gate oxide layer thicknesses, grain size and intra-grain defects, hydrogenation process efficiency (see table 9). The minimum value (S_o) of about 60 mV dec^{-1} (at room temperature) can only be obtained on monocrytalline SOI TFTs. One way to reduce the deleterious influence of defects on the S value is to use very thin layers of gate oxide in order to increase C_{ox} as much as possible [138]. As a value of 0.8 V dec^{-1} is typical of a 1000 Å-thick gate oxide, subthreshold slopes below 0.2 V dec^{-1} can be obtained for a sub 200 Å-thick gate oxide. However, it is worth pointing out that problems of uniformity and repeatability can arise when small gate oxide thicknesses are of concern.

A key factor for the obtaining of low threshold voltage values is the implementation of an efficient hydrogenation process. We have previously emphasised the very important role of hydrogen in the a-Si:H network, in order to obtain suitable transistor characteristics. Although the electron mobility of a-Si:H TFTs is very low, in the 1 $cm^2V^{-1}s^{-1}$ range, subthreshold slopes of about 0.5 V dec^{-1} can be achieved thanks to the passivation of deep defects in the gap of the a-Si:H. The effect of hydrogenation is similar in poly-Si material, as hydrogen saturates dangling bonds and breaks the highly strained bonds, thus reducing the deep levels and sharpening the band tails. As the polysilicon processing sequence involves several high temperature steps (T_s>350°C), hydrogenation appears at the end of the flow chart. Although other methods have been proposed [55,194], plasma hydrogenation is the most widely used. Since the pionnering work of Kamins [195], several reports have pointed out the importance of this particular step [83,196-198].

Table 9 shows some significant results published on poly-Si TFT characteristics. Inspection of it shows that the highest values of the electron mobility are obtained using pulsed laser crystallisation (see § 3.1.4). This can be related to the fact that the intragrain defect (twins, dislocations...) density is much lower when laser crystallisation is implemented (compare figures 18 and 19). Moreover, grain boundaries in laser-crystallised material are well defined and sharp as opposed to the case of SPC. As a consequence, a lower value of the DOS is anticipated, which is confirmed by the reduced values of the subthreshold slope and threshold voltage (see table 1).

While the electrical characteristics of TFTs fabricated using pulsed laser crystallisation are definitely better, the uniformity of these characteristics turns out to be a

problem [205,206]. As usual laser beams are typically of small size (say 1 to 5 cm^2), the beam has to be scanned over the plate if large area substrates are used. TFTs fabricated in the regions of overlap exhibit lower electron mobilities [205,206]. This non-uniformity is still noticeable on a semi-logarithmic scale ! [205]. The problems can be solved either by using a high energy / large area beam [203] or by carefully optimising the film thickness and substrate temperature [206]. Finally, as a result of the higher electron mobilities in the poly-Si TFTs obtained by pulsed laser crystallisation, hot carrier degradations (see below, figure 26 and comments) could be worsened [207].

Table 9 : Recent results published on poly-Si TFT performances. (SPC) refers to solid phase crystallisation process as (L) refers to pulsed laser-crystallisation process.

Ref.	Company involved	T_{max} (°C)	μ, (cm^2 $V^{-1}s^{-1}$)	S ($V dec^{-1}$)	V_t (V)	I_{off}, (pA μm^{-1})(a)
[199]	Sony	270 (L)	450	0.25	1.1	-
[194]	IMEC	630 (SPC)	55	1.05	5	-
		630 (L)	140	0.5	1.5	0.1
[145](c)	Philips	650 (SPC)	34	0.3	- 2.5	1.5
[155]		620 (SPC)	27	0.95	~ 6	0.2
[200]		- (L)	160	0.6	~ 2	2
[196]	Xerox	600 (SPC)	40	0.6	2	0.15
[201]		350 (L)	50	0.33	~ 1	1(b)
[157]	Hitachi	600 (SPC)	37	1.2	6.2	10
[192]		450 (L)	65	0.85	~ 4	~ 0.5
[158]	Seiko	600 (SPC)	24	0.9	~ 5	0.5
[177]		550 (L)	38	1	~ 5	0.2
[202]	Thomson	580 (SPC)	65	1	6.5	0.1
[203]		580 (L)	40	0.6	5	0.6
[204]	NEC	600 (L)	140	0.7	~ 5	50(b)

(a) $V_{ds} = 5$ V and $V_{gs} = -10$ V

(b) $V_{gs} = -5$ V

(c) p-type, with Lightly Doped Drain structures

As far as AMLCD fabrication is concerned, a very low leakage current density has to be obtained for the TFTs of the matrix in the off-state and this can still be a problem for laser-crystallised poly-Si (see table 9). Laser crystallisation is a low temperature technique and as such, it is compatible with the a-Si:H existing processes. Hence, poly-Si can be selectively crystallised at the periphery of the glass plate, enabling the integration of the driving circuitry (or of part of it), while keeping a-Si:H TFTs with very low leakage for pixel switching. Such "dual" technology has been proposed with bottom-gate [201,205,208] and top-gate TFT architectures [209]. However, when the amorphous precursor is highly hydrogenated (such as PECVD material which contains about 10 at% of hydrogen - see § 2.1.), much care has to be taken during laser irradiation to prevent the formation of hydrogen bubles which induce a very rough poly-Si surface. Selective

dehydrogenation at the periphery can be achieved with sequentiel irradiations at increasing laser energies [201].

The average grain size, which is about 200-500 nm for the standard pulsed laser crystallisation process can be dramatically increased when the substrates are locally thinned [210]. This drastically reduces the solidification rate and results in grain sizes of 50 µm and more. The technique allows the obtaining of electron mobilities in excess of 600 $cm^2V^{-1}s^{-1}$ [211], which is as high as those obtained on monocrystalline SOI [183]. However, the implementation of the method on large area substrates is not obvious.

Figure 26 presents the output characteristics $I_{ds} = f(V_{ds})$ for constant values of V_{gs}, of a n-type poly-Si TFT. The channel width and length are respectively 40 µm and 20 µm (two 10 µm-length gates in serie).

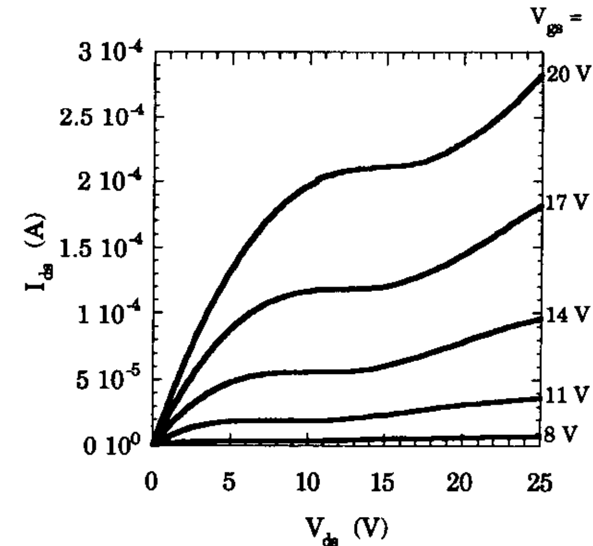


Figure 26: Typical output characteristics of a poly-Si TFT, channel width = 40 µm and chanel length = 20 µm (2 x 10 µm).

For the low V_{ds} range, I_{ds} increases with V_{ds} and then saturates as in long channel monocrystalline MOSFETs. For V_{ds} larger than a certain value V_{ds0}, which depends on V_{gs}, the drain current increases dramatically. For smaller channel lengths (L = 5 or 10 µm), the saturation regime can even be difficult to identify [115]. This regime is often called the "kink" regime, by analogy with the phenomenon occuring in SOI MOSFETs at short channel lengths [212]. However, in poly-Si TFTs, it is not strictly a "kink" effect as the phenomenon of second saturation is highly gate-voltage dependent. As a matter of fact, in figure 26, for V_{gs}-V_t > 5V (V_t=10V), I_{ds} increases continuously after the saturation, a

behaviour which is rather similar to the breakdown regime in monocrystalline Si MOSFETs. For V_{gs} around V_t, two saturation regimes can indeed be identified before breakdown, the second one being analogous to the "kink" effect reported in SOI MOSFETs. The reasons why these effects appear for very long channel as compared to Si MOSFET are not yet clear. The kink effect disappears in fully-depleted SOI MOSFETS [212], when the channel thickness is reduced to about 100 nm. However, in poly-Si TFTs, it is still observed for a channel thickness in that range.

It is now well accepted that operating in this so-called "kink" regime can significantly affect the device parameters, especially the transconductance in the linear regime [213]. The observed degradations are induced by the hot carriers produced at the channnel-drain junction under high V_{ds} bias. They can create interface state defects and trapped charges in the gate oxide which affect on- and off- currents as well. In particular, this effect can be used to reduce the off-current of poly-Si TFTs [214]. However, the instability issue of poly-Si TFTs is not as critical as that of a-Si:H TFTs. Lifetime of poly-Si TFTs (defined as the time for which on-current falls by 30% under stress) can exceed a few years [207] and various circuit applications have been demonstrated (see below).

3.4 Polysilicon TFTs Circuit Application

The performances of poly-Si TFTs make these devices ideal candidates for both digital and analog circuits implementation on large area non-refractory substrates. The advantages of poly-Si have led to its use in a variety of applications, such as AMLCDs with integrated drivers [215], video fluorescent active matrix displays [216], printer heads [217], linear image sensors [218,219], load devices in static random acces memories [220], control logic in power devices [221], operational amplifiers for neural networks [222].

An explanation of why poly-Si has rapidly become the material of choice for large area circuit integration, can be found in an important figure of merit used for digital circuits, the characteristic processing time τ_P. This quantity is given by :

$$\tau_P = \frac{L(L+L_D)}{\mu(V_S - V_t)} \qquad (10)$$

where L is the channel length, L_D the gate-to-source / drain overlap, μ is the field effect mobility, V_S the supply voltage, and V_t the threshold voltage. The lower τ_P, the higher the speed attainable by logic circuits. It can be seen that high mobilities and low gate overlaps both contribute to reducing τ_P. The field effect mobility of poly-Si TFTs is more than two orders of magnitude higher than in a-Si:H and of the same order of magnitude than in CdSe. However, in the case of poly-Si, self-aligned structures (i.e. with zero overlap) are easily fabricated, while they are difficult to obtain in the other two technologies. Moreover, poly-Si offer the advantage of having both n- and p-type devices so that both single channel (NMOS or PMOS) and complementary (CMOS) circuits are possible.

By far the most developed present application of poly-Si is the integration of driving circuits onto AMLCDs. In 1983 the first shift register obtained on low-temperature poly-Si was shown [223], followed, one year after, by the first fully integrated black and white display [224] fabricated in a CMOS technology and capable of 1MHz operation. Since then, the use of improved processes like SPC and laser crystallisation has brought the operating frequency to over 10 MHz, although, by clever circuit techniques it is possible to address high resolution displays with clock signals of the order of few MHz only [225]. The integration of drivers is becoming of primary importance for the development of both high definition TV (HDTV) and workstation projectors (see figure 27 for an example of such a circuit).

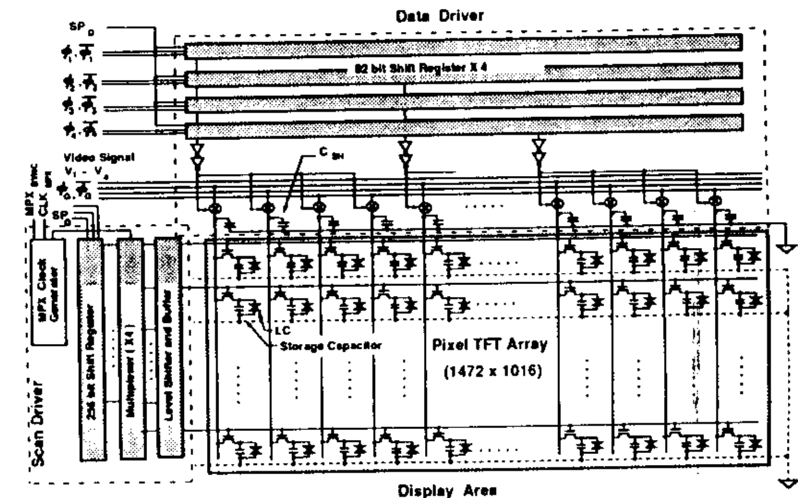


Figure 27 : Block diagram of poly-Si AMLCD for HDTV projector with integrated drivers. Clock frequency for data drivers is 1.8 MHz.

As stated in § 2.3, for such displays, usually with resolutions exceeding 1000x1000 pixels on sizes smaller than 3.5 inches, the fabrication of the drivers on the same plate is the only practical way to overcome the problem of bonding external chips as it is normally done with larger size a-Si:H displays. The complexity of the circuits is also rapidly growing, and drivers with several logic gates per line have been demonstrated [226]. Data drivers capable of handling HDTV signals have been fabricated using multi-phased clocks architectures [227] as well as full digital drivers with 5 bits accuracy [228]. To improve manufacturing yields, circuits dedicated to test the display before assembly are also included thus allowing laser repair [229,230]. Another technique used is the inclusion

of redundancy in the circuits [231] as shown in figure 28, with the possibility of self-repair or re-wiring by laser.

Figure 28: Schematic diagram for redundant shift registers used in the display of figure 27

At present, the highest circuit performance and the more complex displays have been realised on quartz by high temperature processes similar to conventional CMOS processes. In the future, the use of low temperature processes (SPC or laser) should lead to the same level of performance, or in the case of laser crystallisation even improve them, on cheaper and larger glass substrates. The fabrication of analog circuits, namely operational amplifiers, has also been demonstrated both on high [232,233] and low [222,234,235] temperature poly-Si. Although they suffer, for the moment, from problems connected to a high sensitivity to bias conditions, they have already performance levels suitable for switched capacitor circuits applications. In figure 29 a compensated CMOS OpAmp is shown, which has been realised with a low temperature process, giving an open loop gain of 45 dB and a bandwith of 2kHz with a 30V supply voltage [235]. This device has been succesfully applied to the fabrication of a neural network integrating both a-Si:H and poly-Si devices. Circuits like the one of figure 29 will allow the integration, on the same substrate and with the same process, of sensors, displays and signal processing functions, thus greatly reducing the costs and increasing the reliability of personal portable products such as, for example, small electronic notepads with character recognition or pocket faxes without scanning optics, etc..

Figure 29 : Schematic diagram of a compensated poly-Si operational amplifier.

4. Conclusions

We have presented in this chapter the major materials and technologies used in large area electronics. We have not mentioned CdSe, in spite of its good transport properties, because its industrial use is very limited, due to several drawbacks [236]. Clearly, as silicon can be used, it will be used. Any contender must present some really huge advantages in terms of performances or manufacturability in order to be seriously taken into consideration.

We have shown that the a-Si:H technology was today very mature, and as far as pixel switches of AMLCDs are concerned, few problems remain, since the instability of the TFTs do not jeopardise the life time of displays because of the low pixel duty cycle.

Analysts forecast that the LCD market will be comparable to the crystalline semiconductor market by the end of the century. At that time, two dimensional image sensors which are currently being developed will also be on the market, thus increasing the market share of large area electronics.

Although it may still be too early to discern clearly the direction low temperature polysilicon technology will take in the coming years, it is obvious that the AMLCD field will benefit from driver integration. Low temperature poly-Si technology, either SPC or laser crystallisation will probably displace the a-Si:H technology by the end of the century.

In non-display areas, image sensors will probably use poly-Si for on-board sampling and processing operations, although the low frequency noise figures of poly-Si TFTs might not be compatible with the severe requirements of x-ray imaging panels.

Finally, we believe that polysilicon, which is already used in accelerometers for air-bag controllers [237], will increasingly find applications in the area of smart sensors for local signal amplification and / or processing.

Acknowledgements

The authors would like to thank B.Mourey, F. Maurice, N. Szydlo and T. Kretz from Thomson LCD in Moirans for helpful conversations and a-Si:H TFT measurements. Thanks are also due to O. Huet and F. Petinot at Thomson LCR who have contributed to the practical realisation of this book chapter. Finally, we would like to acknowledge fruitful discussions with E. Fogarassy from CNRS in Strasbourg, M. Stehle and B. Godard from Sopra in Bois Colombes, and M. Arques from Thomson TE in Moirans.

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