Exercise 2 Addendum

After completed exercise two

A) Explore the dec0corel.vbe file (BOP output file)

B) Explore the file dec0core.vst file:
1) How many models are used?
2) How many instances of these models are used?
3) How many internal signals interconnect the cells?
4) Draw a schematic representation of the dec2to4.vst file

C) Explore the chip.vst file
1) How many models are used?
2) How many instances of these models are used?
3) How many internal signals interconnect the cells?
4) Draw a schematic representation of the dec2to4.vst file.

D) Explore the layout
1) Which area occupies the core of the chip
2) Which area occupies the chip
3) How many metal layers do you identify?
4) How do the metal layers contact each other?
5) How do a metal layer make contact with diffusion areas?
6) How do a metal layer make contact with a transistor gate?
7) Are all gates of the same length and/or width? Why?.

E) Write a true table for a 3 to 8 bits decoder and write the logic equations to describe it.

F) Write a true table for a 4 to 2 bit encoder and write a set of logic equations to describe it. What about non legal input?

G) Write a true table for an 8 to 3 bit encoder and write the logic equations to describe it.