ICTP Microprocessor Laboratory
African Regional Course on Advanced VLSI Design Techniques
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(Low Voltage) Analog Design

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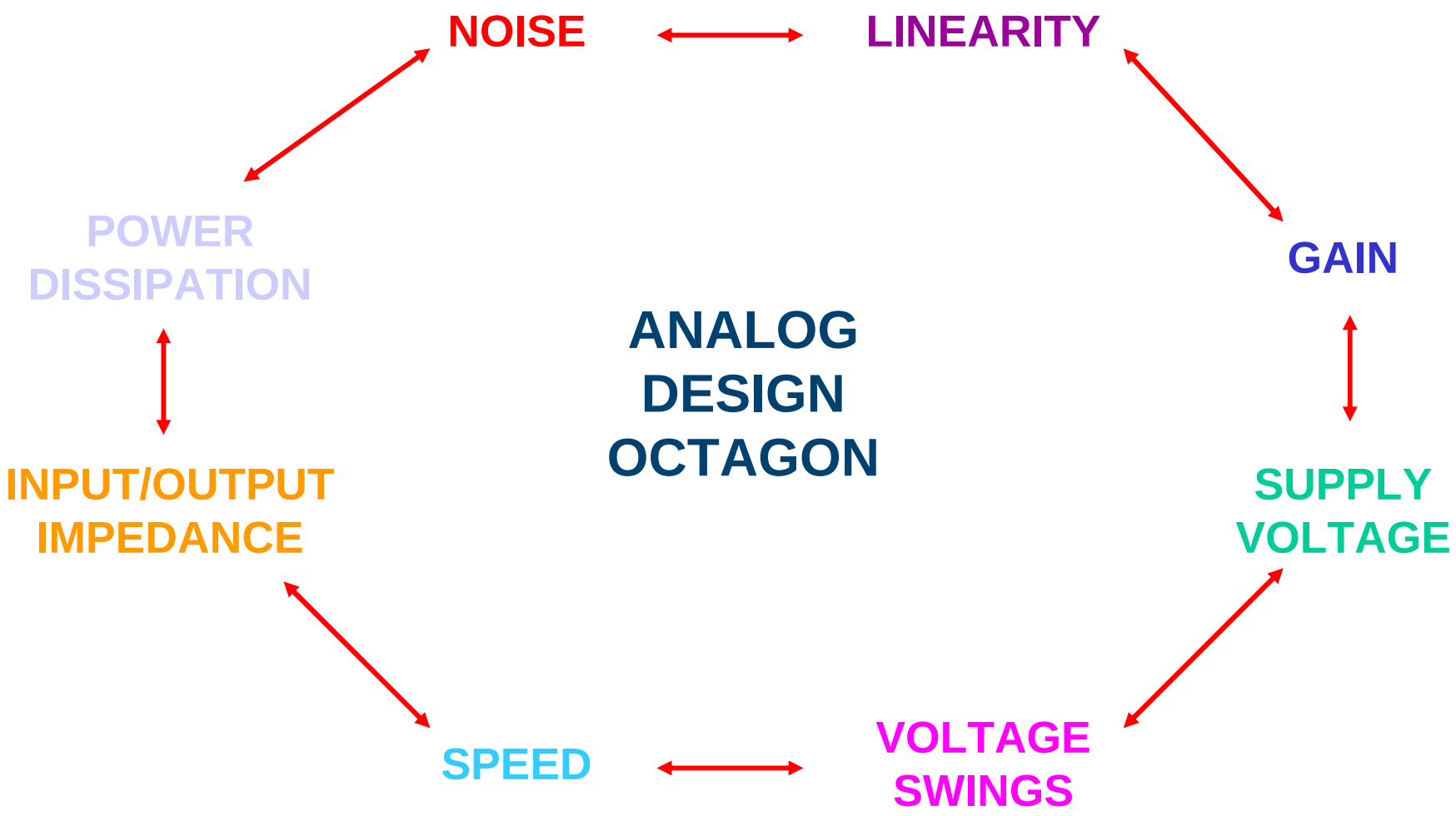
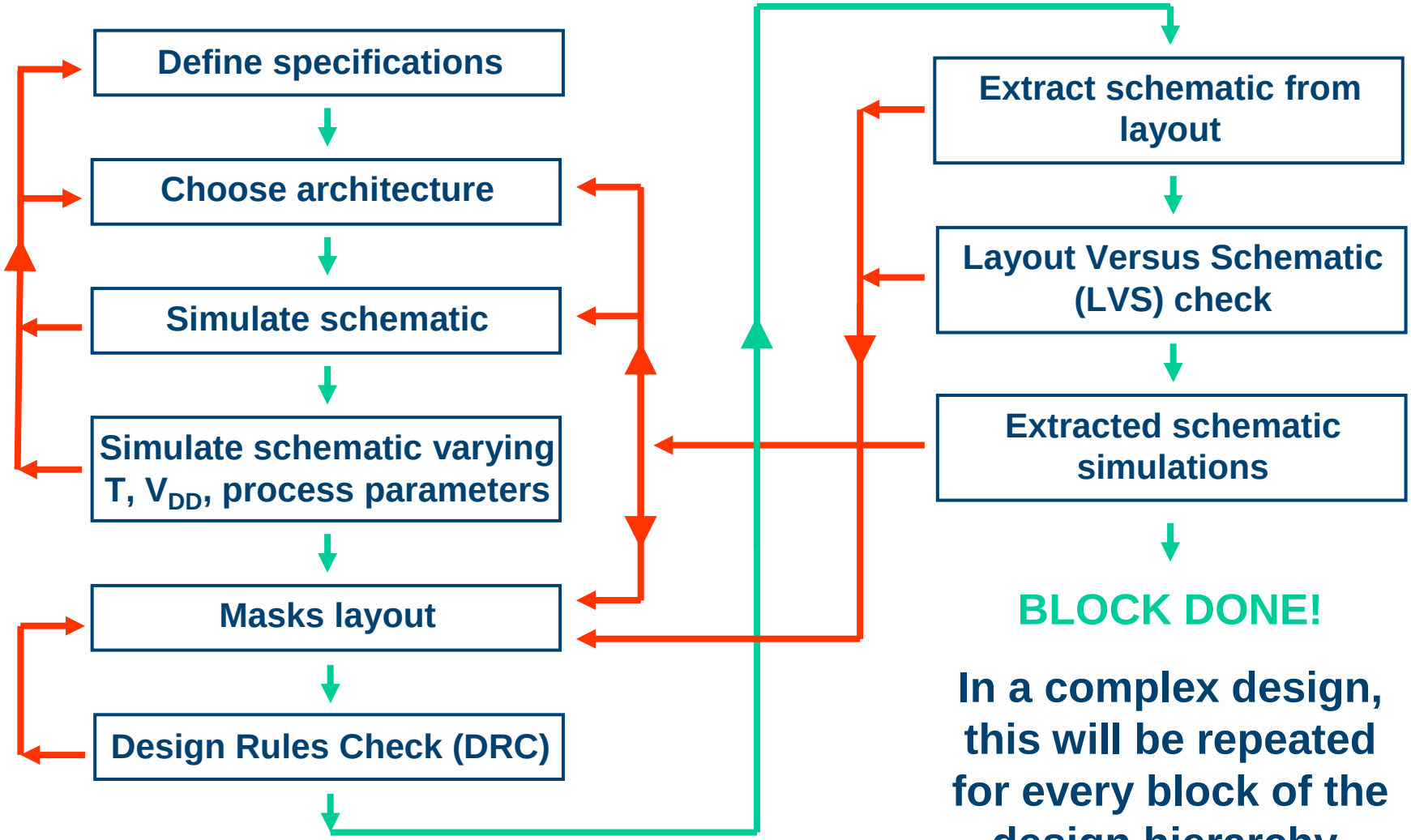
Analog design trade-offs



Behzad Razavi, "CMOS Technology Characterization for Analog and RF Design", *IEEE JSSC*, vol. 34, no. 3, March 1999, p. 268.

Analog design methodology



In a complex design, this will be repeated for every block of the design hierarchy.

Outline

- Single-stage amplifiers
- The differential pair
- The current mirror
- Differential pair + active current mirror
- Frequency analysis of an amplifier
- Operational amplifier (op amp) design

B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill International Edition, 2001.
P.R. Gray, P.J. Hurst, S.H. Lewis, R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, J. Wiley & Sons, 4th edition, 2001.
R. Gregorian, *Introduction to CMOS Op-Amps and Comparators*, J. Wiley & Sons, 1999.
R.L. Geiger, P.E. Allen and N.R. Strader, *VLSI Design Techniques for Analog and Digital Circuits*, McGraw-Hill International Edition, 1990.
D.A. Johns and K. Martin, *Analog Integrated Circuit Design*, J. Wiley & Sons, 1997.

Outline

- Single-stage amplifiers
  - Common-source Stage
  - Common-drain Stage (Source Follower)
  - Common-gate Stage
  - Cascode Stage
  - Folded cascode Stage
- The differential pair
- The current mirror
- Differential pair + active current mirror
- Frequency analysis of an amplifier
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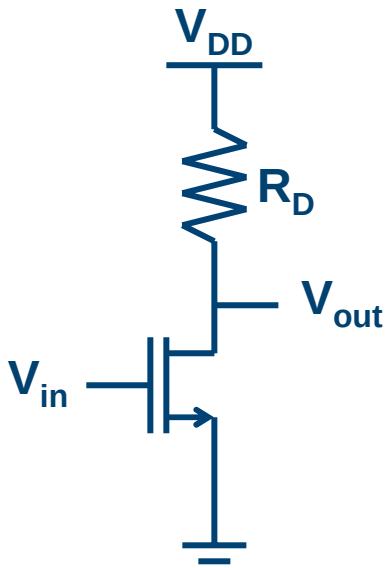
Common-Source Stage (CSS)



DC characteristic

$$V_{out} = V_{DD} - R_D \frac{\beta}{2n}(V_{in} - V_T)^2$$

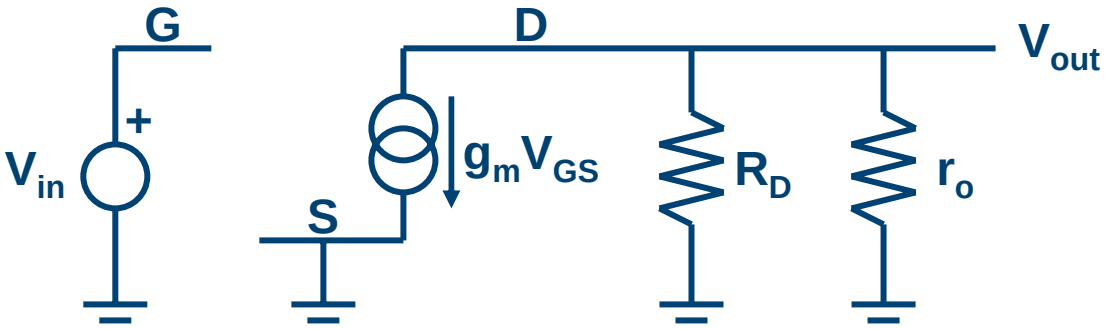
Small signal gain

$$G = \frac{\partial V_{out}}{\partial V_{in}} = -R_D \frac{\beta}{n}(V_{in} - V_T) = -g_m R_D$$

Small signal gain (with channel length modulation)

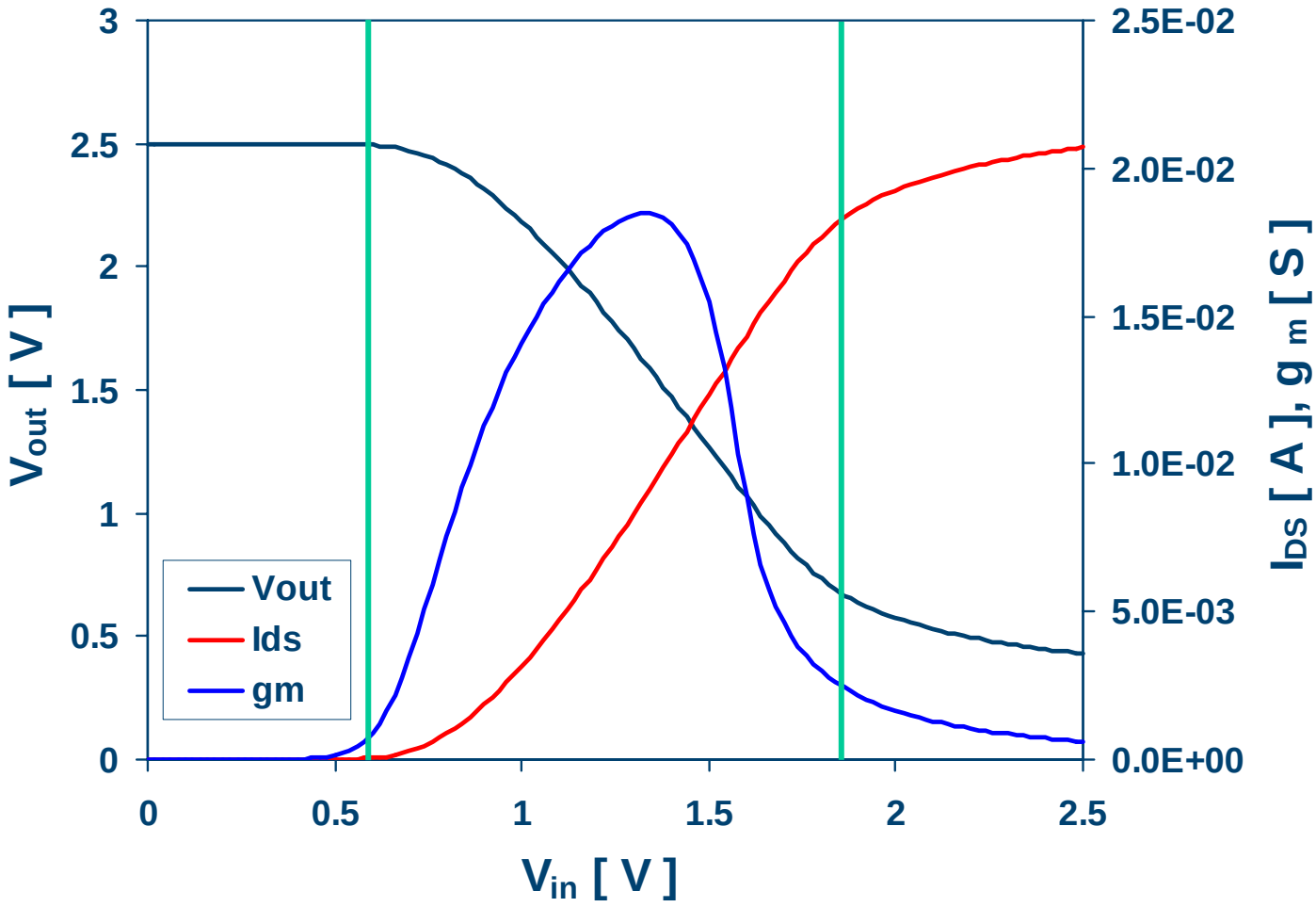
$$G = -g_m (r_0 \,//\, R_D) = -g_m \frac{r_0 R_D}{r_0 + R_D}$$

Small signal model in saturation



The above results could also have been obtained directly from the small signal model

CSS Simulation - DC



W = 100 μm

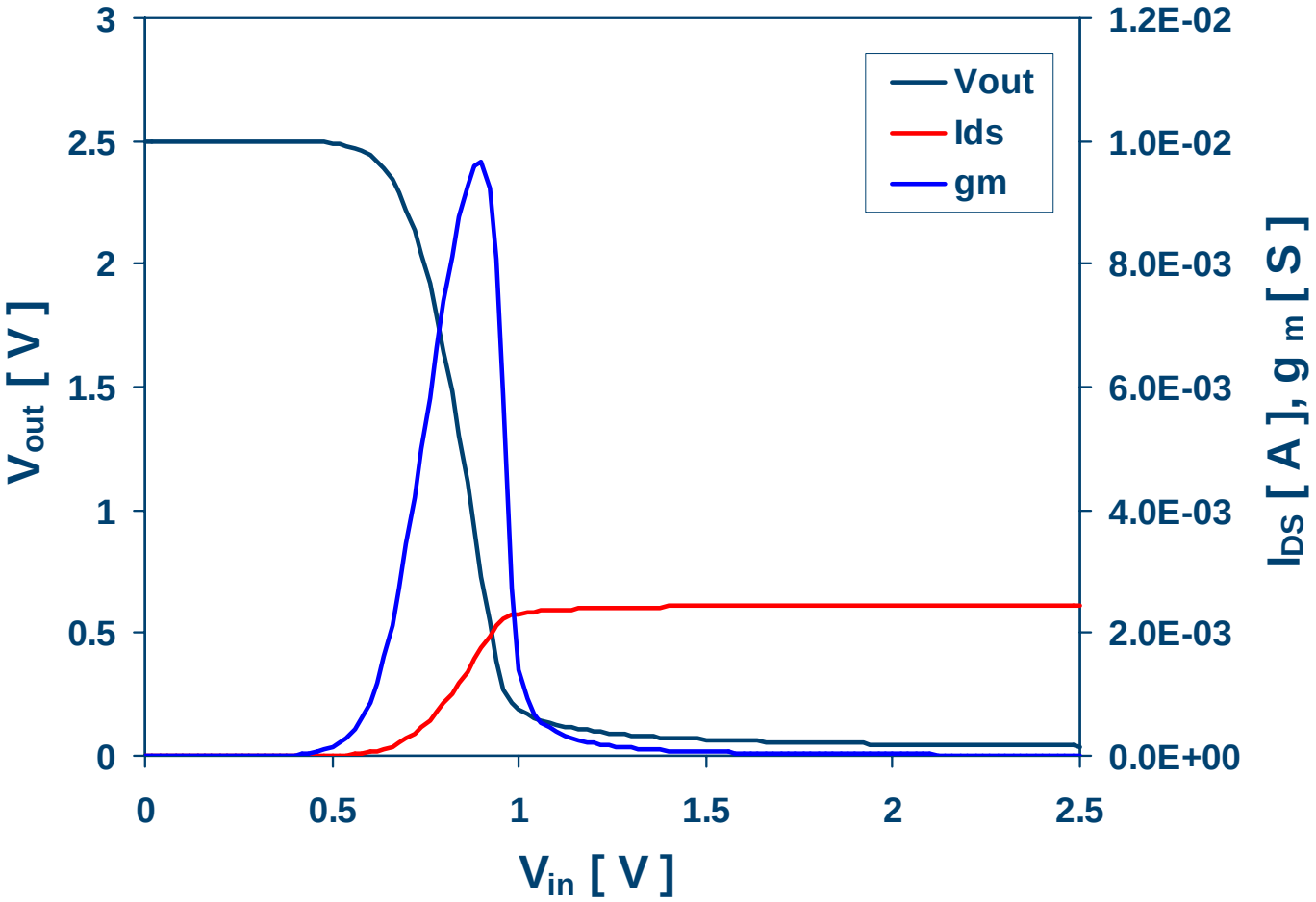
L = 0.5 μm

R = 100 Ω

The maximum small signal gain is only –1.8!!!

CSS Simulation - DC

Increasing the value of the load resistor to 1 kΩ we have



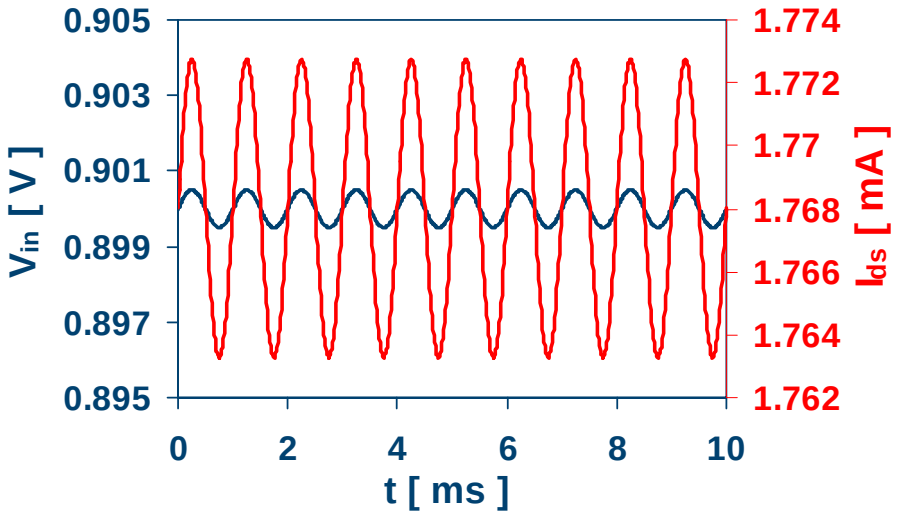
W = 100 μm

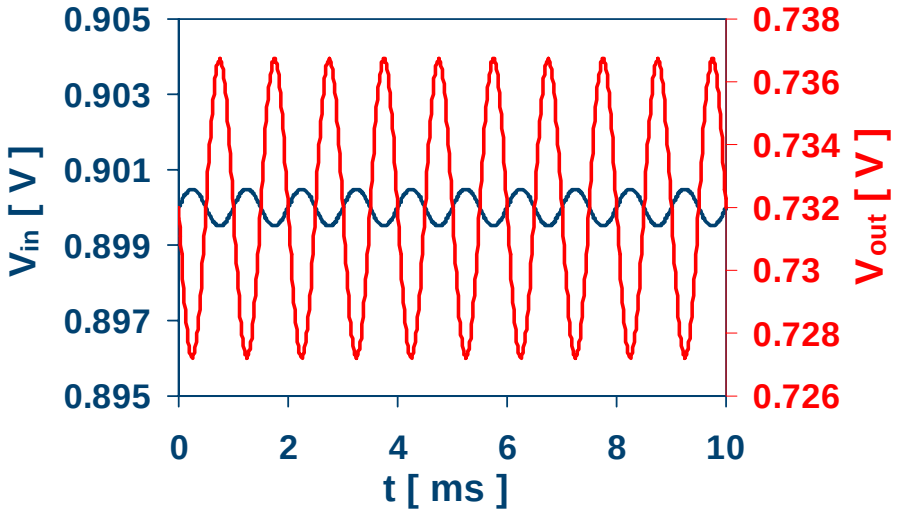
L = 0.5 μm

R = 1000 Ω

The maximum small signal gain is now –9.6.

CSS Simulation – Small Signal





R = 1000 Ω

g_m = 9.6 mS

We inject at the input a sinusoid with frequency 1 kHz, peak to peak amplitude 1 mV AND dc offset = 0.9 V.

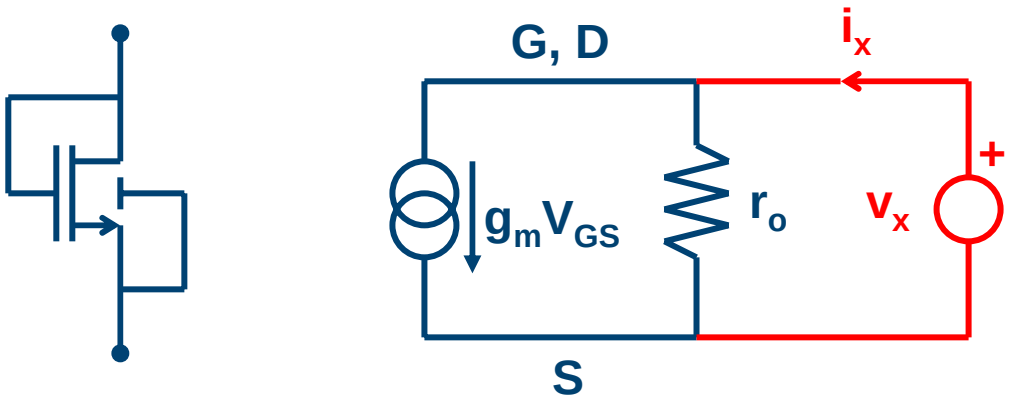
The DC offset is important to be in the right bias point.

The input voltage is converted in a current by the transistor and then in a voltage again by the resistor.

Diode-connected transistor

A MOS transistor behaves as a small signal resistor when gate and drain are shorted. A transistor in this configuration is referred to as "diode-connected" transistor. The device is always in saturation.

To calculate the impedance of this device we use the small-signal equivalent circuit and a test voltage generator (in red). The ratio between the voltage v_x applied and the current i_x gives the impedance.



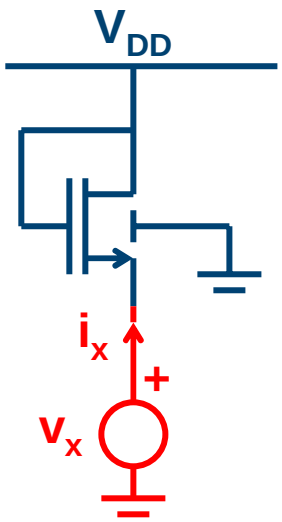
$$i_x = g_m v_x + \frac{v_x}{r_0}$$

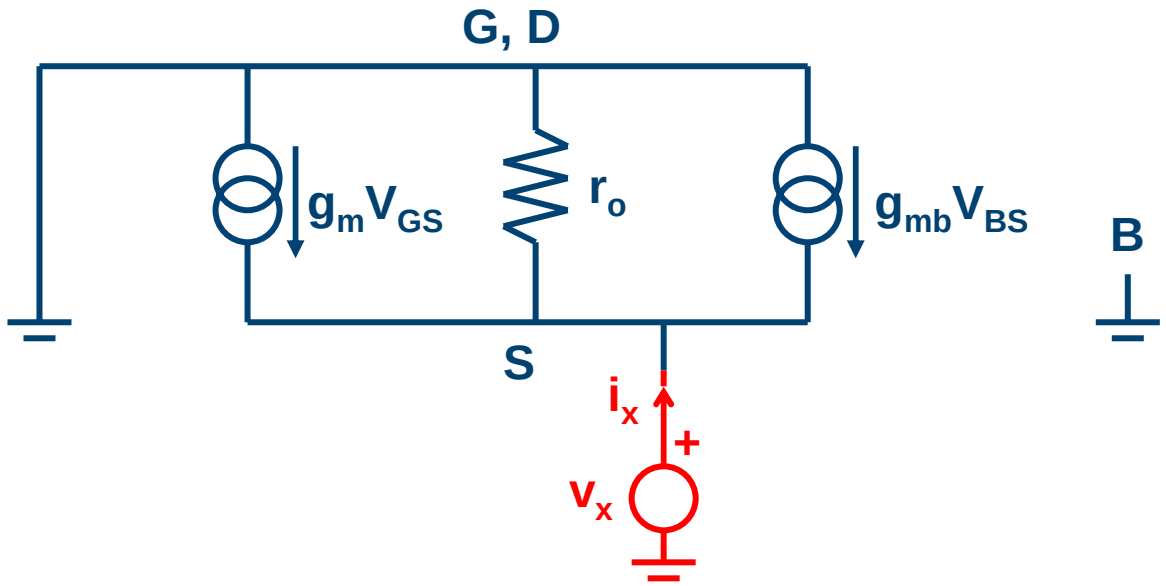
$$R = \frac{v_x}{i_x} = \frac{1}{g_m + \frac{1}{r_0}} \approx \frac{1}{g_m}$$

The calculation show that the impedance is given by the parallel of two resistors, $1/g_m$ and r_0.

Diode-connected transistor

Impedance seen looking into the source.





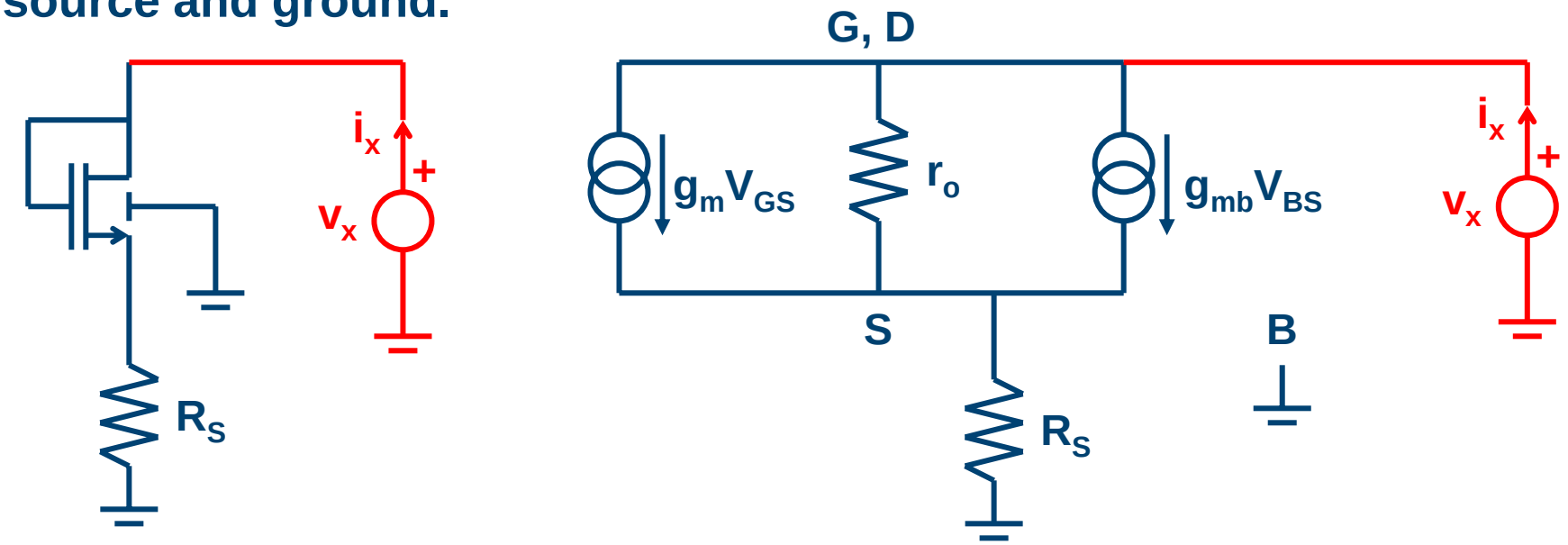
$$i_x = g_m v_x + \frac{v_x}{r_0} + g_{mb} v_x$$

$$R = \frac{v_x}{i_x} = \frac{1}{g_m + g_{mb} + \frac{1}{r_0}} \approx \frac{1}{g_m + g_{mb}}$$

In this case we have three resistances in parallel: $1/g_m$, $1/g_{mb}$ and r_0.

Diode-connected transistor

Impedance seen looking into the drain with a resistor R_S between the source and ground.

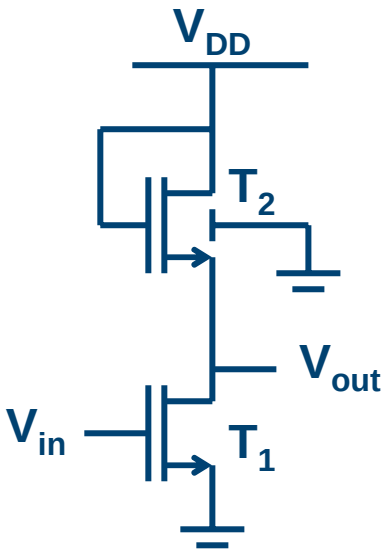


$$i_x = g_m(v_x - i_x R_S) + \frac{v_x - i_x R_S}{r_0} - g_{mb} i_x R_S$$

$$R = \frac{v_x}{i_x} = \frac{1 + \left(g_m + g_{mb} + \frac{1}{r_0}\right) \cdot R_S}{g_m + \frac{1}{r_0}} \approx \frac{1}{g_m} + \frac{g_m + g_{mb}}{g_m} \cdot R_S$$

Without bulk effect (g_{mb}) and the channel length modulation (r_0) we would see the series of $1/g_m$ and R_S. If $R_S = 0$ we find again $1/g_m$.

CSS with diode-connected load



Small signal gain $G = -g_{m1} \cdot R_{out} = -g_{m1} \cdot (R_{D1} // R_{S2})$

$$G = -g_{m1} \cdot \frac{1}{g_{m2} + g_{mb2} + \frac{1}{r_{02}} + \frac{1}{r_{01}}} \approx -\frac{g_{m1}}{g_{m2}} \cdot \frac{g_{m2}}{g_{m2} + g_{mb2}} = -\frac{1}{n_2} \cdot \frac{g_{m1}}{g_{m2}}$$

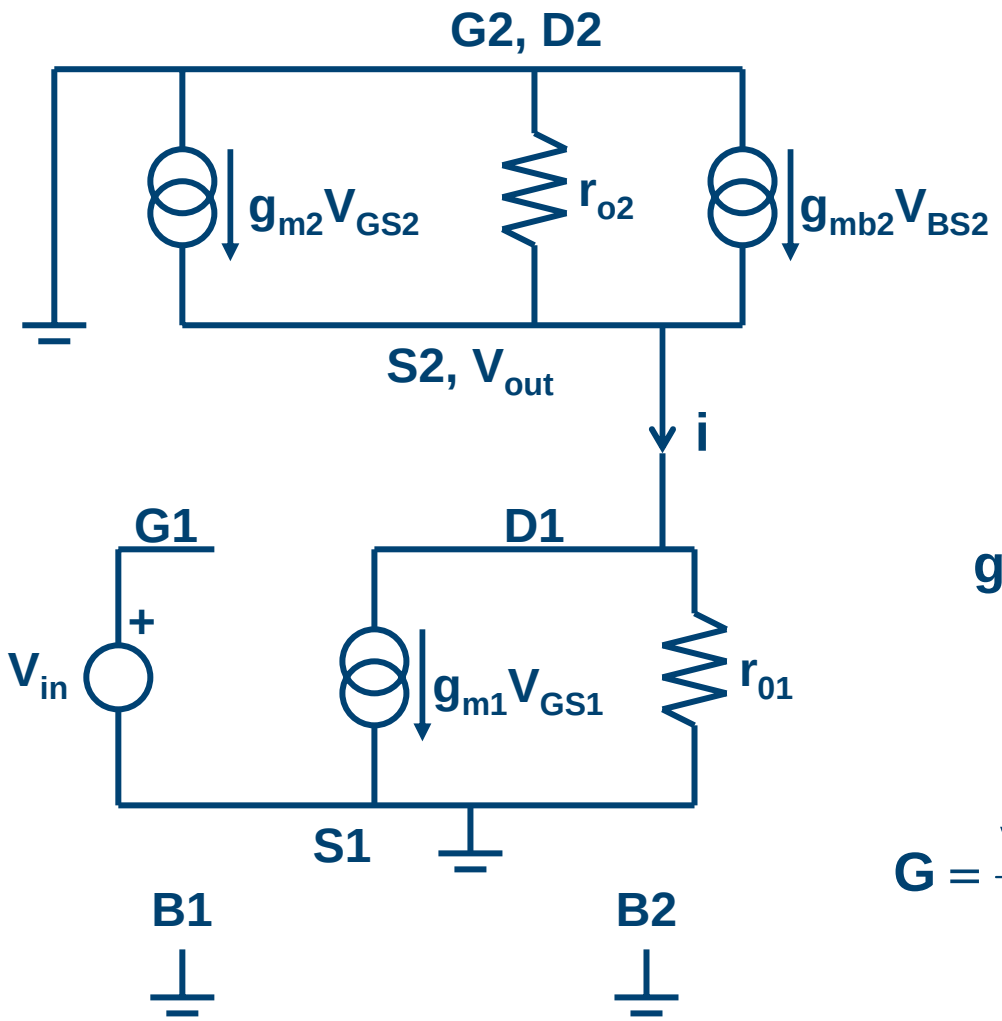
For T_1 and T_2 in strong inversion $G = -\frac{1}{n_2} \cdot \sqrt{\frac{(W/L)_1}{(W/L)_2}}$

The equations above can be obtained in three different ways:

- **Using the results found for single transistors (as we have done)**
- **Starting from the DC equations and doing some mathematics (boring…)**
- **Using the small signal equivalent circuit (see next slide)**

In an N-well CMOS process, the bulk contacts of all the NMOS are connected together to ground (substrate). On the other hand, each bulk contact of the PMOS (each well) can be connected to a desired signal.

Small signal circuit



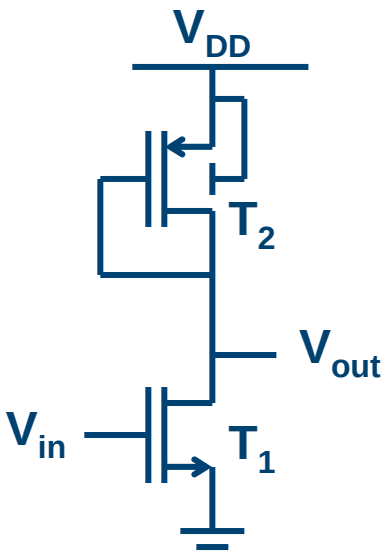
$$\begin{cases} i = g_{m1}v_{in} + \dfrac{v_{out}}{r_{01}} \\ i = -g_{m2}v_{out} - \dfrac{v_{out}}{r_{02}} - g_{mb2}v_{out} \end{cases}$$

$$g_{m1}v_{in} = -v_{out}\left(g_{m2} + g_{mb2} + \frac{1}{r_{01}} + \frac{1}{r_{02}}\right)$$

$$G = \frac{v_{out}}{v_{in}} = -g_{m1} \cdot \frac{1}{g_{m2} + g_{mb2} + \dfrac{1}{r_{02}} + \dfrac{1}{r_{01}}}$$

CSS with diode-connected load

Substituting the NMOS load with a PMOS load, we get rid of the bulk effect.



Small signal gain

$$G = -g_{m1} \cdot \frac{1}{g_{m2} + \frac{1}{r_{02}} + \frac{1}{r_{01}}} \approx -\frac{g_{m1}}{g_{m2}}$$

In strong inversion, we have

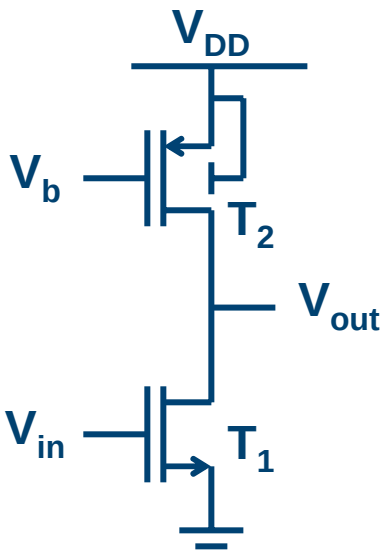
$$G = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}}$$

Drawbacks of this configuration:

- **It is difficult to have high gain**
- **$V_{out\_max} = V_{DD} - |V_{GS2}|$.**
- **To have gain, $(W/L)_2$ is made smaller than $(W/L)_1$. This will limit the maximum output voltage, since $|V_{GS2}|$ will be quite higher than V_{T2}.**

CSS with Current Source load

To increase the gain, we can use the output resistance of a transistor. T2 provides the DC current bias to T1, and has a high output impedance. The bias current is determined by V_b.



Small signal gain

$$G = -g_{m1}\left(r_{01} \,//\, r_{02}\right) = -g_{m1} \cdot \frac{1}{\frac{1}{r_{02}} + \frac{1}{r_{01}}} = -g_{m1} \cdot \frac{r_{01} \cdot r_{02}}{r_{01} + r_{02}}$$

This solution gives a much higher gain than the other solutions and has a better DC output swing, since $V_{out\_max} = V_{DD} - |V_{DS2\_sat}|$ and $V_{out\_min} = V_{DS1\_sat}$.

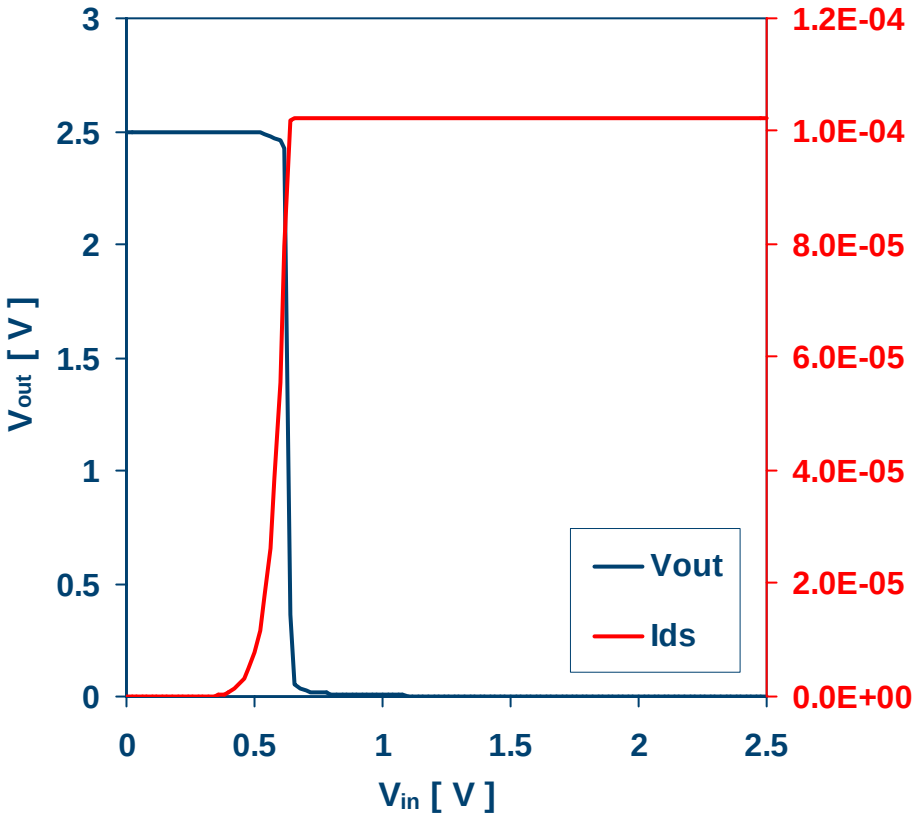
The output of the circuit shown is in an undefined state (high-impedance node). This circuit needs therefore an "external system" to fix its output DC bias point (we need a feedback network!).

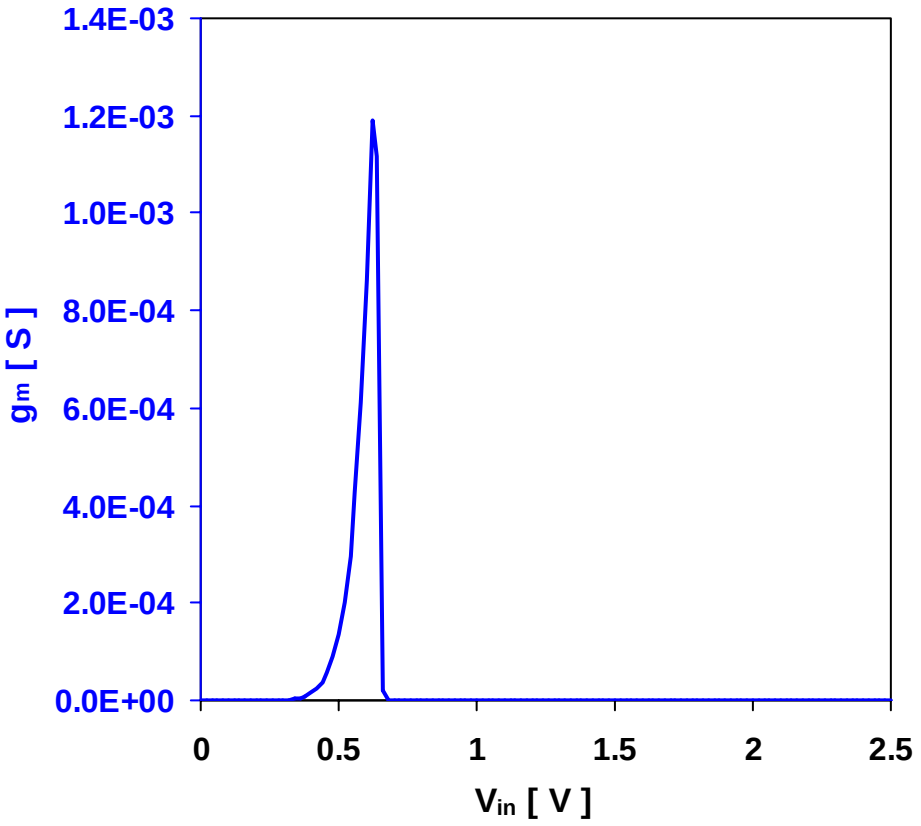
CSS-CSL Simulation - DC

CSS-CSL = Common Source Stage with Current Source Load

Input Transistor $W_1 = 100\ \mu m$, $L_1 = 0.5\ \mu m$

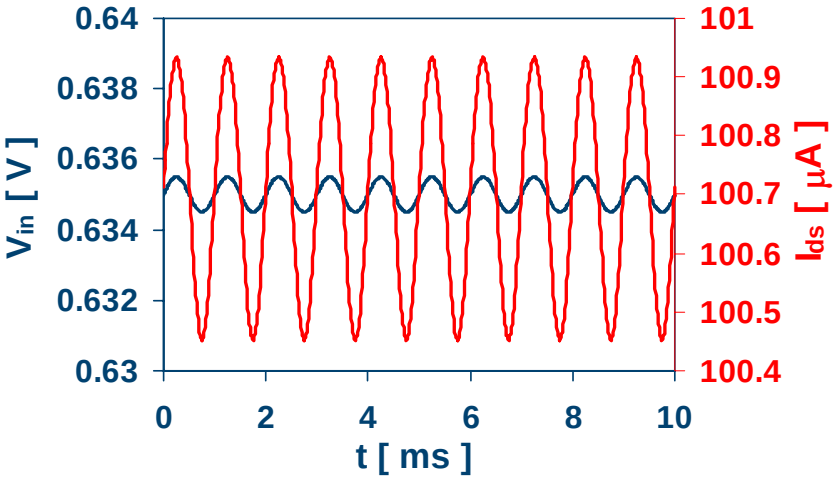
Load Transistor $W_2 = 800\ \mu m$, $L_2 = 4\ \mu m$

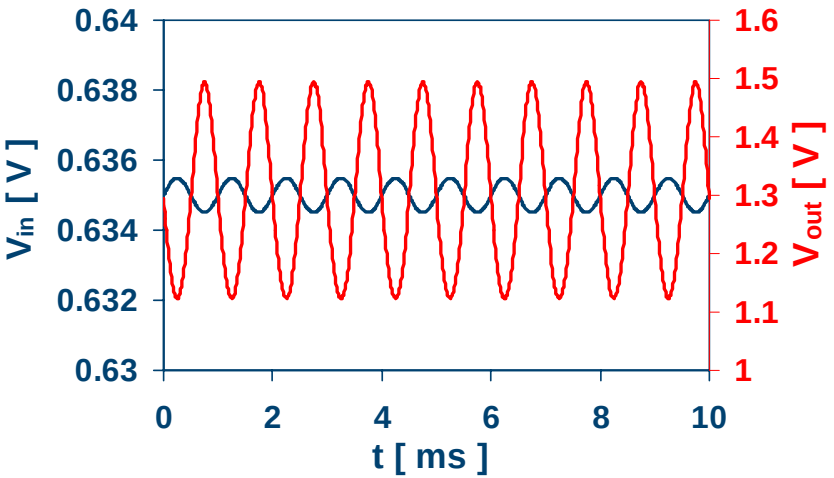




CSS-CSL Simulation – Small Sign.

Small signal simulations





We inject at the input a sinusoid with frequency 1 kHz, peak to peak amplitude 1 mV and DC offset = 0.635 V.

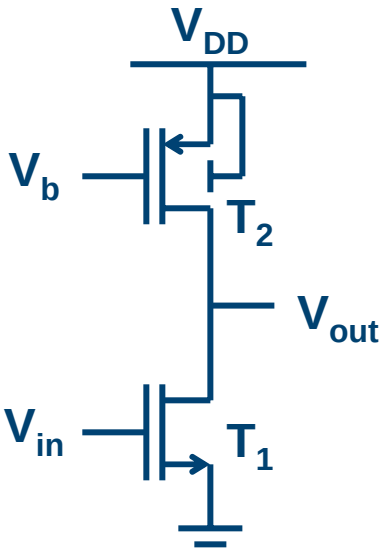
The DC offset is important to be in the right bias point (especially for the output!)

With a current of just 100 µA and the same input transistor dimensions as in the case of the CSS with load resistor, we have a gain of –373.

N.B. The output current is smaller than what it should be. The bias point is so critical that the simulator has some problems…

CSS with Triode load

This circuit is the same as the CSS with Current Source load, but the gate bias of transistor T2 is low enough to make sure that T2 works in the linear region and therefore it behaves as a resistor.



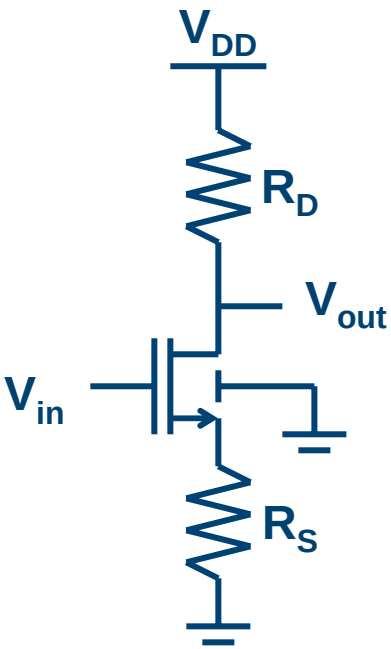
Small signal gain

$$G = -g_{m1} \cdot \frac{1}{\mu_P C_{ox} \frac{W_2}{L_2} (V_{DD} - V_b - V_{TP})}$$

To have T2 in the linear region, we must have $V_b < V_{out} - V_{TP}$ (where V_{TP} is a positive number). If we can not take $V_b < 0$ V, we can take it = 0 V. In this case we must have $V_{out} > V_{TP}$.

The principal drawback of this circuit is that the small-signal gain depends on many parameters.

CSS with Source Degeneration



In some applications, the square-law dependence of the drain current upon the gate overdrive voltage introduces excessive non linearity. R_S "smoothes" this effect since it takes a portion of the gate overdrive voltage. At the limit, for $R_S >> 1/g_m$, the small signal gain does not depend on g_m (and therefore on I_{DS}) anymore.

It is interesting to note that the approximated small signal gain (which can be easily calculated with the small signal equivalent circuit) can also be calculated as if R_S and $1/g_m$ were two resistors in series.

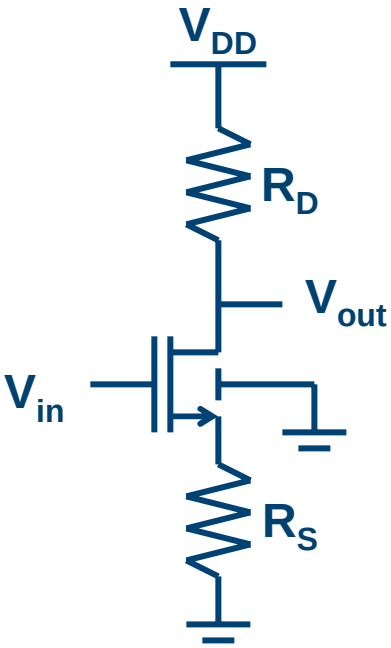
Small signal gain (approximation)

$$G = -\frac{g_m}{1+g_m R_S}\cdot R_D = -\frac{R_D}{\frac{1}{g_m}+R_S}$$

CSS with Source Degeneration

The approximated small signal voltage gain can also be seen as the product of the small signal equivalent transconductance of the degenerated CS Stage multiplied by the total resistance seen at the output (R_D).

To calculate the exact small signal voltage gain we need the exact small signal equivalent transconductance and the output resistance of the degenerated CS Stage. Both these quantities can be calculated with the equivalent small signal circuits.



Small signal gain (approximation)

$$G = -\frac{g_m}{1 + g_m R_S} \cdot R_D = -g_{m\_eq} \cdot R_D$$

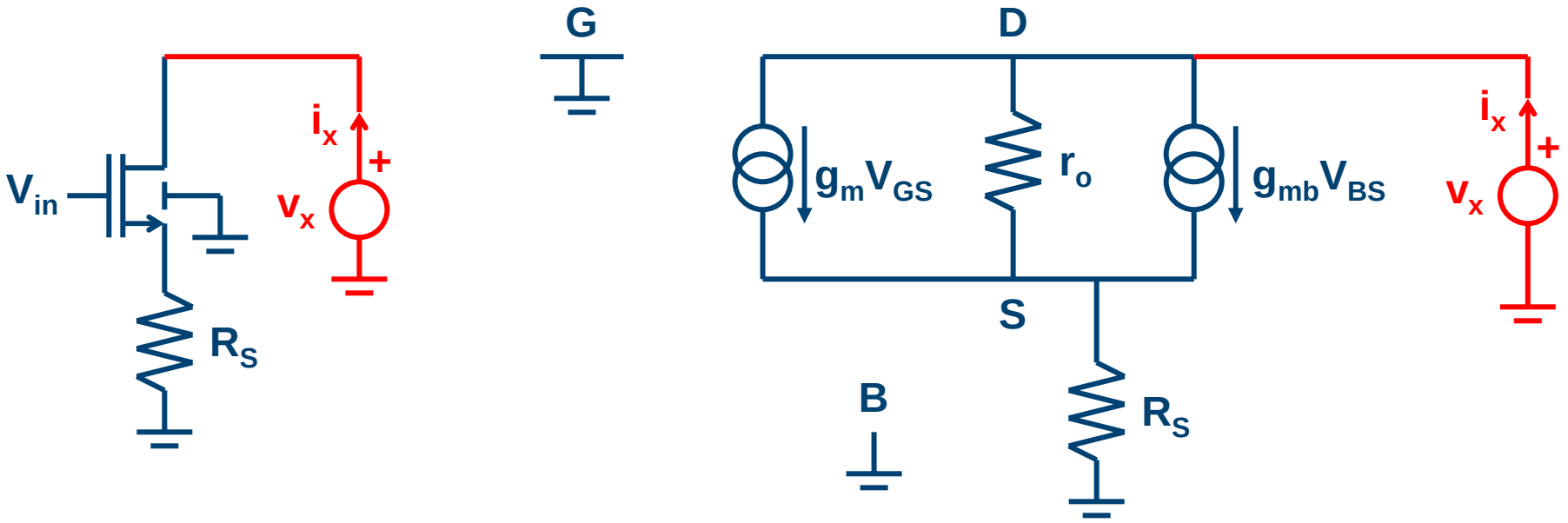
Exact small signal equivalent transconductance (with channel length modulation and bulk effect)

$$g_{m\_eq} = \frac{g_m r_0}{R_S + r_0 + (g_m + g_{mb}) \cdot R_S \cdot r_0}$$

DO IT YOURSELF AS AN EXERCISE!

CSS with Source Degeneration

Calculation of the output resistance of the degenerated CS Stage.

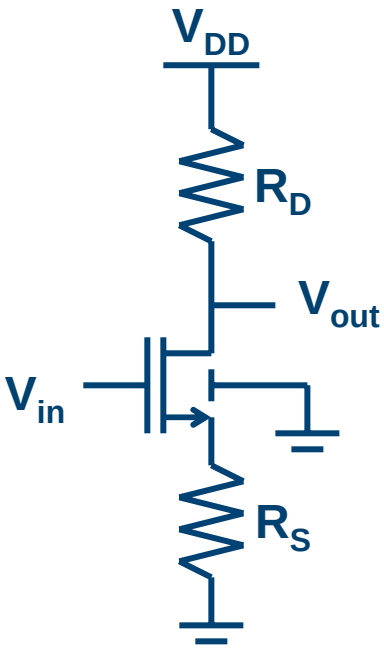


$$i_x = -g_m v_s + \frac{v_x - v_s}{r_0} - g_{mb} v_s \qquad v_s = i_x R_S$$

$$R_{out\_CSS\_deg} = \frac{v_x}{i_x} = r_0 + R_S + (g_m + g_{mb}) \cdot r_0 R_S$$

CSS with Source Degeneration

Exact small signal gain of the degenerated CS Stage.



Approximated small signal gain

$$G_{appr.} = -\frac{g_m}{1+g_m R_S}\cdot R_D = -g_{m\_eq}\cdot R_D$$

Output resistance of the degenerated CS Stage

$$R_{out} = R_{out\_CSS\_Deg} \,//\, R_D$$

$$R_{out\_CSS\_deg} = r_0 + R_S + (g_m + g_{mb})\cdot r_0 R_S$$

Exact small signal gain

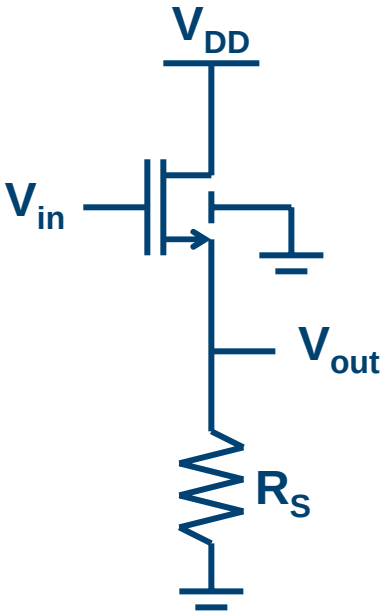
$$G = -g_{m\_eq}\cdot R_{out}$$

$$g_{m\_eq} = \frac{g_m r_0}{R_S + r_0 + (g_m + g_{mb})\cdot R_S \cdot r_0}$$

Exercise: try to obtain the same equation with the complete small signal circuit

Source Follower (SF)

The analysis of the Common Source Stage (CSS) with current source load demonstrated that to have a high voltage gain we have to have a high load impedance. If we want to use a CSS to drive a low impedance load, we have to put a "buffer" between the CSS and the load. The simplest buffer is the Source Follower (also called Common Drain Stage).



How do we obtain the small signal gain? We could use the small signal equivalent circuit or we can be clever and reuse what we have seen up to now!

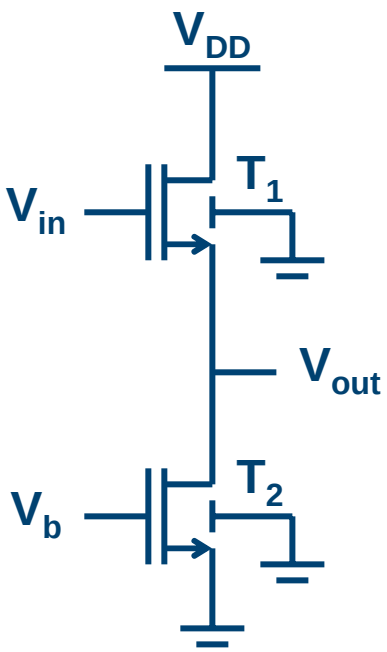
$$G = \frac{V_{out}}{V_{in}} = g_m \cdot \left(R_S \,//\, \frac{1}{g_m + g_{mb} + 1/r_0} \right)$$

$$G = \frac{g_m}{g_m + g_{mb} + \frac{1}{r_0} + \frac{1}{R_S}} = \frac{g_m \cdot R_S}{1 + (g_m + g_{mb}) \cdot R_S}$$

The gain of our buffer is never one! It is, in the best case, 1/n

Source Follower (SF)

The Source Follower with a resistor is highly non linear, since the drain current in T1 is a strong function of the input DC level.
We can therefore replace the resistor with a current source.



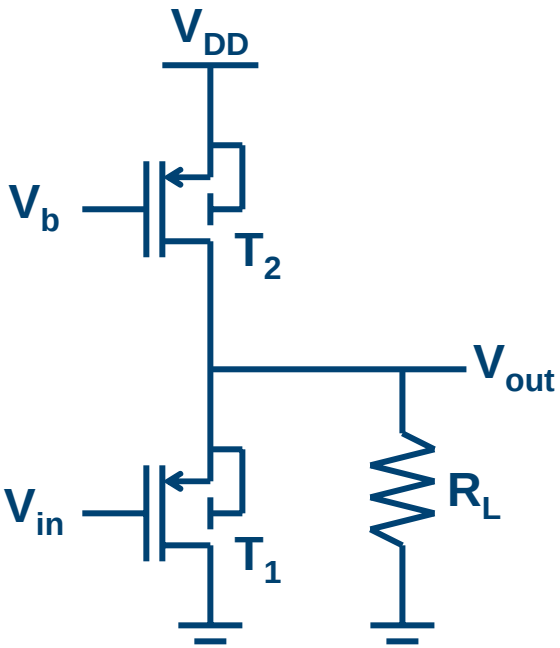
$$G_{SF\_NMOS} = g_{m1} \cdot \left(r_{02} \,//\, \frac{1}{g_{m1} + g_{mb1} + 1/r_{01}} \right) = \frac{g_{m1}}{g_{m1} + g_{mb1} + 1/r_{01} + 1/r_{02}}$$

The gain is in this case close to 1/n (still not 1…). The circuit is still non linear due to the body effect (non linear dependence of V_{T1} upon the source potential). This can be solved using a PMOS Source Follower, in which both the transistors have the body (well) connected to the source. In this case, we have:

$$G_{SF\_PMOS} = g_{m1} \cdot \left(r_{02} \,//\, \frac{1}{g_{m1} + 1/r_{01}} \right) = \frac{g_{m1}}{g_{m1} + 1/r_{01} + 1/r_{02}}$$

The gain can be in this case very close to one!

Source Follower drawbacks



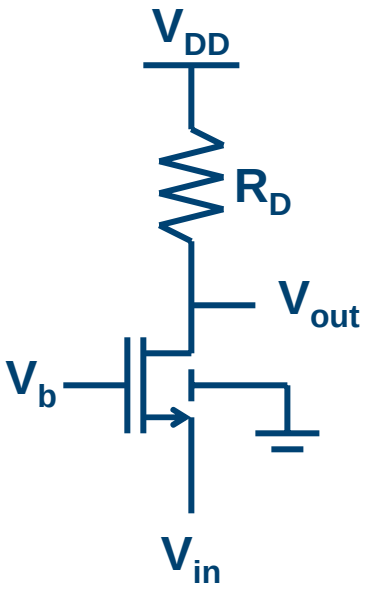
$$G = g_{m1} \cdot \left(R_L \,//\, r_{02} \,//\, \frac{1}{g_{m1} + 1/r_{01}} \right) = \frac{g_{m1}}{g_{m1} + 1/r_{01} + 1/r_{02} + 1/R_L}$$

$$G \approx \frac{g_{m1}}{g_{m1} + 1/R_L} = \frac{R_L}{R_L + 1/g_m}$$

If the source follower has to drive a low impedance, we risk to have a gain which is significantly smaller than one. Another important drawback is that source followers shift the signal by one V_{GS}. This is a drawbacks especially in low voltage circuit, where this causes a limitation in the voltage headroom. On the other hand, if the power supply voltage is high enough, source followers can be used as voltage level shifters.

Common-Gate Stage (CGS)

In Common-Source Stages and Source Followers the input signal is applied to the gate. We can also apply it to the source, obtaining what is called a Common-Gate Stage (CGS)



$$R_{out} = R_{out\_CGS} \,//\, R_D \qquad R_{out\_CGS} = r_0$$

$$R_{in} = \frac{1 + R_D / r_0}{g_m + g_{mb} + r_0} = \frac{R_D + r_0}{1 + (g_m + g_{mb}) \cdot r_0} \quad \rightarrow \quad \text{EXERCISE!}$$

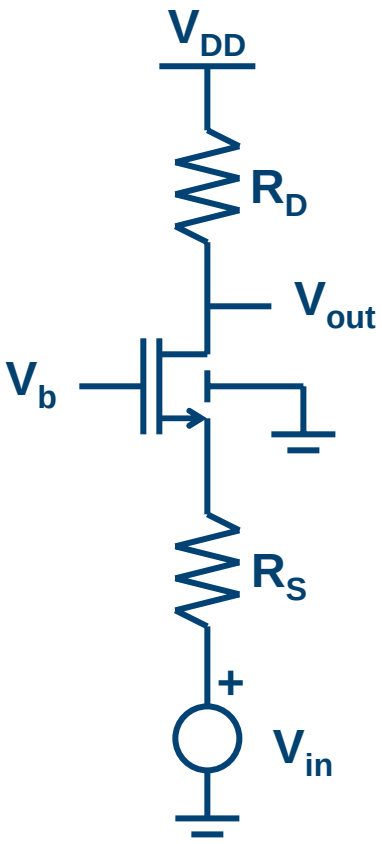
$$G = \frac{R_{out}}{R_{in\_R_D=0}} = (r_0 \,//\, R_D) \cdot (g_m + g_{mb} + 1/r_0)$$

$$G = \frac{R_D}{R_{in}} = R_D \cdot \frac{r_0 \cdot (g_m + g_{mb}) + 1}{R_D + r_0} \approx g_m \cdot n \cdot R_D$$

The input impedance of a CGS is relatively low, but this only if the load impedance in low. The gain is slightly higher to the one of a CSS, since we apply the signal to the source. N.B. We have calculated the small signal gain using 2 different methods (red and blue). The results are identical!

Common-Gate Stage (CGS)

With the results obtained, it is now very easy to study the most "general" case, which includes the impedance R_S of the signal source, the channel modulation effect and the bulk effect. Let's call R_{in} the resistance seen by the ideal voltage source.



$$R_{in} = R_S + \frac{R_D + r_0}{1 + (g_m + g_{mb}) \cdot r_0} \qquad \frac{v_{in}}{R_{in}} \cdot R_D = v_{out}$$

$$G = \frac{v_{out}}{v_{in}} = \frac{R_D}{R_{in}} = R_D \cdot \frac{1 + (g_m + g_{mb}) \cdot r_0}{R_S \cdot [1 + (g_m + g_{mb}) \cdot r_0] + R_D + r_0}$$

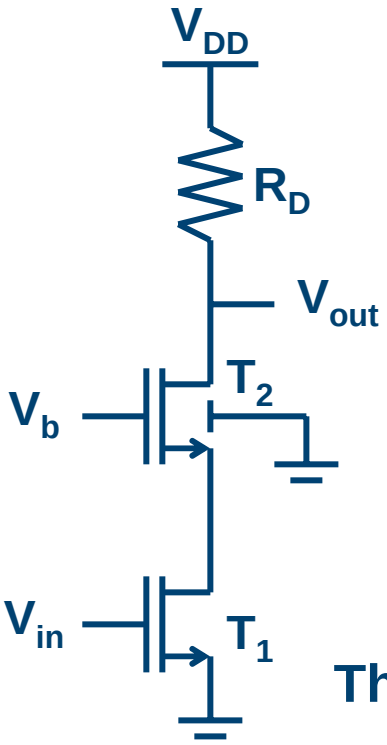
This result is very similar to the one of a Common Source Stage with source degeneration. The gain here is still slightly higher due to the body effect. It is now also easy to calculate the resistance seen into the output.

$$R_{out} = R_D \,//\, R_{out\_CSS\_deg}$$

$$R_{out\_CSS\_deg} = r_0 + R_S + (g_m + g_{mb}) \cdot r_0 R_S$$

Cascode Stage (CascS)

The "cascade" of a Common-Source Stage (V-I converter) and of a Common-Gate Stage is called a "Cascode".

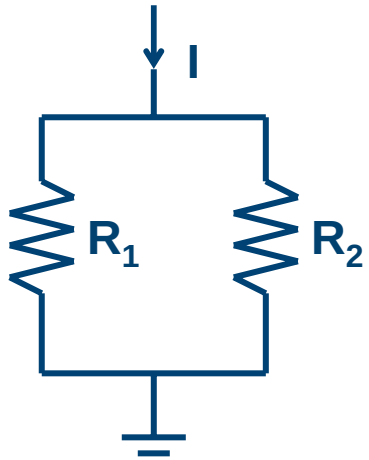


$$v_{out} = -v_{in} \cdot g_{m1} \cdot \frac{r_{01}}{R_D + r_{02}} \cdot R_D$$
$$r_{01} + \frac{}{1 + (g_{m2} + g_{mb2}) \cdot r_{02}}$$

$$G = -g_{m1} \cdot \frac{r_{01}}{R_D + r_{02}} \cdot R_D \approx -g_{m1} R_D$$
$$r_{01} + \frac{}{1 + (g_{m2} + g_{mb2}) \cdot r_{02}}$$

The gain is practically the same as in the case of a Common-Source Stage.

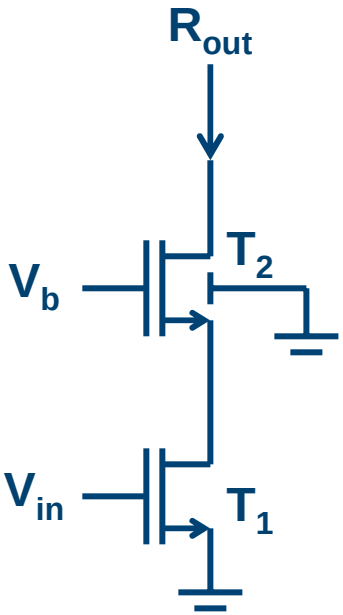
REMINDER



$$I_1 = \frac{R_2}{R_1 + R_2} \cdot I$$

Cascode Stage Output Resistance

One nice property of the cascode stage can be discovered looking at the resistance seen in the drain of T2. This is quickly done if we look at T2 as a Common-Source Stage with a degeneration resistor = r_{01}.



$$R_{out\_CSS\_deg} = r_0 + R_S + (g_m + g_{mb}) \cdot r_0 R_S$$

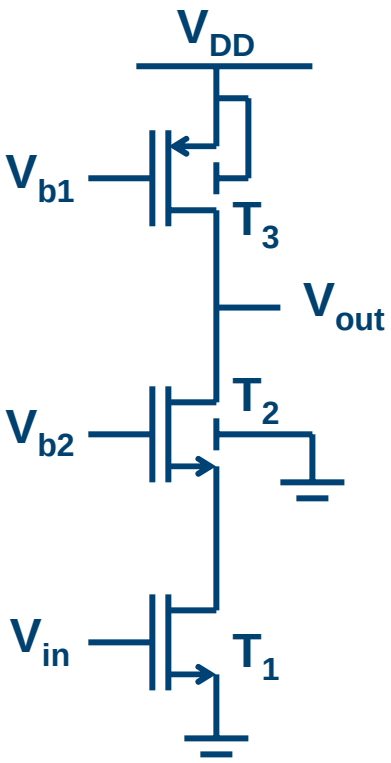
$$R_{out\_CascS} = r_{01} + r_{02} + (g_{m2} + g_{mb2}) \cdot r_{01} r_{02} \approx (g_{m2} + g_{mb2}) \cdot r_{01} r_{02}$$

Compared to a CSS, the output impedance is "boosted" by a factor (g_{m2} + g_{mb2}) r_{02}.

The disadvantage of the cascode configuration is that the minimum output voltage is now the sum of the saturation voltages of T1 and T2. It must therefore be used with care in low voltage circuits.

CascS with current source load

To fully profit of the high output impedance of the cascode stage, it seems natural to load it with a high impedance load, like a current source.



$$R_{out\_CascS} = r_{01} + r_{02} + (g_{m2} + g_{mb2}) \cdot r_{01} r_{02}$$

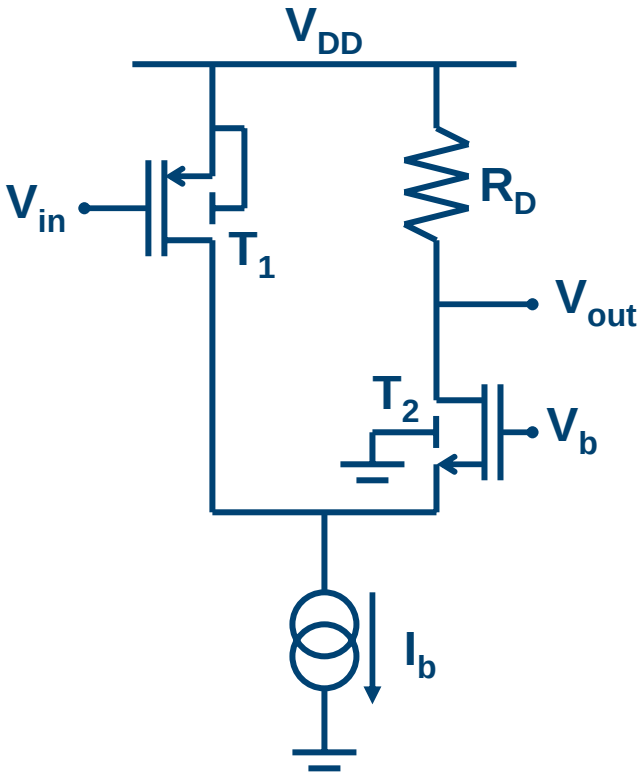
$$R_{out} = R_{out\_CascS} \,//\, r_{03}$$

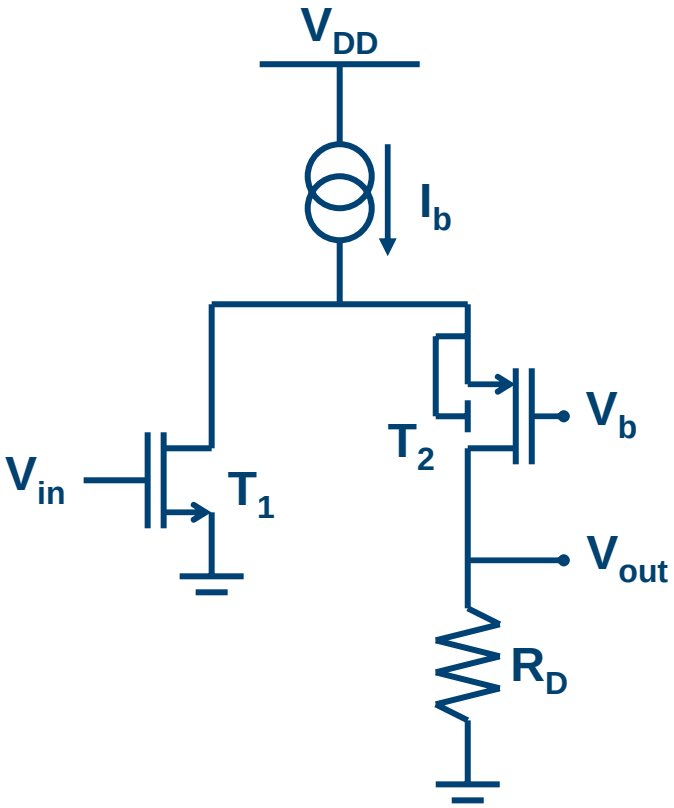
$$G \approx -g_{m1} R_{out}$$

If r_{03} is not high enough, we can use the cascode principle to boost the output impedance of the current source as well.

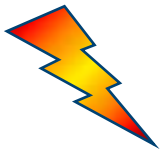
N.B. Remember that the DC output level here is not well defined, and that we will need a feedback loop.

Folded Cascode Stage (FCascS)





This solution is has a lower output impedance than the standard CascS and consumes more current for the same performance.

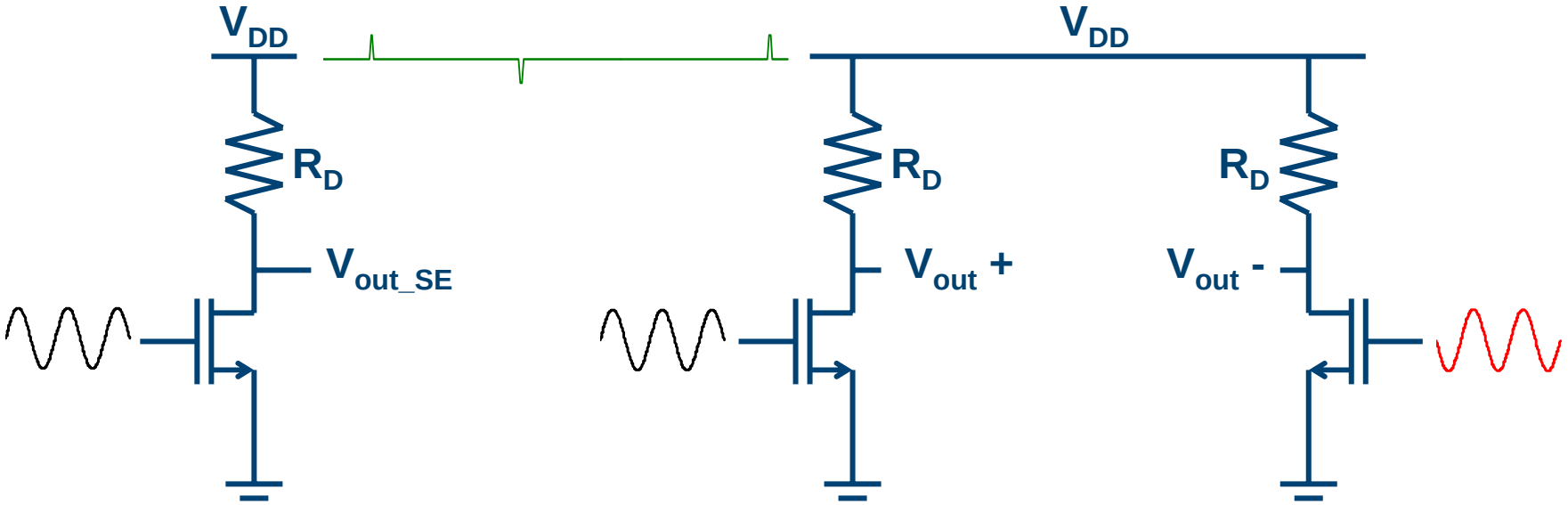


Outline

- Single-stage amplifiers
- The differential pair
  - Differential signal advantages
  - The differential pair
    - Common Mode Analysis
    - Large Signal Analysis
    - Small Signal Analysis
    - Common Mode Rejection Ratio (CMMR)
  - Differential pair with MOS loads
  - Differential Pair Mismatch
- The current mirror
- Differential pair + active current mirror
- Frequency analysis of an amplifier
- Operational amplifier (op amp) design

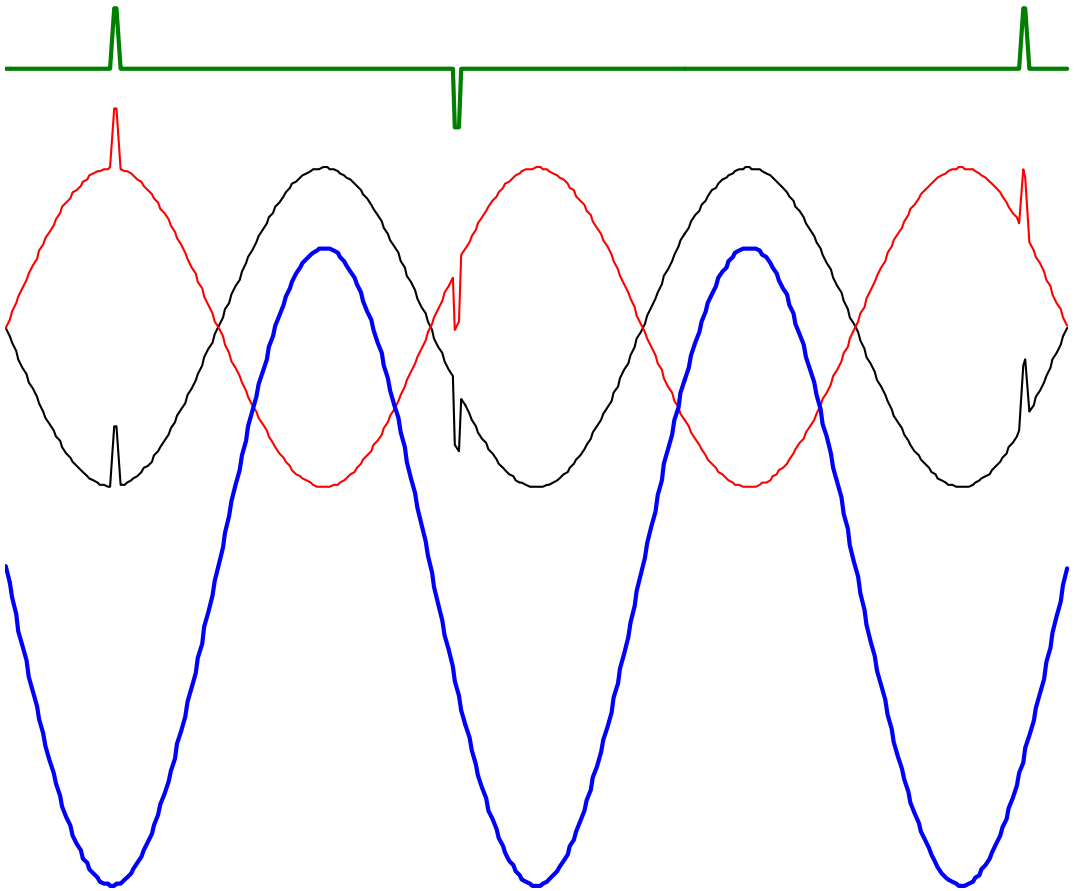
Single-Ended vs Differential

A single-ended signal is defined as a signal measured with respect to a fixed potential (usually, ground).
A differential signal is defined as a signal measured between two nodes which have equal and opposite signal excursions. The "center" level in differential signals is called the Common-Mode (CM) level.
The most important advantage of differential signals over single-ended signals is the much higher immunity to "environmental" noise.
As an example, let's suppose to have a disturbance on the power supply.



Single-Ended vs Differential

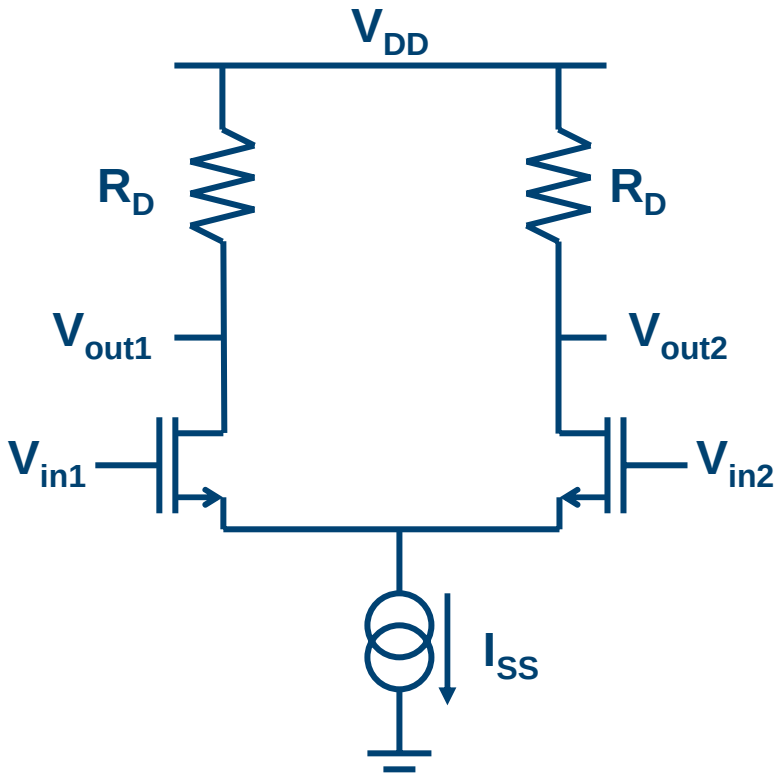
The Common-Mode disturbances disappear in the differential output.

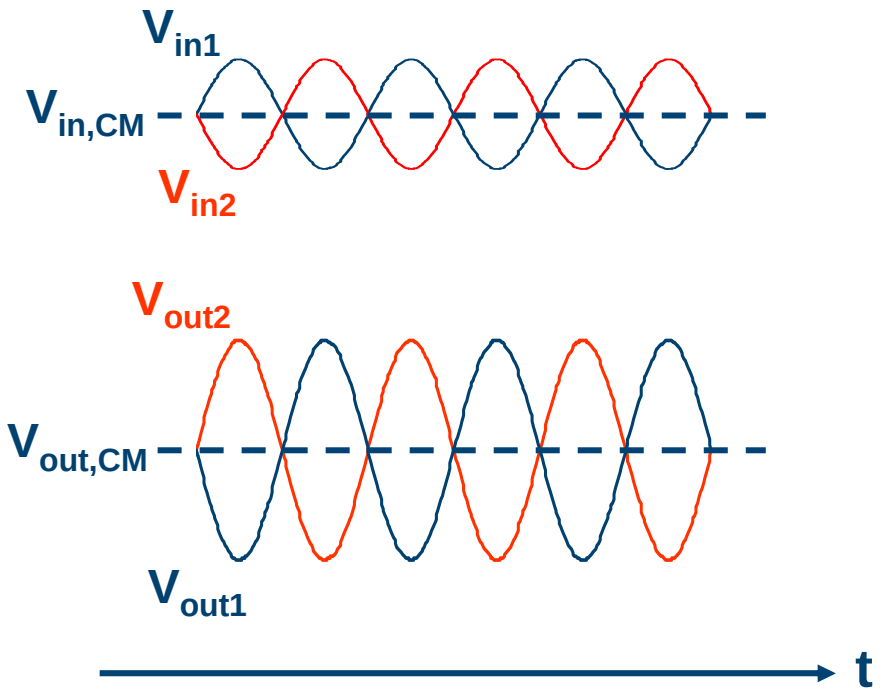


Vdd
Vout_SE = Vout +
Vout -
Vout_diff

$$V_{out\_diff} = V_{out+} - V_{out-}$$

Differential Pair (DP)



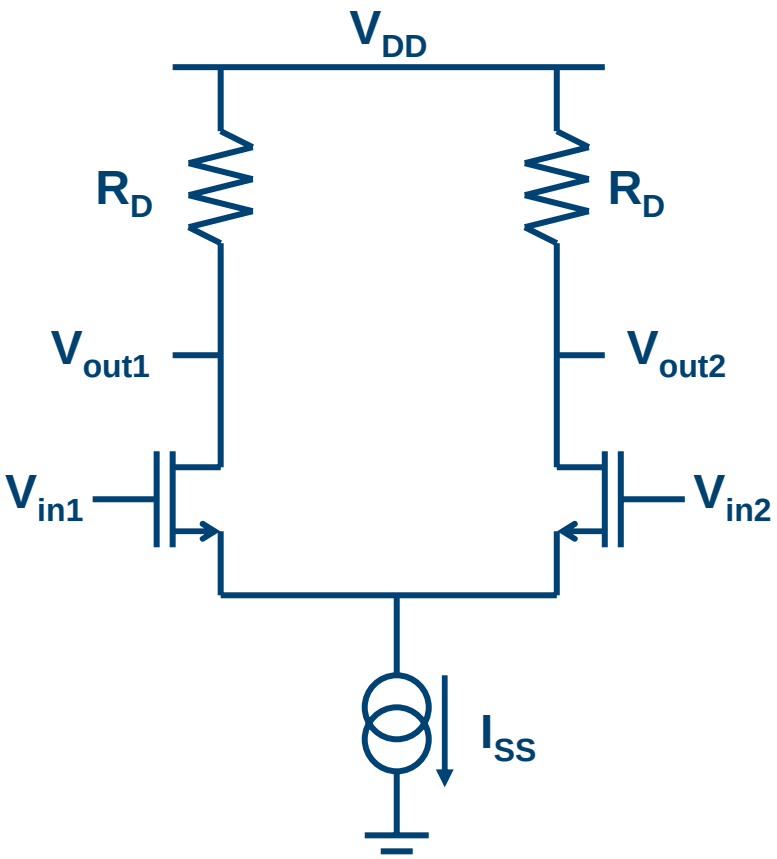


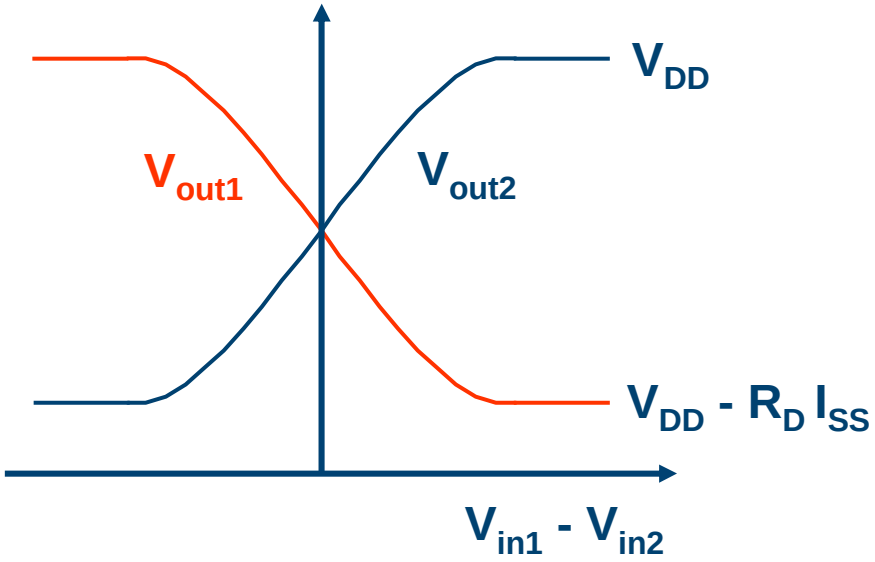
The current source has a very important function, since it makes the sum of the currents in the two branches ($I_1 + I_2 = I_{SS}$) independent from the input common mode voltage.

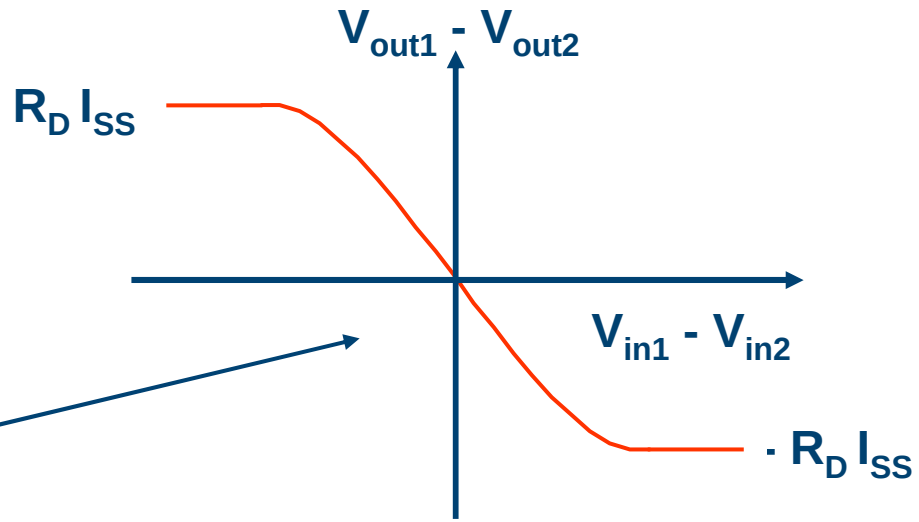
The output common mode voltage is then given by:

$$v_{out,CM} = V_{DD} - R_D \cdot \frac{I_{SS}}{2}$$

Differential Pair



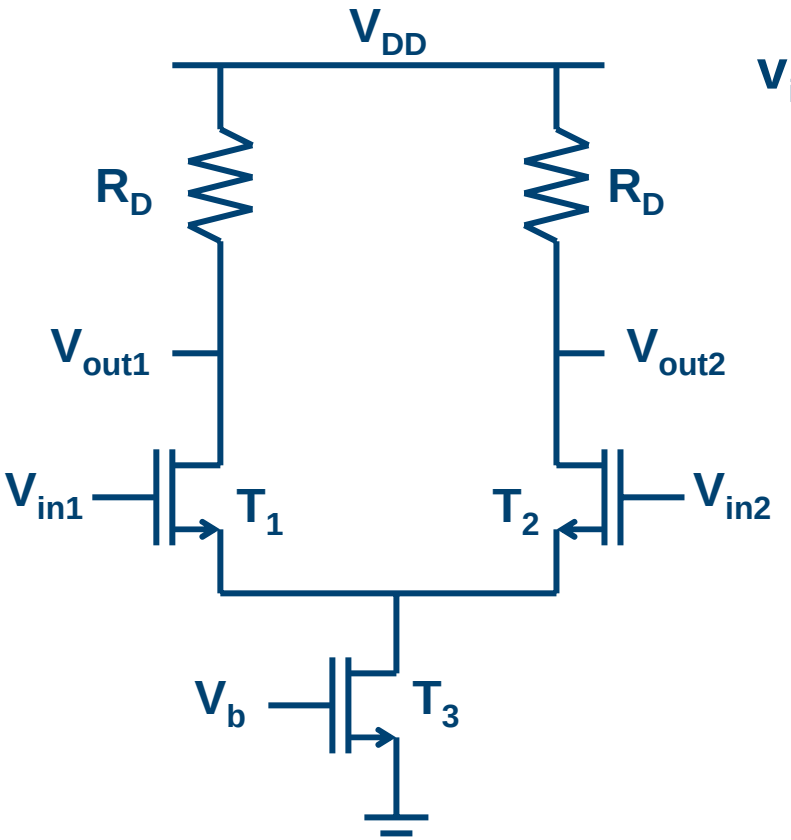




N.B. The small signal gain is the slope of this plot

DP – Common mode analysis

To better understand what can be the maximum voltage excursion of the input, we substitute the ideal current source with a real one.



$$v_{in,CM\_min} = V_{GS1} + (V_{GS3} - V_{T3}) = V_{GS1} + V_{DS\_SAT3}$$

$$v_{in,CM\_max} = \min\left(V_{DD} - R_D \frac{I_{SS}}{2} + V_{T1}, V_{DD} \right)$$

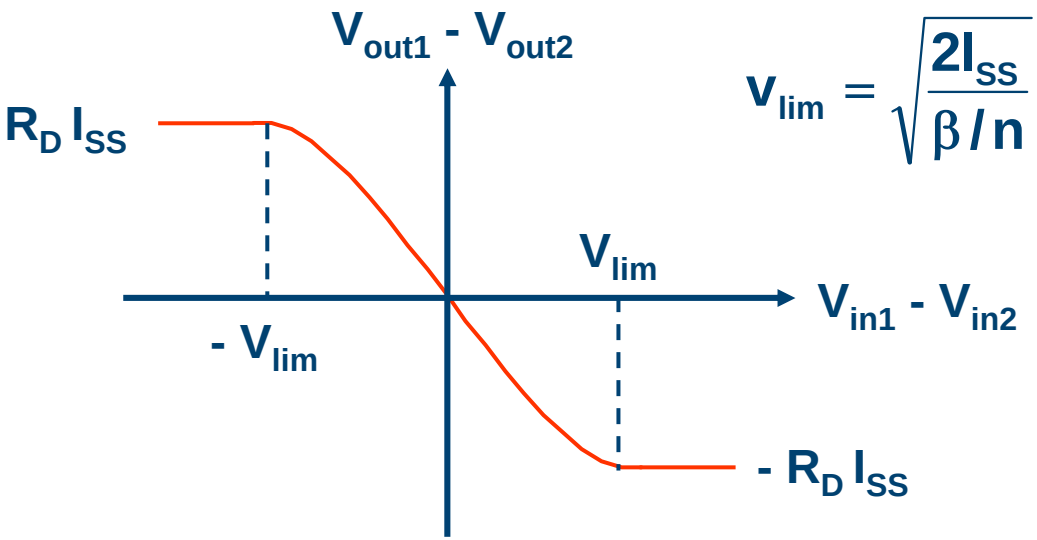
And what can be the maximum excursion of the output?

$$v_{out\_min} = V_{DS\_SAT1} + V_{DS\_SAT3}$$

$$v_{out\_max} = V_{DD}$$

DP - Large signal analysis

With the basic transistor equations, some patience and some mathematics we can obtain the equation for the plot shown.



$$v_{lim} = \sqrt{\frac{2I_{SS}}{\beta / n}}$$

$$v_{out1} - v_{out2} = \Delta V_{out}$$

$$v_{in1} - v_{in2} = \Delta V_{in}$$

$$I_{D1} - I_{D2} = \Delta I$$

$$\Delta V_{out} = -R_D \cdot \Delta I$$

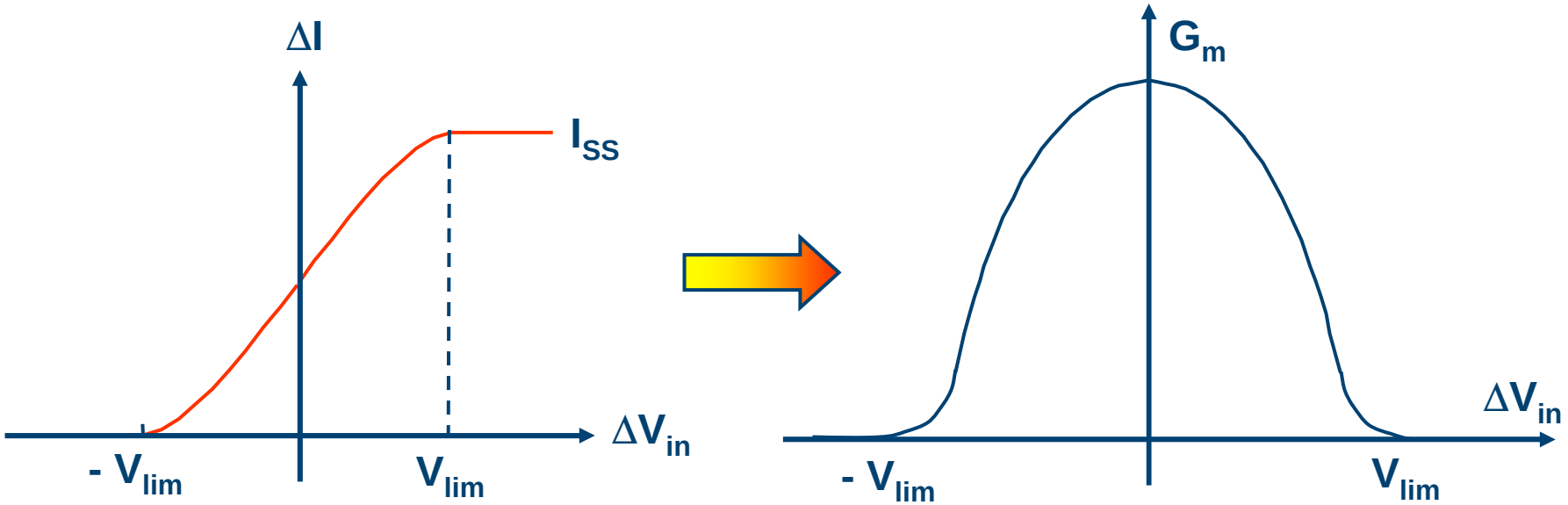
For $\Delta V_{in} < -v_{lim}$ $\quad \Delta I = -I_{SS}$

For $-v_{lim} < \Delta V_{in} < v_{lim}$ $\quad \Delta I = \frac{\beta}{2n} \Delta V_{in} \sqrt{\frac{4I_{SS}}{\beta / n} - \Delta V_{in}^{\,2}}$

For $\Delta V_{in} > v_{lim}$ $\quad \Delta I = I_{SS}$

Differential pair transconductance

Deriving the current difference as a function of the input voltage difference we obtain the transconductance G_m of the differential pair.



$$G_m = \frac{\partial \Delta I}{\partial \Delta V_{in}} = \frac{\beta}{2n} \frac{\frac{4I_{SS}}{\beta / n} - 2\Delta V_{in}^{\ 2}}{\sqrt{\frac{4I_{SS}}{\beta / n} - \Delta V_{in}^{\ 2}}} \xrightarrow{\Delta v_{in} = 0} G_m = \sqrt{\frac{2\beta}{n} \frac{I_{SS}}{2}}$$

DP small signal gain

From the transconductance G_m of the differential pair when the differential stage is balanced ($\Delta v_{in} = 0$), we obtain the small signal gain G.

$$G_m = \sqrt{\frac{2\beta}{n}\frac{I_{SS}}{2}} \qquad \Delta v_{out} = -R_D \cdot \Delta I = -R_D \cdot G_m \cdot \Delta v_{in}$$

$$G = \frac{\Delta v_{out}}{\Delta v_{in}} = -R_D \cdot \sqrt{\frac{2\beta}{n}\frac{I_{SS}}{2}}$$

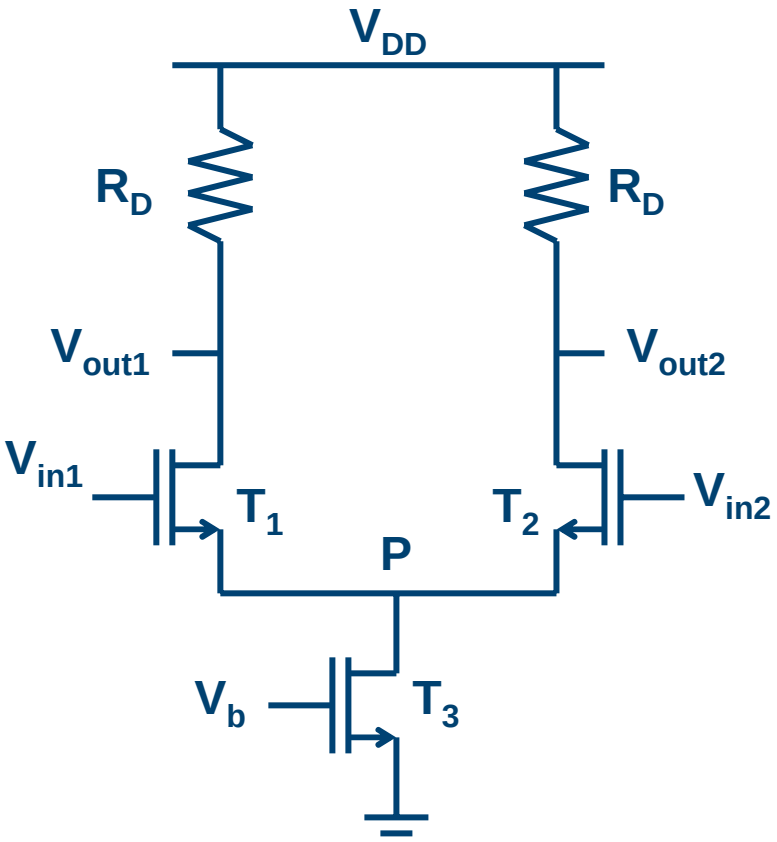
The term circled in red looks suspiciously familiar to us…

It is the transconductance in strong inversion of a transistor carrying a current $I_{SS}/2$! So we can write

$$G = -R_D \cdot g_m$$

DP small signal gain

Now that we know it, is is quite obvious to recognize it looking again at the circuit schematic.



We can see the circuit as two common source stages with degenerated resistor, and superimpose the effects.

Or, even better, we can realize that the point P is (ideally) AC grounded.

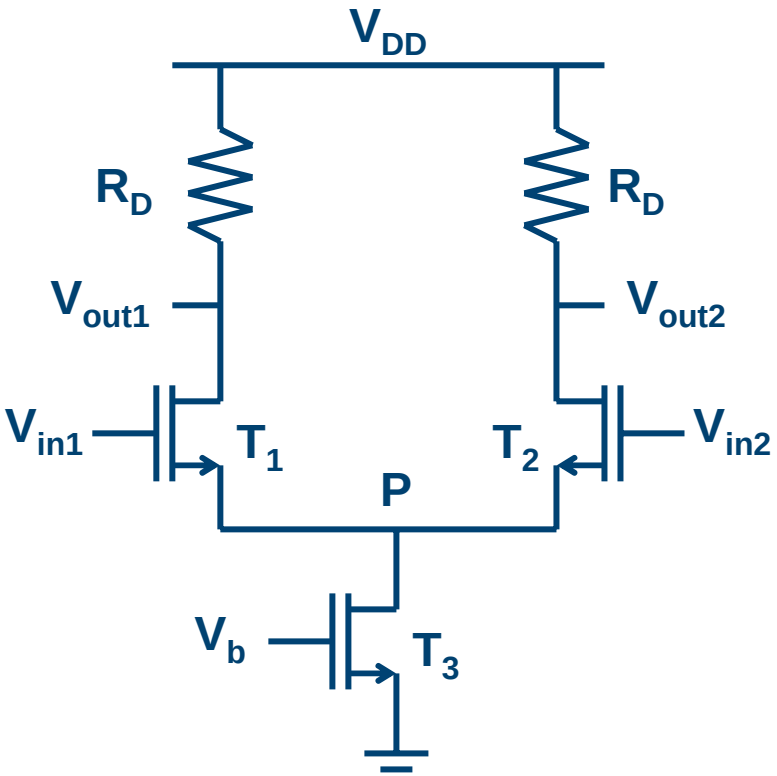
$$v_{out1} = -g_m \cdot R_D \cdot v_{in1}$$

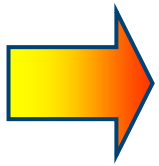
$$v_{out2} = -g_m \cdot R_D \cdot v_{in2}$$

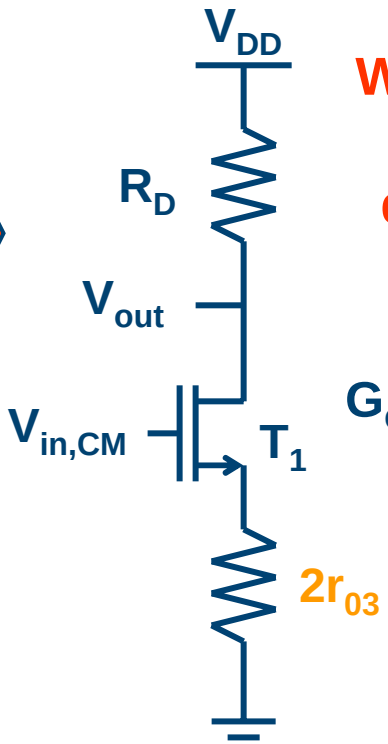
$$v_{out1} - v_{out2} = -g_m \cdot R_D \cdot (v_{in1} - v_{in2})$$

DP Common Mode gain

We have seen that ideally in a differential pair the output voltage does not depend on the common mode input voltage. But in fact the non infinite output impedance r_{03} of the current source has an influence, since the point P do not behave as an AC ground anymore. The symmetry in this circuit suggests that we can see it as two identical half circuits in parallel. This makes the analysis much easier.







What do we have here? A CSS with source degeneration. Easy…

$$G_{CM} = \frac{v_{out}}{v_{in,CM}} = -\frac{R_D}{1/g_m + 2r_0}$$

Common Mode Rejection Ratio

The variation of the common mode output voltage with the common mode input voltage is generally small and not so worrying. MUCH MORE concerning is when we have a differential output as a consequence of a common mode variation at the input! This can happen if the circuit is not fully symmetric (mismatch!).
Let's call $G_{CM\text{-}DM}$ the gain of this common-mode to differential-mode conversion.
A difference in the transconductances of the two transistors, for example, would give:

$$G_{CM-DM} = \frac{\Delta g_m \cdot R_D}{(g_{m1} + g_{m2}) r_{03} + 1}$$

We see that it is essential to have a good current source (very high r_{03}).
To make possible a meaningful comparison between different differential circuit, we want to compare the undesirable differential output given by a common mode input variation and the wanted differential output given by a differential input.

We define the Common Mode Rejection Ratio (CMRR) as: $$CMRR = \left| \frac{G}{G_{CM-DM}} \right|$$

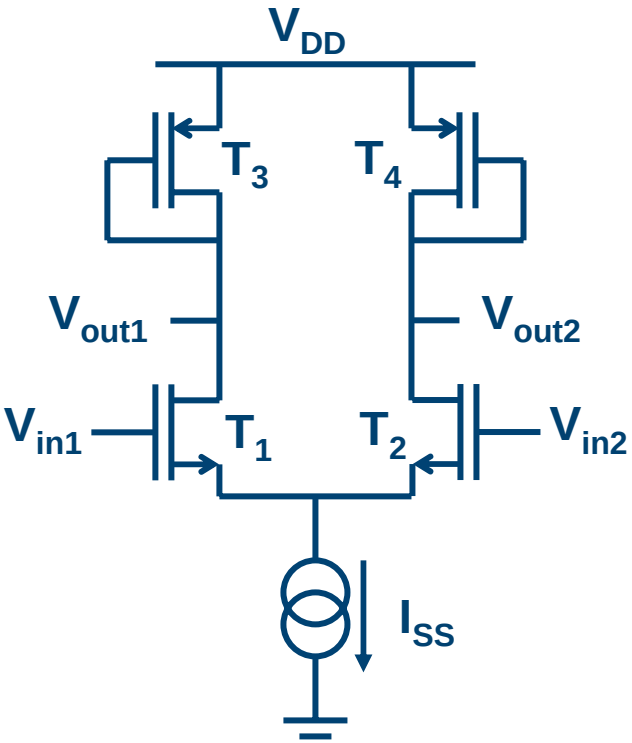
Taking into account ONLY the transconductance mismatch, we obtain $$CMRR \approx \frac{g_m}{\Delta g_m}(1 + 2 g_m r_{03})$$

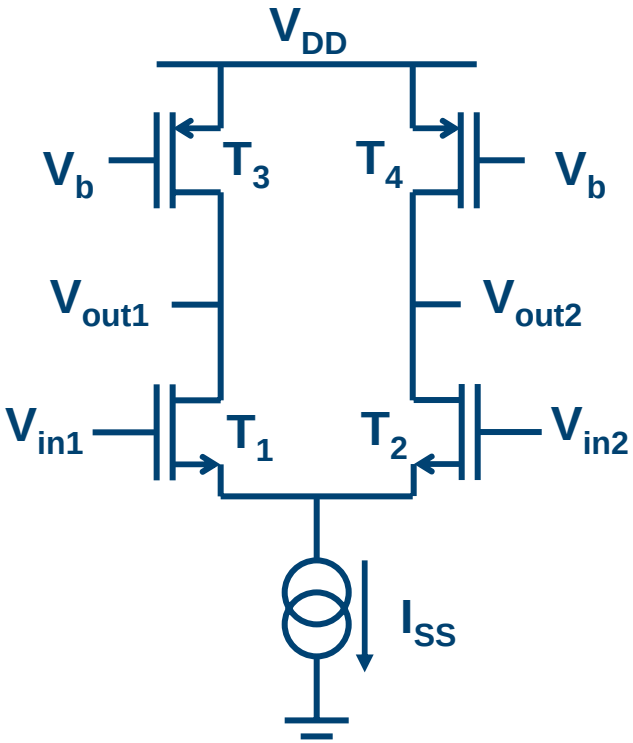
Differential Pair with MOS loads

To analyze the two circuits we can now make use of the half-circuit concept and profit from all the results obtained up to now.

$$G = -g_{mN}\left(\frac{1}{g_{mP}} /\!/ r_{0N} /\!/ r_{0P}\right) \approx -\frac{g_{mN}}{g_{mP}}$$

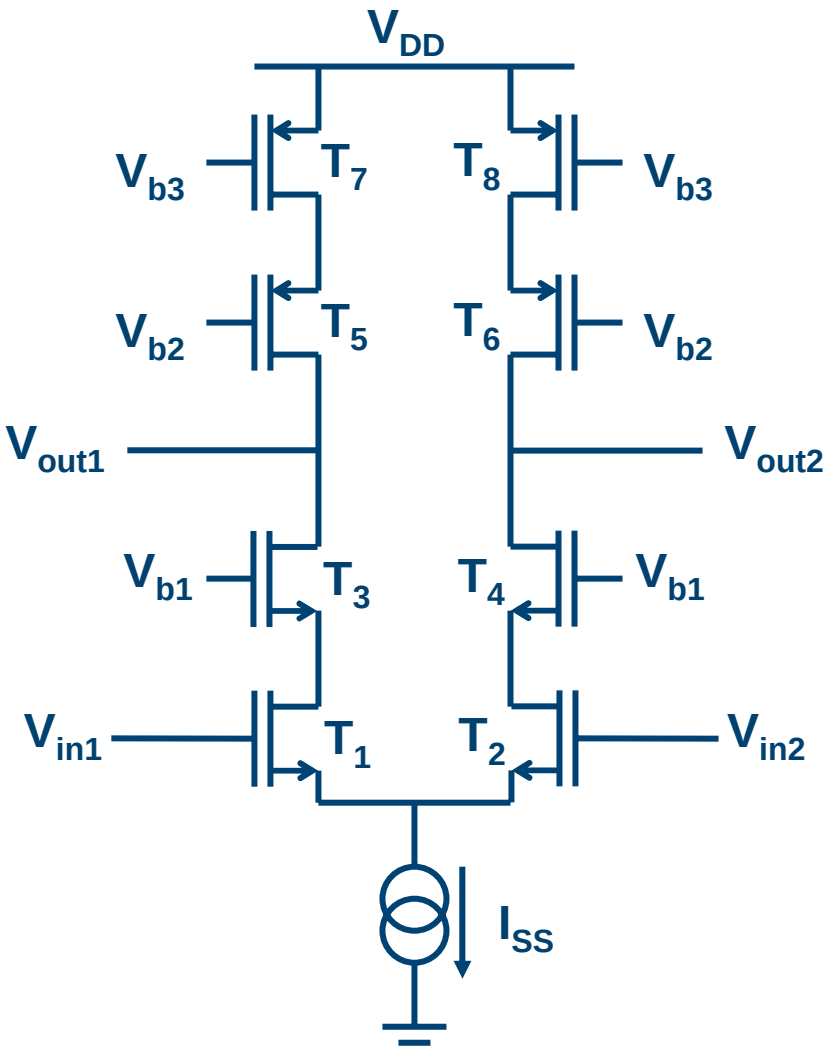
$$G = -g_{mN}\left(r_{0N} /\!/ r_{0P}\right)$$





Cascode Differential Pair

And, of course, the gain can be boosted using common-gate stages.



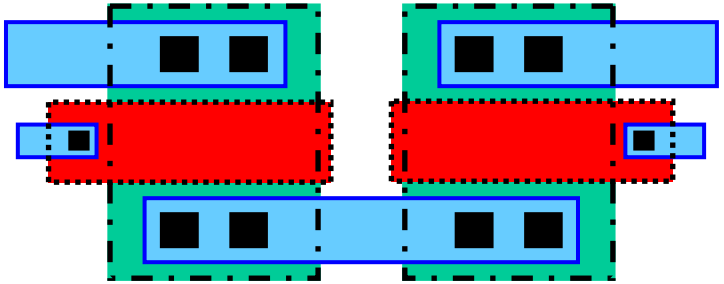
$$G \approx -g_{m1}\left(g_{m3}r_{03}r_{01} \,//\, g_{m5}r_{05}r_{07}\right)$$

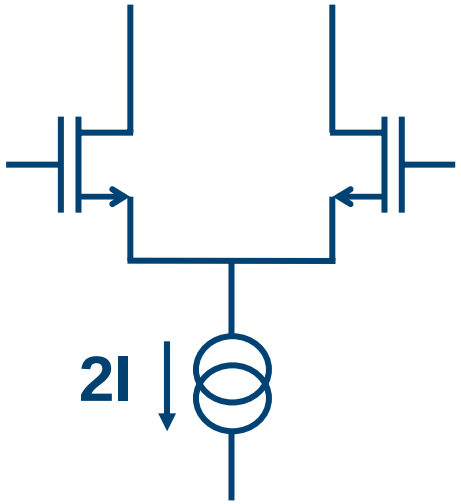
Cascode stages were used a lot in the past, when the supply voltages were relatively high (few volts).

In deep submicron technologies they are used with more care.

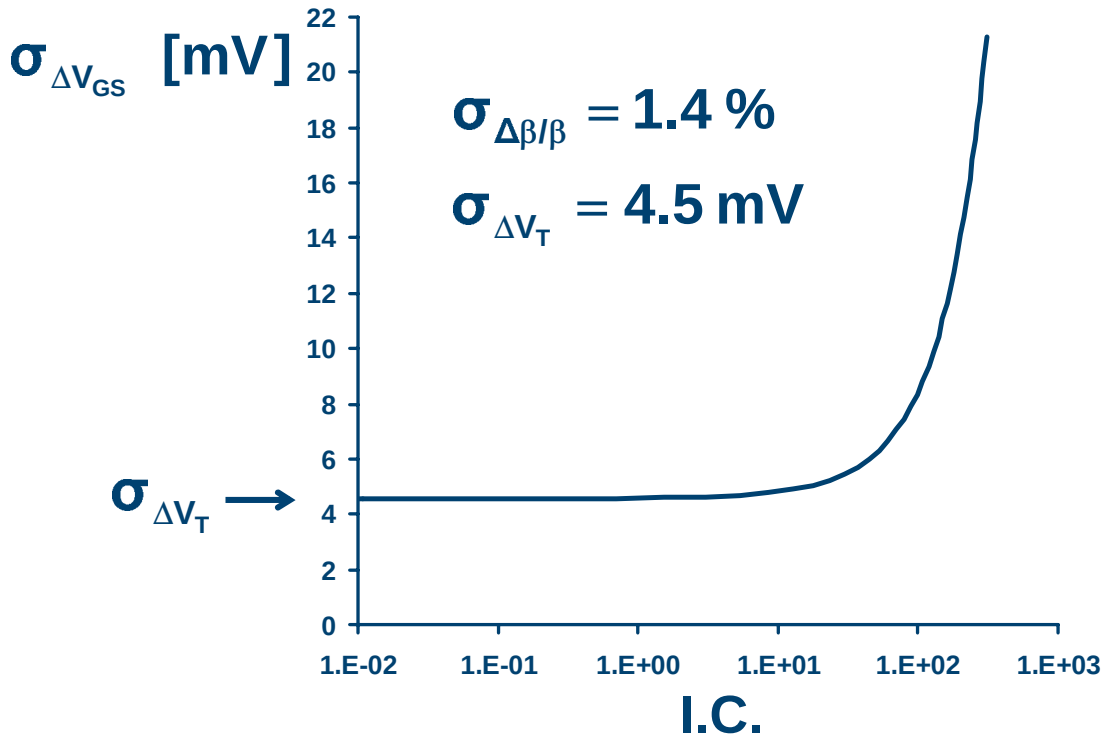
Differential pair mismatch

The two transistors have the same drain current

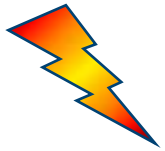




$$\sigma_{\Delta V_{GS}} = \sqrt{\sigma^2_{\Delta V_{th}} + \left(\frac{I}{g_m}\sigma_{\Delta\beta/\beta}\right)^2}$$



Outline



- Single-stage amplifiers
- The differential pair
- The current mirror
  - Standard Current Mirror
  - Cascode Current Mirror
  - Low-voltage Cascode Current Mirror
  - Current Mirror Output Impedance
  - Current Mirror Mismatch
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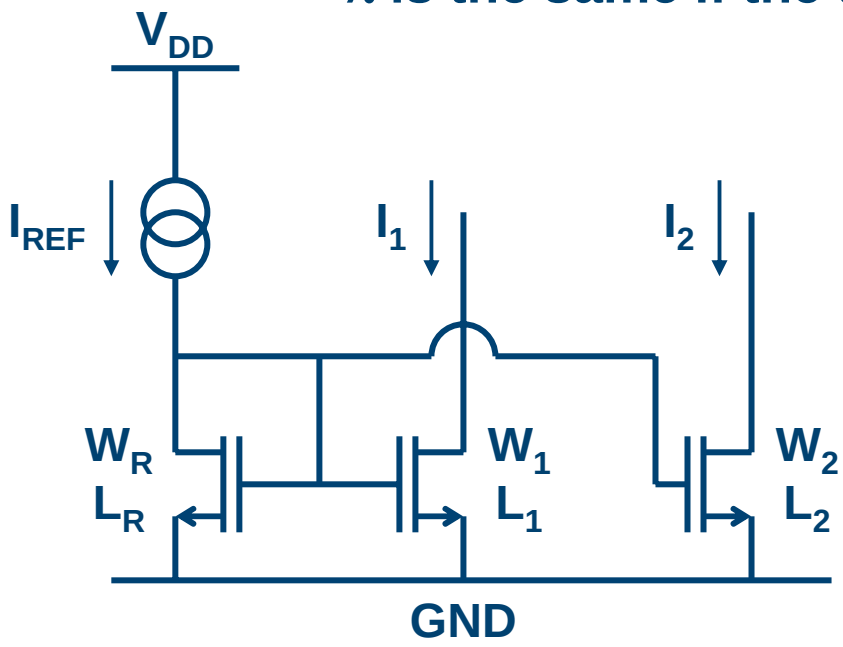
Current mirror (CM)

We suppose that all the transistors have the same μ, C_{ox} and V_T.
λ is the same if the transistors have the same L

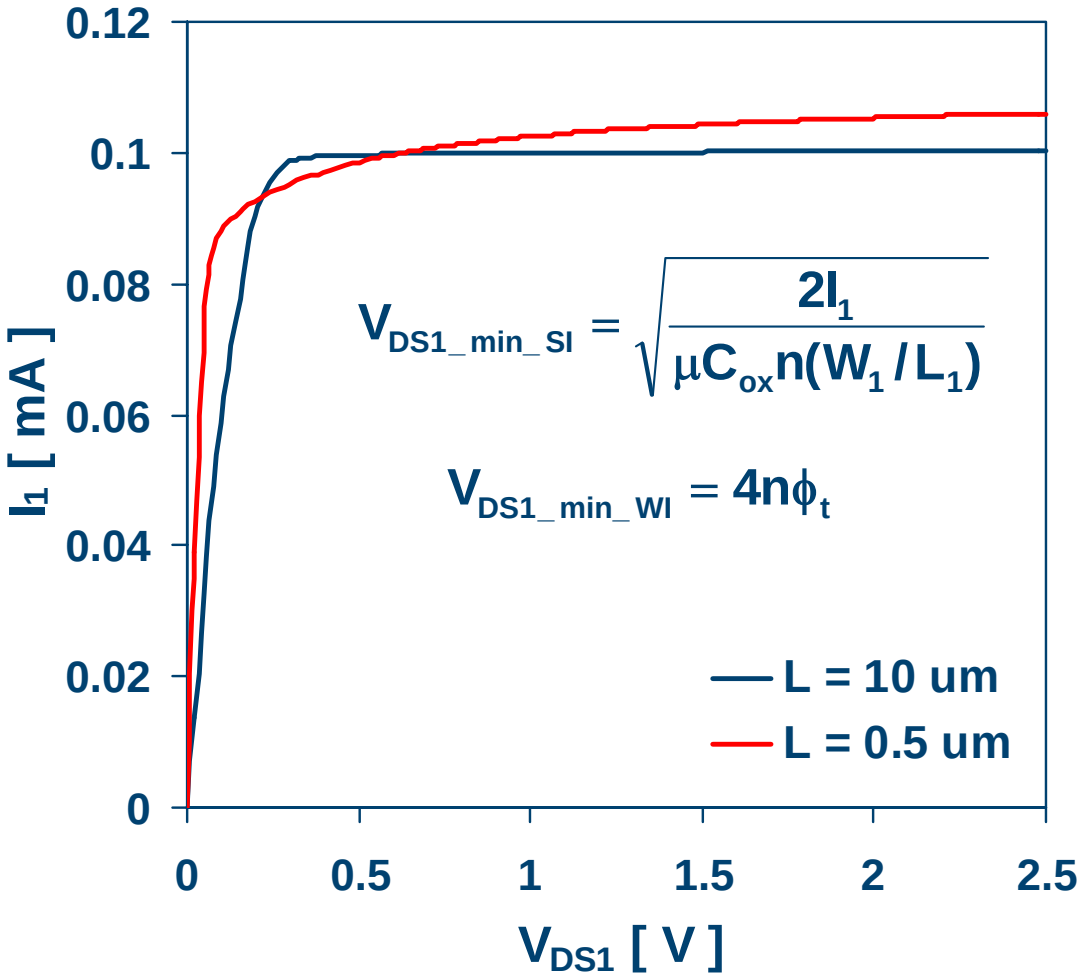


$$I_1 = I_{REF} \cdot \frac{\frac{W_1}{L_1}\left(1+\lambda_1 V_{DS1}\right)}{\frac{W_R}{L_R}\left(1+\lambda_R V_{DSR}\right)}$$

To have an exact replica of the reference current, we have to make the transistor identical AND they must have the same V_{DS}. When this is not possible, choosing long devices reduces the effect of λ.
Precise current ratios can be obtained playing with the ratio between the transistor widths (not the lengths!).

Current mirror simulation

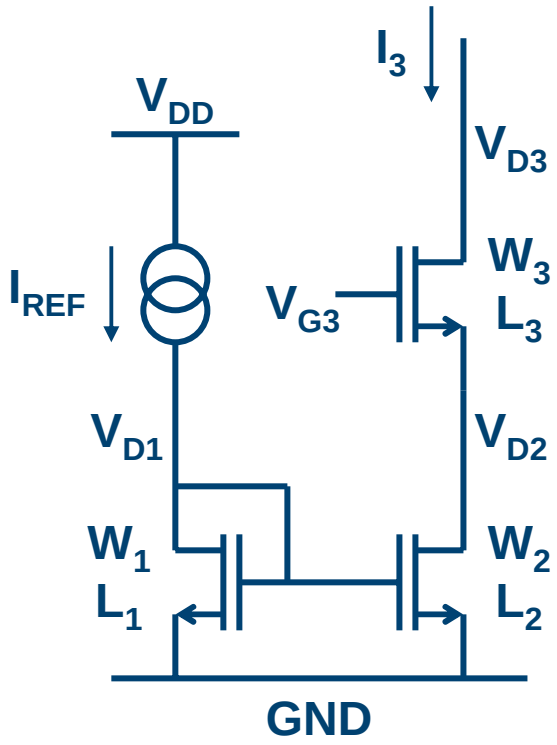
0.25 μm technology, V_{DD} = 2.5 V, I_{REF} = 100 μA, $W_R = W_1$ = 100 μm, $L_R = L_1$



@ V_{DS1} = 2.5 V

T1	L = 0.5 [μm]	L = 10 [μm]
I_D [μA]	106	100.3
β [mA/V²]	60.54	2.488
g_m [mS]	1.77	0.594
V_T [mV]	635.7	635.6
V_{GS} [mV]	636.7	943
V_{DS_sat} [mV]	70.76	269.7
R_{out} [MΩ]	0.866	14.5

Cascode current mirror (CCM)



V_{G3} must be fixed so that $V_{D1} = V_{D2}$.

Making $L_1 = L_2$ and therefore having $\lambda_1 = \lambda_2$, we obtain that the current I_3 practically does not depend on the voltage V_{D3}. Of course, all the devices must be in saturation (the circuit is not suitable for low voltage applications).

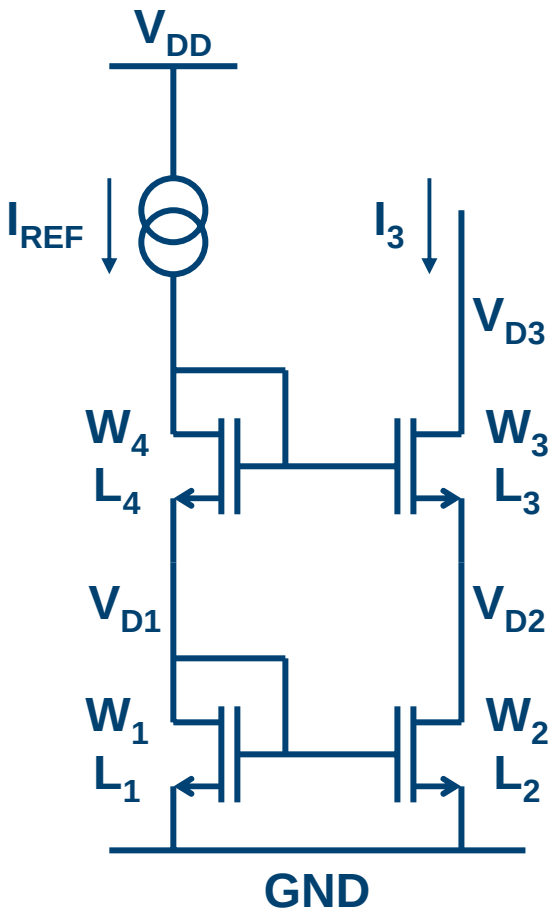
$$I_3 = I_{REF} \cdot \frac{W_2 / L_2}{W_1 / L_1}$$

$$\Delta V_{D2} \approx \frac{\Delta V_P}{(g_{m3} + g_{mb3}) \cdot r_{03}}$$

Important: L_3 can be different from L_1 and L_2.

How do we fix V_{G3} so that $V_{D1} = V_{D2}$?

Cascode current mirror (CCM)



Transistor 4 does the job here!

Transistors 1 & 2 decide the current ratio.

Transistors 3 & 4 fix the bias $V_{D1} = V_{D2}$.

These results are valid even if transistors 3 & 4 suffer from body effect.

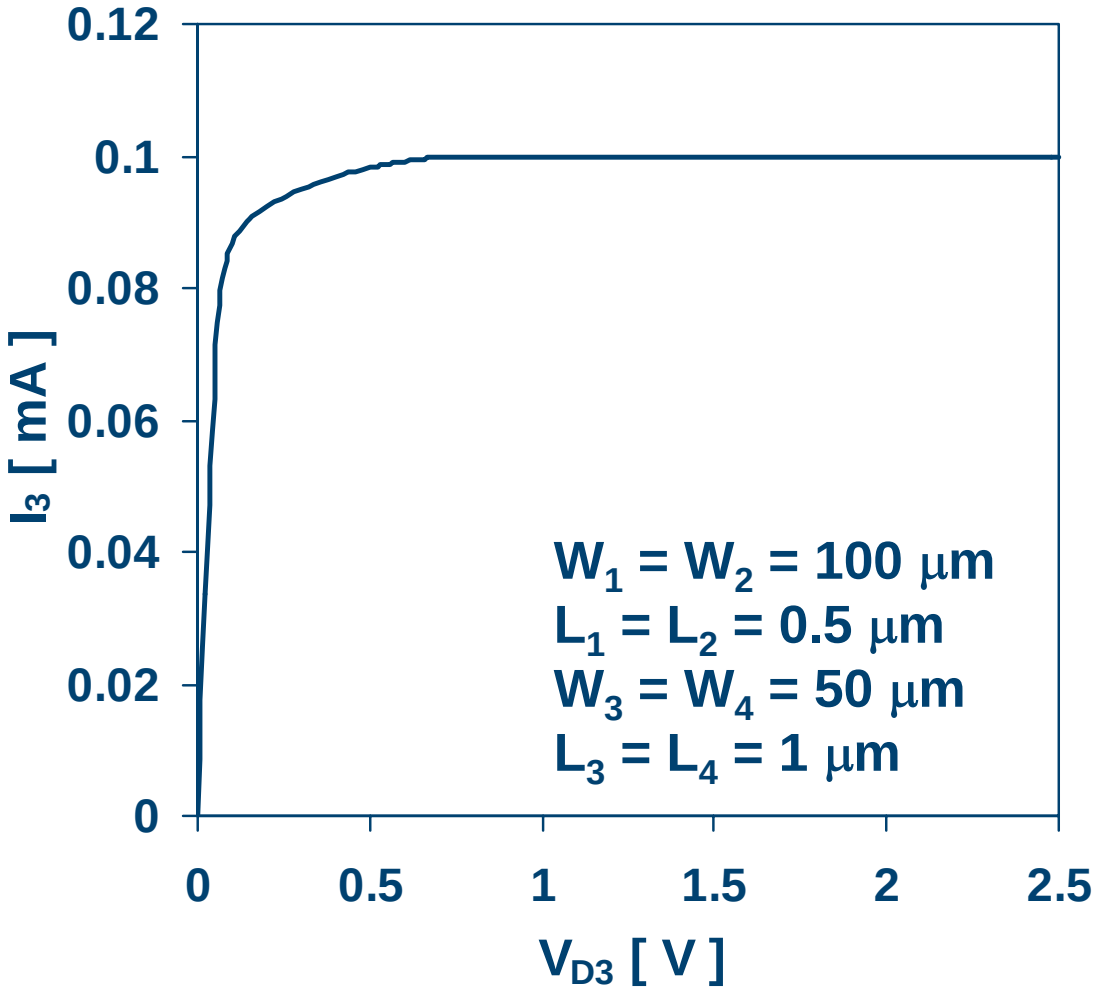
$$I_3 = I_{REF} \cdot \frac{W_2/L_2}{W_1/L_1}$$

$$\frac{W_2/L_2}{W_1/L_1} = \frac{W_3/L_3}{W_4/L_4}$$

The problem of this current mirror is that $V_{D3} > V_{DS3} + V_{GS2}$.

Cascode current mirror simulation

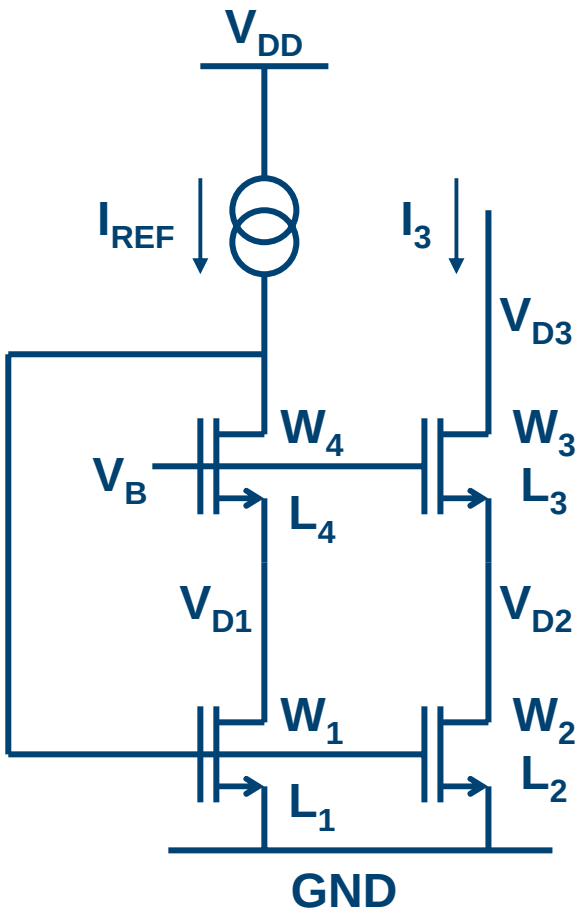
0.25 μm technology, V_{DD} = 2.5 V, I_{REF} = 100 μA



@ V_{D3} = 2.5 V

	T2	T3
I_D [μA]	100	100
β [mA/V²]	60.54	13.08
g_m [mS]	1.676	1.211
V_T [mV]	635.7	852
V_{GS} [mV]	636.7	962.4
V_{DS_sat} [mV]	70.75	128.7
R_{out} [MΩ]	0.108	1.037

Low Voltage CCM (LVCCM)



The main difference of this current mirror compared to the standard cascode current mirror is that here we can lower the voltages V_{D1} and V_{D2} to the limit of the saturation of transistors T1 and T2.

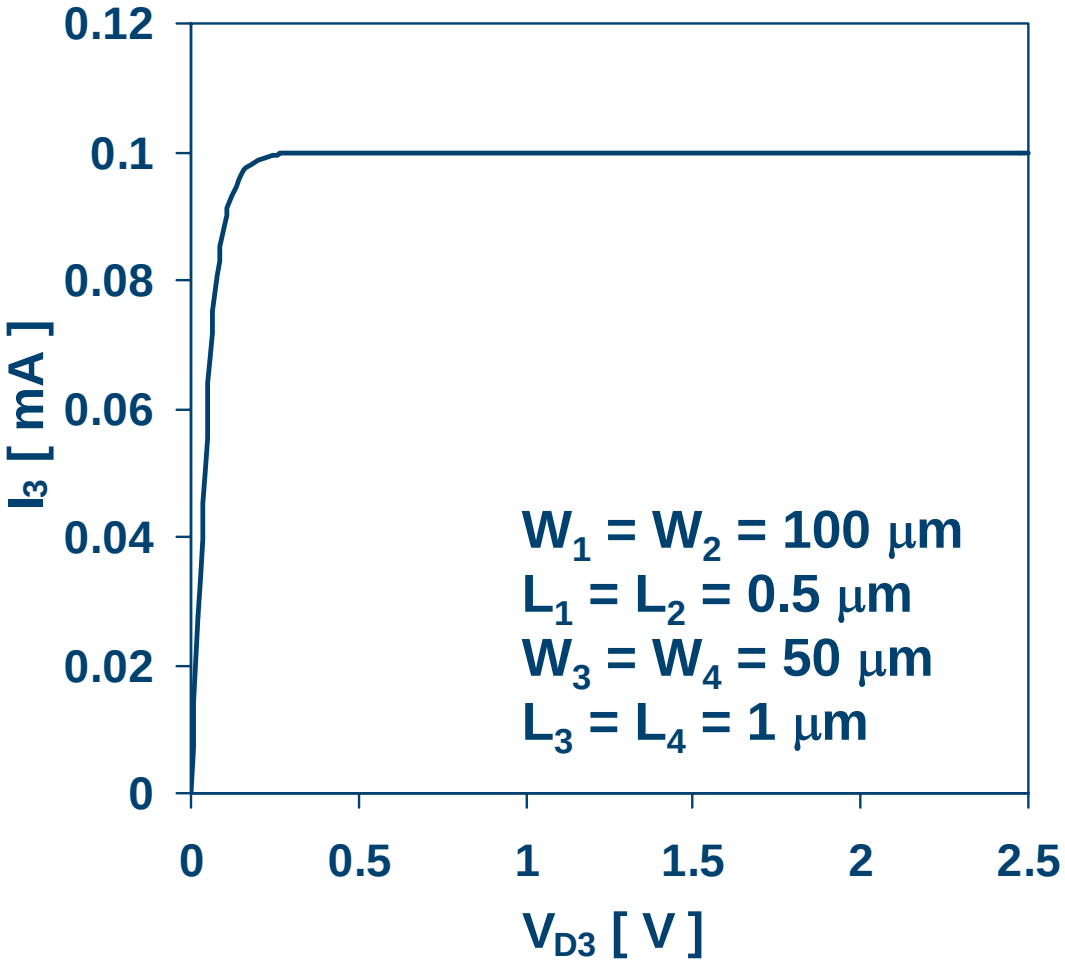
$$I_3 = I_{REF} \cdot \frac{W_2/L_2}{W_1/L_1}$$

$$\frac{W_2/L_2}{W_1/L_1} = \frac{W_3/L_3}{W_4/L_4}$$

The minimum output voltage (V_{D3}) here is just two saturation voltages.

Low Voltage CCM simulation (1)

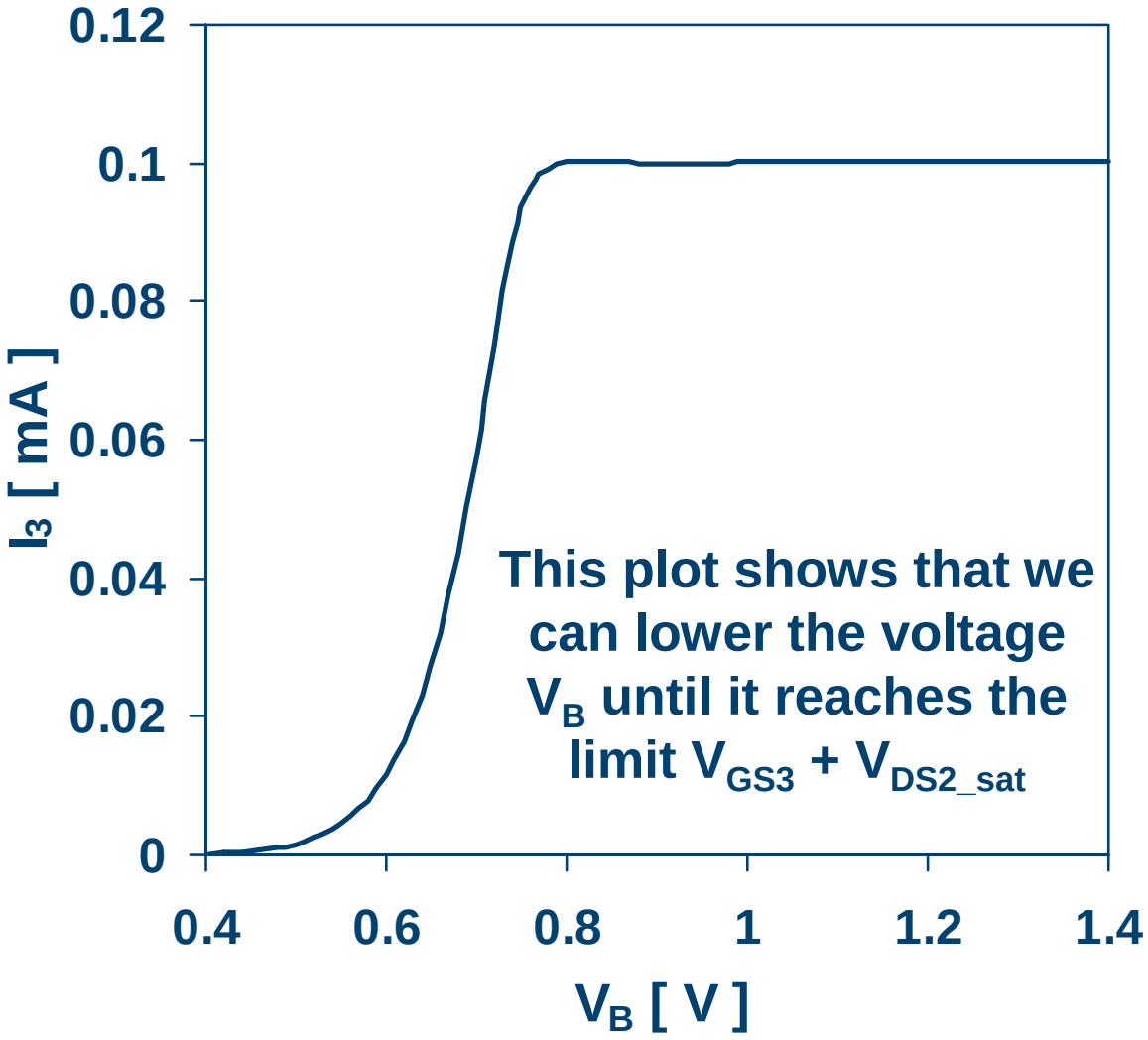
0.25 μm technology, V_{DD} = 2.5 V, I_{REF} = 100 μA

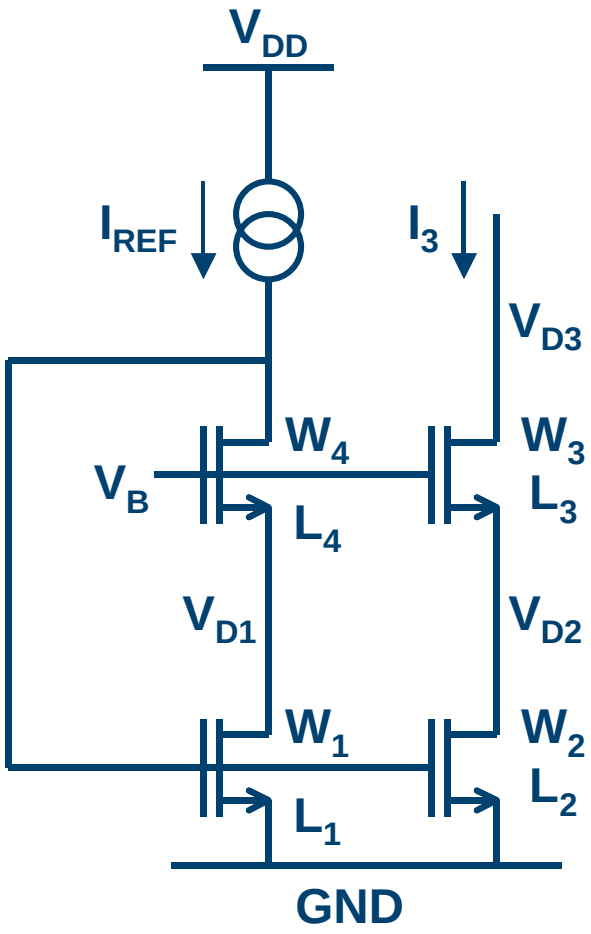


@ V_{D3} = 2.5 V

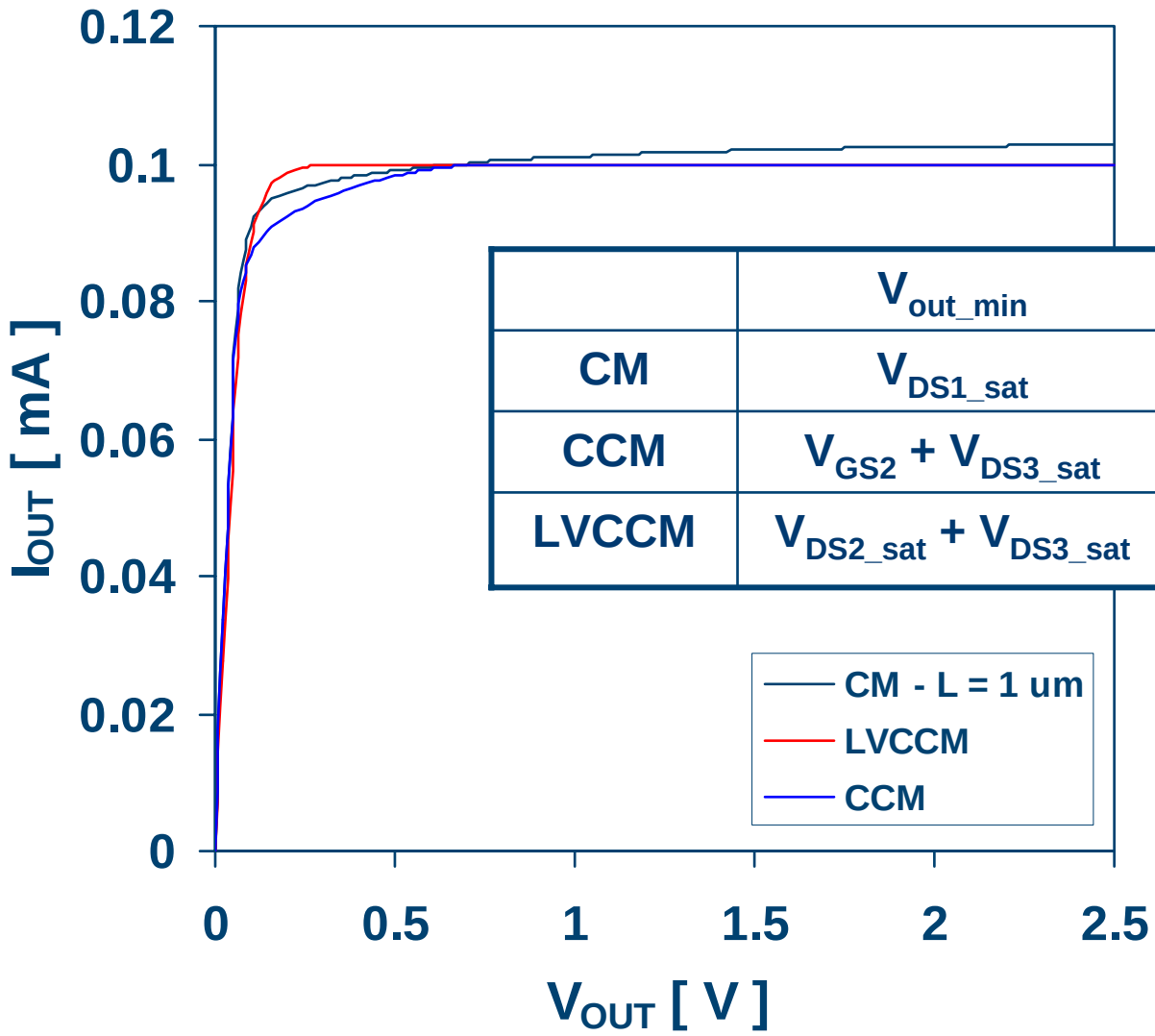
	T2	T3
I_D [μA]	100	100
β [mA/V²]	60.5	13.57
g_m [mS]	1.641	1.208
V_T [mV]	635.7	692.4
V_{GS} [mV]	642.5	798.3
V_{DS_sat} [mV]	72.87	123.6
R_{out} [MΩ]	0.021	1.6

Low Voltage CCM simulation (2)



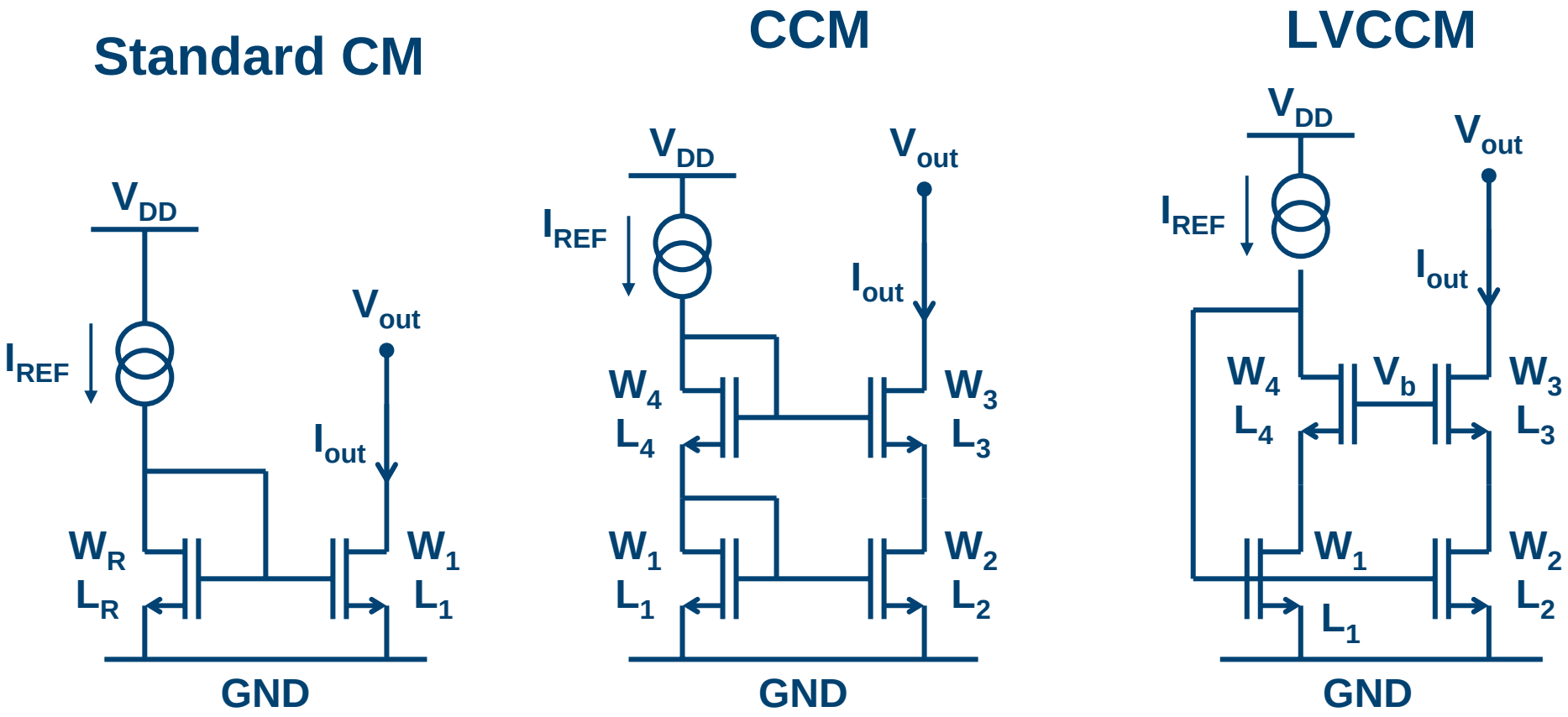


Current mirrors: comparison



	V_{out_min}	Precision
CM	V_{DS1_sat}	Poor (unless large L)
CCM	$V_{GS2} + V_{DS3\_sat}$	Good
LVCCM	$V_{DS2\_sat} + V_{DS3\_sat}$	Good

Current mirror output impedance

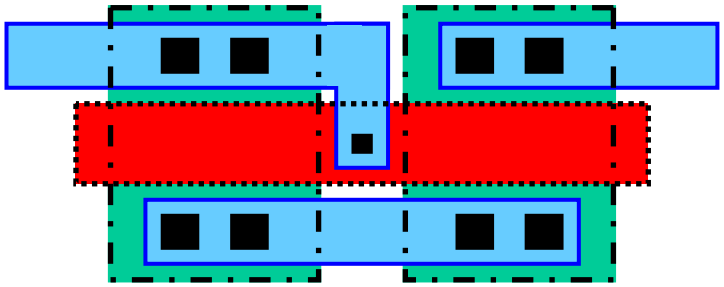


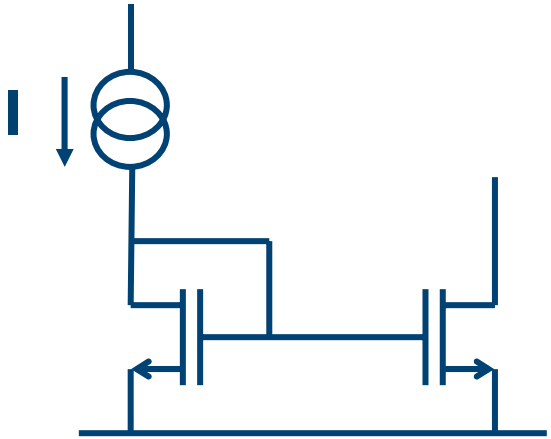
$$r_{out} = r_{01}$$

$$r_{out} = r_{02} + r_{03} + \left(g_{m3} + g_{mb3}\right) \cdot r_{02} r_{03}$$

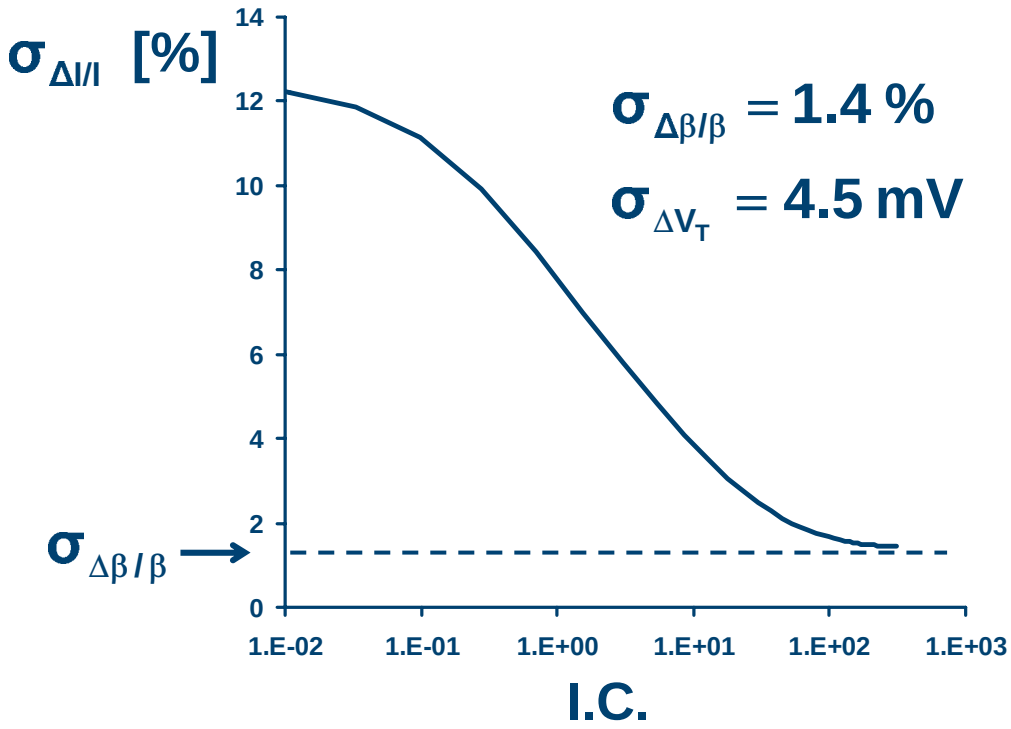
Current mirror mismatch

The two transistors have the same gate voltage





$$\sigma_{\Delta I/I} = \sqrt{\sigma^2_{\Delta\beta/\beta} + \left(\frac{g_m}{I}\sigma_{\Delta V_{th}}\right)^2}$$

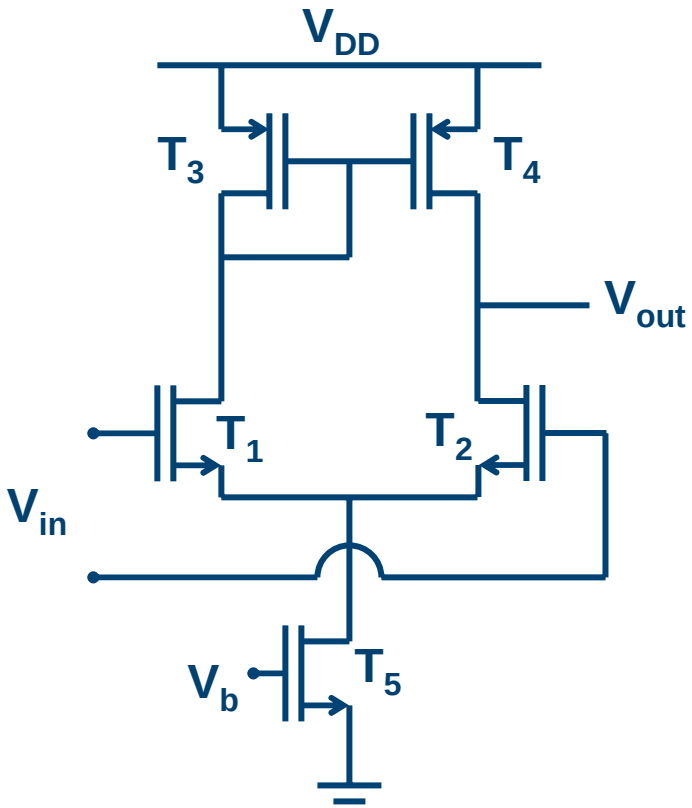


Outline

- Single-stage amplifiers
- The differential pair
- The current mirror
- Differential pair + active current mirror
  - Common mode, small signal and large signal analysis
  - Noise
  - Offset
- Frequency analysis of an amplifier
- Operational amplifier (op amp) design

Differential Pair + Active CM

Current mirrors can also process a signal, and they can therefore be used as active elements. A differential pair with an active current mirror is also called a differential pair with active load. The current mirror here has also the important role to make a differential to single-end conversion!



Common Mode Analysis

$$v_{in,CM\_min} = V_{GS1} + V_{DS\_SAT5}$$

$$v_{in,CM\_max} = \min\left(V_{DD} - V_{GS3} + V_{T1}, V_{DD}\right)$$

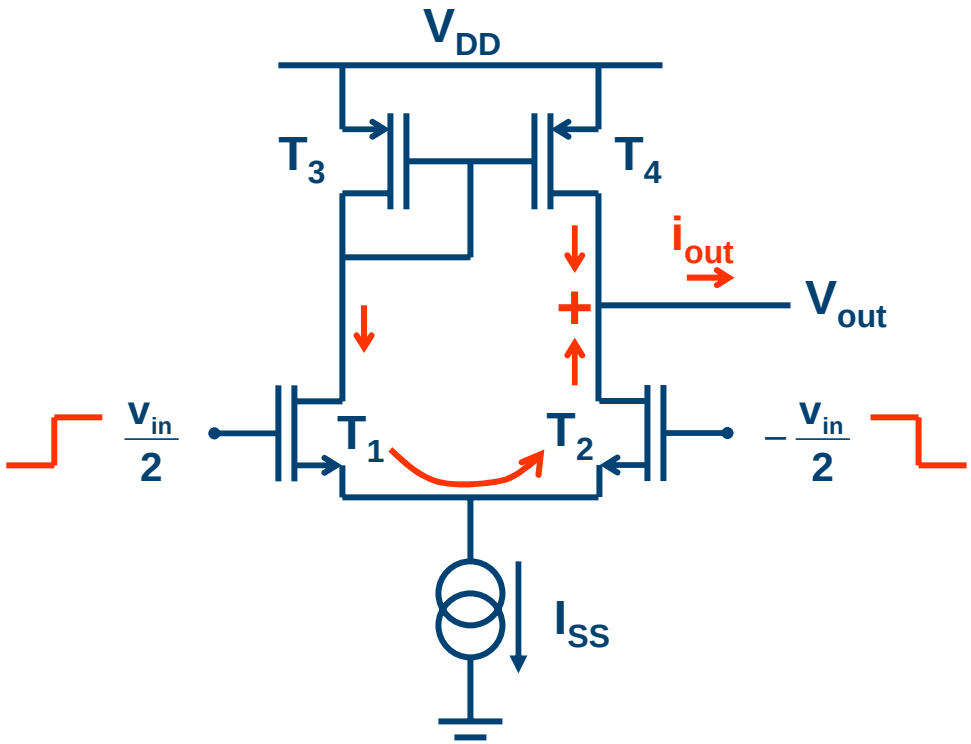
Maximum output excursion

$$v_{out\_min} = V_{DS\_SAT2} + V_{DS\_SAT5}$$

$$v_{out\_max} = V_{DD} - V_{DS\_SAT4}$$

Differential Pair + Active CM

Let's now calculate the small-signal behavior, neglecting the bulk effect for simplicity. The circuit is NOT symmetric, and therefore we can not use the half-circuit principle here. As a first approximation, we can consider the common sources of the input transistors as a virtual ground. The small-signal gain G can be seen as the product of the total transconductance of the stage and of the output resistance.



$$G = G_m \cdot R_{out}$$

$$i_{out} = -g_{m1}\frac{v_{in}}{2} - g_{m2}\frac{v_{in}}{2} = -g_{m1,2} \cdot v_{in}$$

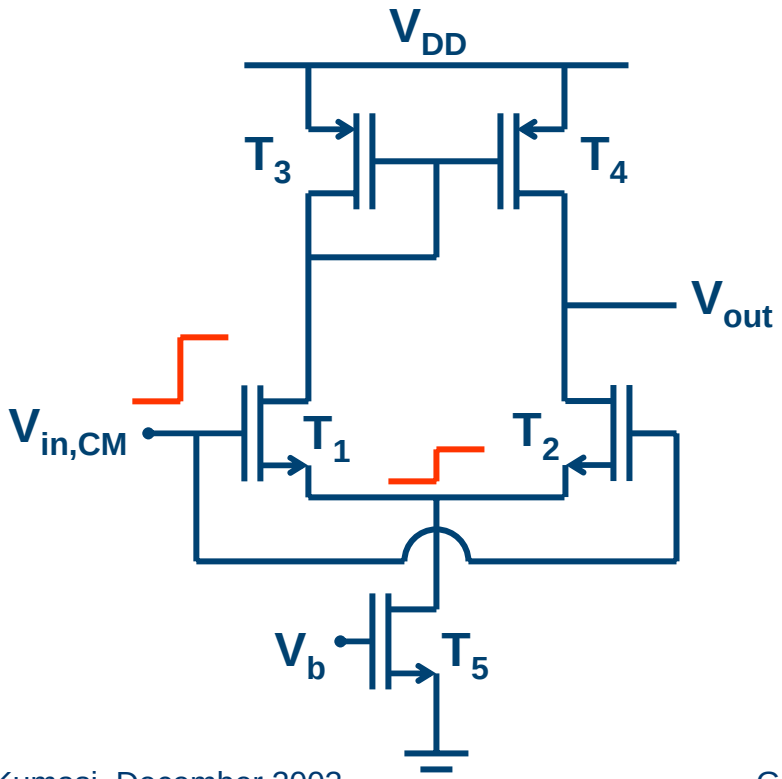
$$G_m = \frac{i_{out}}{v_{in}} = -g_{m1,2}$$

$$R_{out} = r_{02} \,//\, r_{04}$$

$$G = -g_{m1,2}\left(r_{02} \,//\, r_{04}\right)$$

Differential Pair + Active CM

In reality, the current source is not ideal, and this has an effect on the gain we have just calculated. This effect is in general negligible. What is not negligible is the effect of r_{05} on the common mode gain. For a common mode input signal the circuit can be seen symmetric! It can be shown that even for a perfectly symmetric circuit (no mismatch) a CM signal at the input ($\Delta v_{in,CM}$) generates an unwanted signal at the output (Δv_{out}).

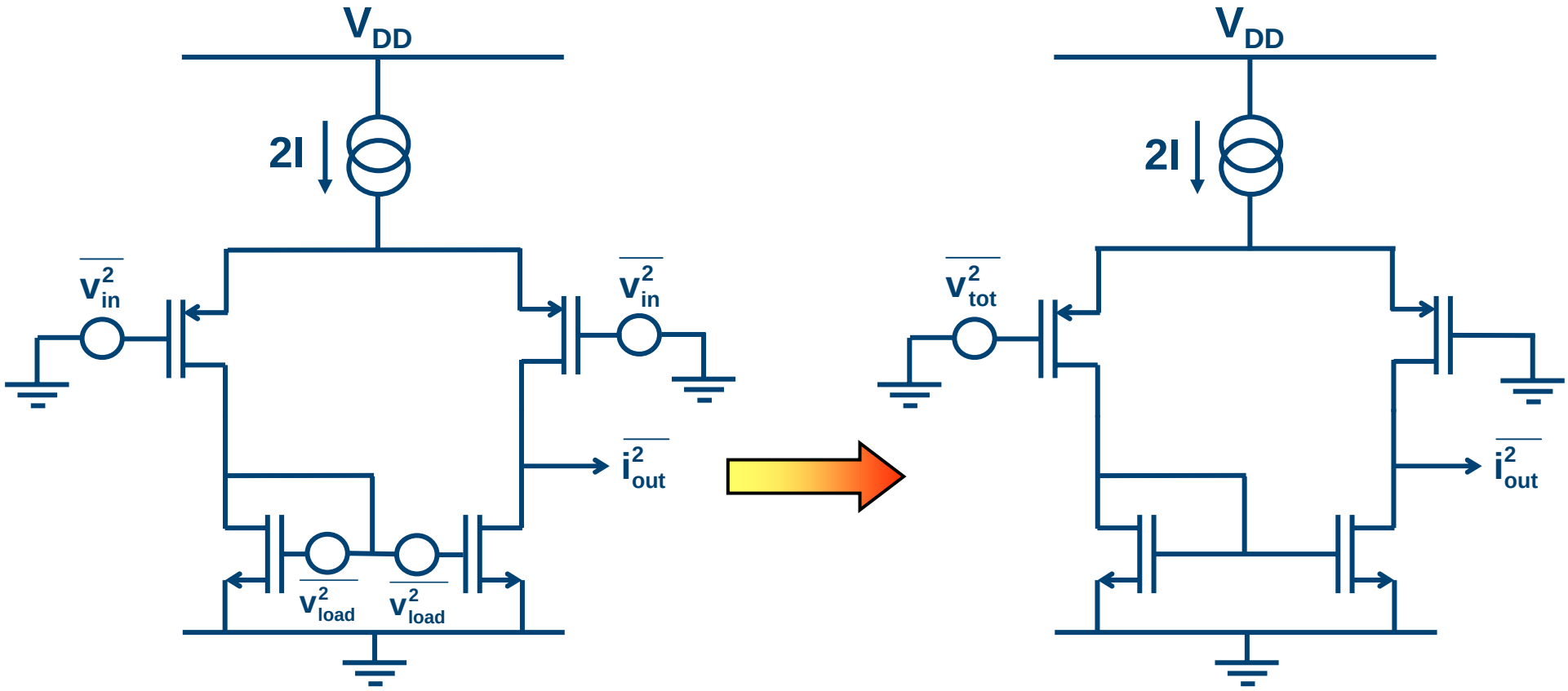


Common Mode Gain (neglecting bulk effect and $r_{01,2}$)

$$G_{CM} = \frac{\Delta V_{out}}{\Delta V_{in,CM}} = -\frac{\frac{1}{2g_{m3,4}} // \frac{r_{03,4}}{2}}{\frac{1}{2g_{m1,2}} + r_{05}} =$$

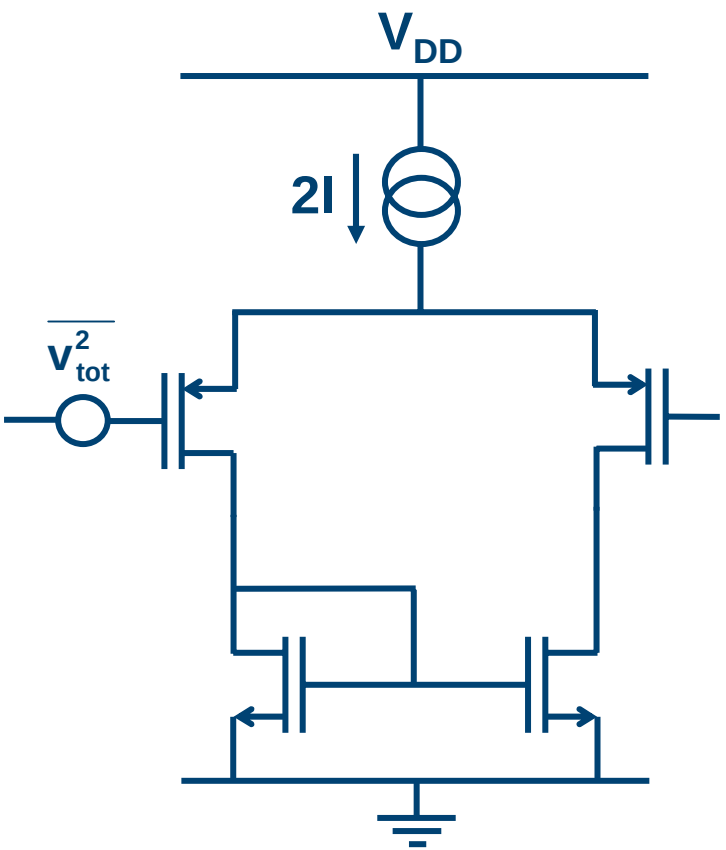
$$= -\frac{1}{1 + 2g_{m1,2}r_{05}} \frac{g_{m1,2}}{g_{m3,4}}$$

Noise in a DP + Active CM



$$\overline{v_{tot}^2} = 2 \cdot \overline{v_{in}^2} + 2 \cdot \left(\frac{g_{m\_load}^2}{g_{m\_in}^2} \right) \cdot \overline{v_{load}^2}$$

Noise in a DP + Active CM



$$\overline{v_{tot\_1/f}^2} = 2 \cdot \frac{K_{a\_in}}{C_{ox}^2 W_{in} L_{in}} \cdot \frac{1}{f} \cdot \left(1 + \frac{K_{a\_load} \cdot \mu_{load} \cdot L_{in}^2}{K_{a\_in} \cdot \mu_{in} \cdot L_{load}^2}\right) \cdot \Delta f$$

⇩

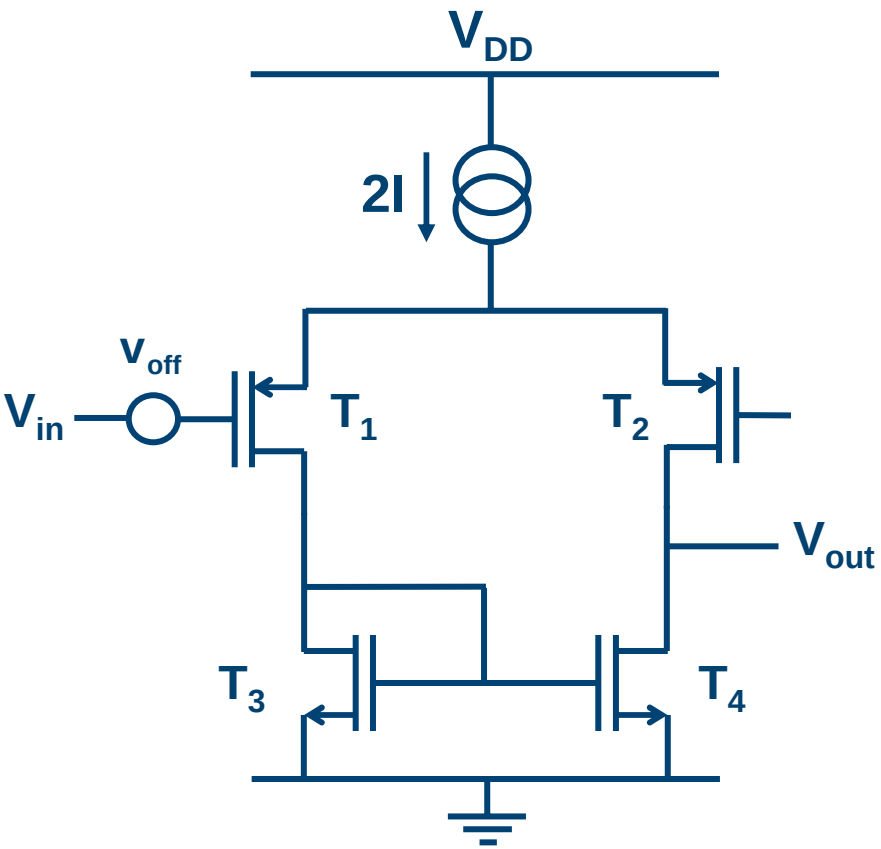
Make $W_{in} L_{in}$ big and $L_{load} > L_{in}$

$$\overline{v_{tot\_th}^2} = 4kTn\gamma \cdot \frac{2}{\sqrt{2\mu_{in} C_{ox} \frac{W_{in}}{L_{in}} I}} \cdot \left(1 + \sqrt{\frac{\mu_{load}\left(\frac{W}{L}\right)_{load}}{\mu_{in}\left(\frac{W}{L}\right)_{in}}}\right) \cdot \Delta f$$

⇩

Make $\left(\frac{W}{L}\right)_{in} > \left(\frac{W}{L}\right)_{load}$

Offset of a DP + Active CM



RANDOM OFFSET (WORST CASE)

$$v_{off} = \Delta V_{T1,2} + \frac{I}{g_{m1,2}}\left(\frac{\Delta\beta_{1,2}}{\beta_{1,2}} + \frac{\Delta\beta_{3,4}}{\beta_{3,4}} + \frac{g_{m3,4}}{I}\Delta V_{T3,4}\right)$$

SYSTEMATIC OFFSET

The difference in the drain voltages of T1 and T2 gives origin a difference in the DC currents in the two branches.

"COMMON MODE" OFFSET

As we have already seen, a common mode signal at the input gives a non zero output voltage signal.

List of Acronyms

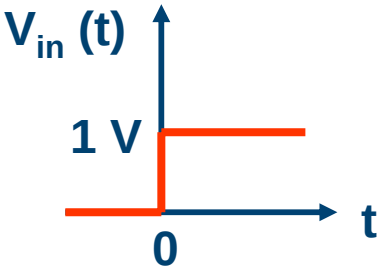
- **CSS:** **Common-Source Stage**
- **CSS-CSL:** **Common-Source Stage with Current Source Load**
- **SF:** **Source Follower (also called Common-Drain Stage)**
- **CGS:** **Common-Gate Stage**
- **CascS:** **Cascode Stage = CSS + CGS**
- **FCascS:** **Folded Cascode Stage**
- **DP:** **Differential Pair**
- **CM:** **Current Mirror**
- **CCM:** **Cascode Current Mirror**
- **LVCCM:** **Low-Voltage Cascode Current Mirror**
- **CMRR:** **Common Mode Rejection Ratio**

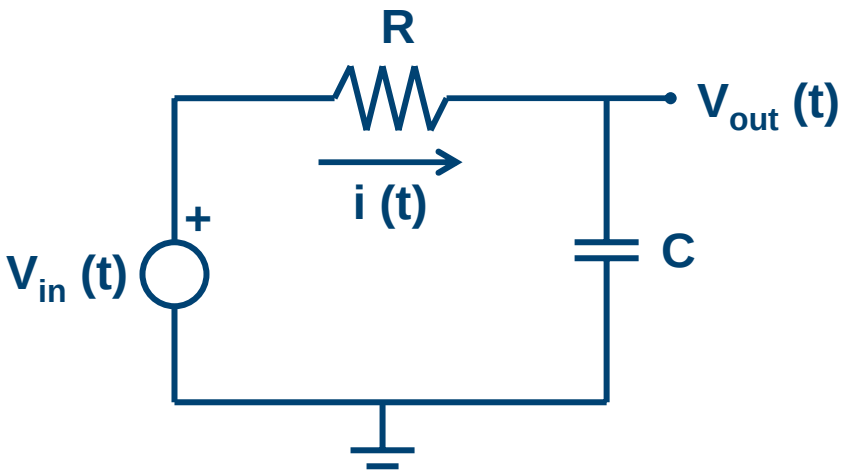
sorry… ☺

Outline

- Single-stage amplifiers
- The differential pair
- The current mirror
- Differential pair + active current mirror
- Frequency analysis of an amplifier
  - Low pass filter analysis
  - Bode diagrams
  - Miller's Theorem
  - Frequency response of a Common Source Stage
  - Feedback
  - Stability issues in an amplifier
- Operational amplifier (op amp) design

Low-pass filter – time domain





REMINDER:
FOR A CAPACITOR C WE HAVE THAT

$$i(t) = C\frac{dv(t)}{dt}$$

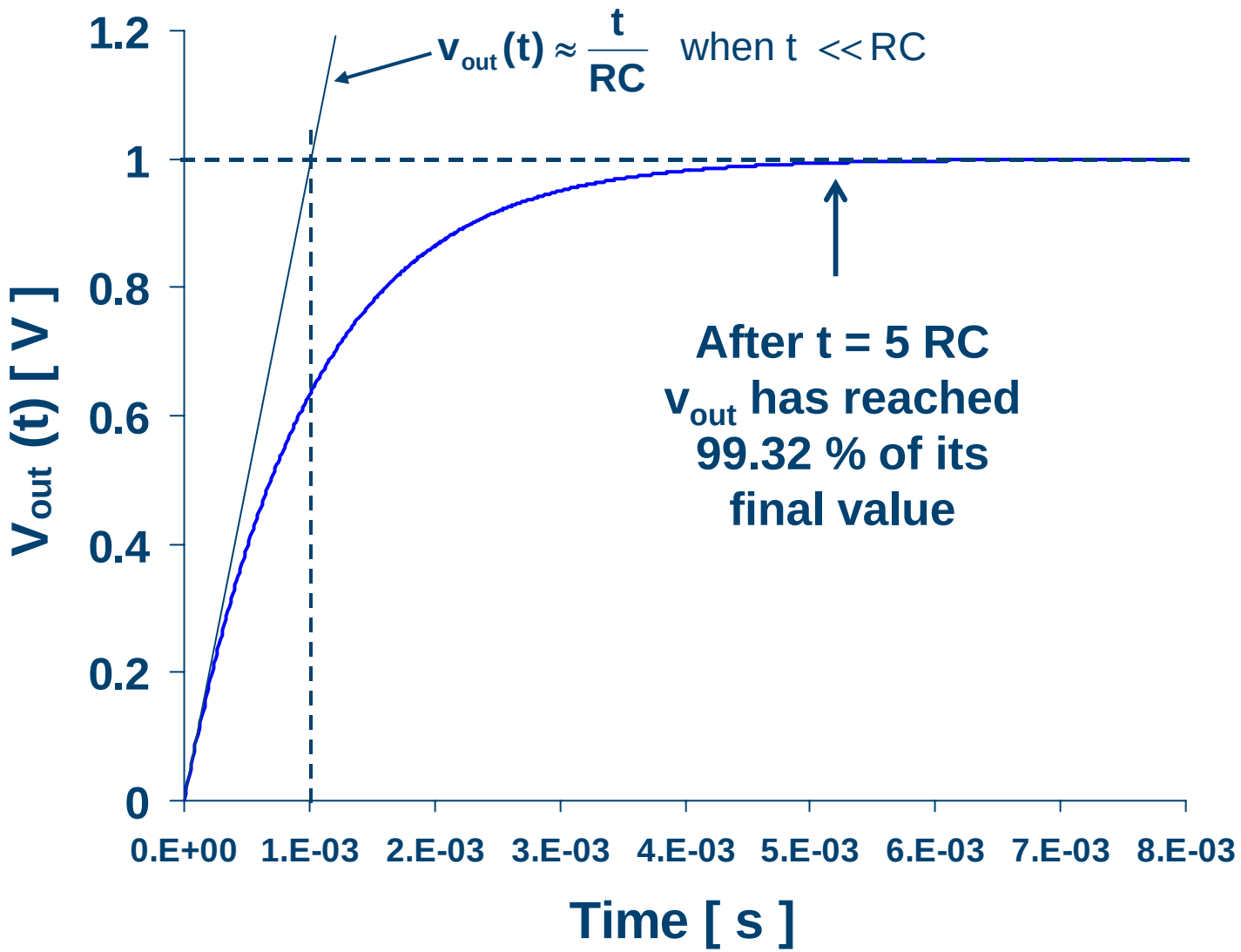
$$v_{out}(t) = 1 - R \cdot i(t) \longrightarrow v_{out}(t) = 1 - RC \cdot \frac{dv_{out}(t)}{dt} \longrightarrow RC \cdot \frac{dv_{out}(t)}{dt} + v_{out}(t) = 1$$

We can integrate the differential equation with the initial condition that the capacitor is not charged for t = 0 s (i.e. $V_{out}(0+) = 0$). We obtain:

$$v_{out}(t) = 1 - e^{-\frac{t}{RC}}$$

For more complex circuits, the equations become difficult to manage…

Low-pass filter – time domain



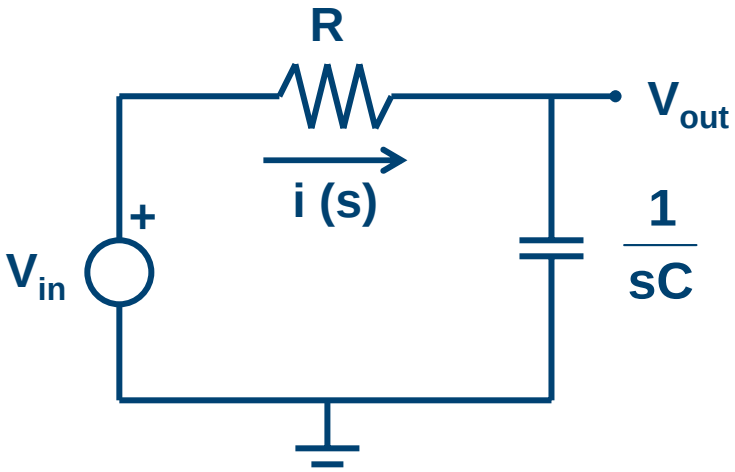
R = 1 kΩ

C = 1 μF

RC = 1 ms

Low-pass filter – frequency domain

In the *frequency* domain (s), the resistor has an impedance R and the capacitor has an impedance 1/sC. This allows calculating very easily the *transfer function* H(s) from input to output.



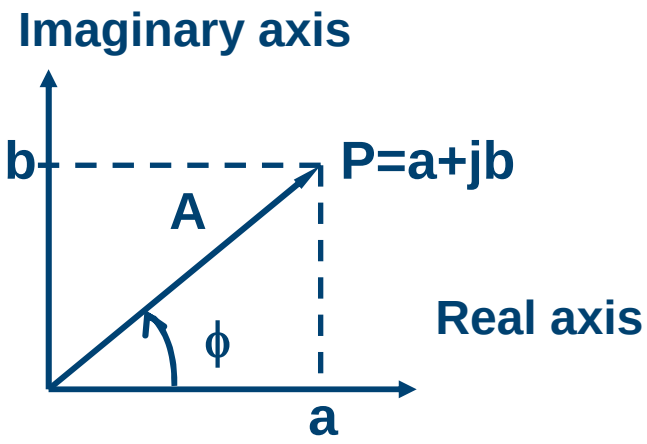
$$v_{out}(s) = \frac{v_{in}(s)}{R + \frac{1}{sC}} \cdot \frac{1}{sC} = \frac{v_{in}(s)}{1 + sRC}$$

$$H(s) = \frac{v_{in}(s)}{v_{out}(s)} = \frac{1}{1 + sRC} = \frac{1}{1 + \frac{s}{\omega_p}}$$

At this point, we can use the Laplace transformation to have the frequency representation of the input signal. This, multiplied by the transfer function, gives the output signal (as a function of the frequency). Anti-transforming by Laplace gives the output signal as a function of the time.

Complex numbers

A complex number has the form s = a + j·b, where $j = \sqrt{-1}$
We can associate a sinusoid of a given frequency to a complex number



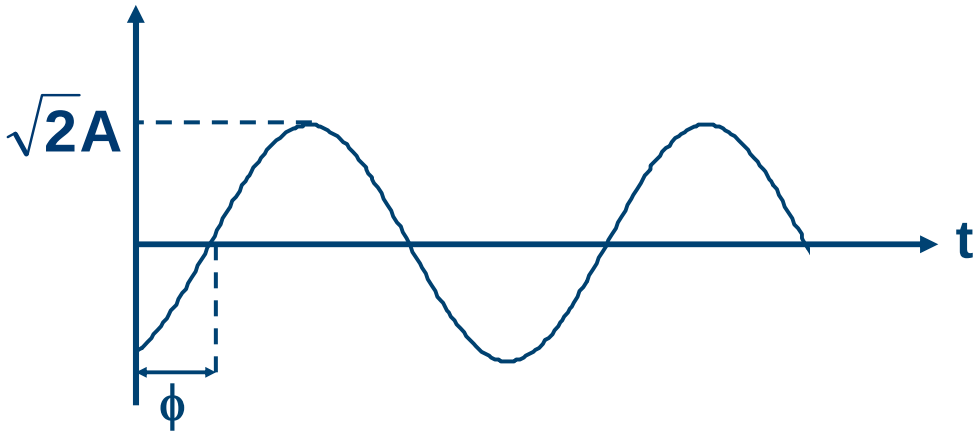
$$a = A \cdot \cos\phi$$

$$b = A \cdot \sin\phi$$

$$\phi = \arctan\frac{b}{a}$$

$$A = |s| = \sqrt{a^2 + b^2}$$

$$y(t) = \sqrt{2}A\sin(\omega t + \phi)$$



$$e^{jx} = \cos x + j \cdot \sin x$$

$$a + j \cdot b = A \cdot \cos\phi + j \cdot A \cdot \sin\phi = A \cdot e^{j\phi}$$

Fourier Transformation

A signal f(t) can be obtained superposing sinusoids and cosinusoids of different frequencies (harmonic components of the signal). We can therefore write:

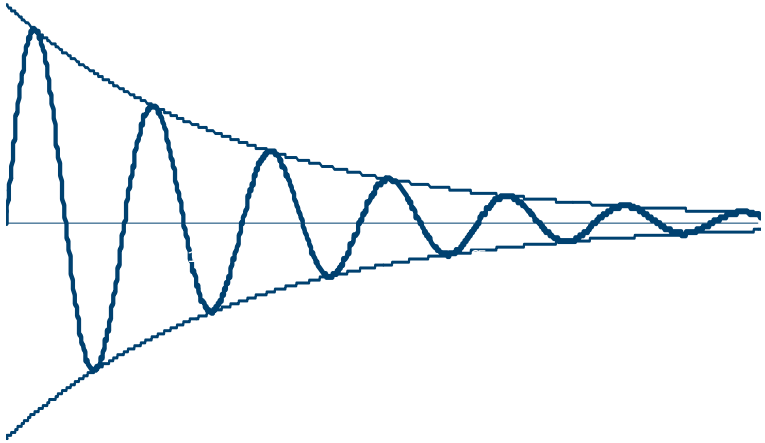
$$f(t) = \frac{1}{2\pi}\int_{-\infty}^{+\infty} f(\omega)e^{j\omega t}d\omega = \frac{1}{2\pi}\int_{-\infty}^{+\infty} \rho_\omega e^{j(\omega t+\theta_\omega)}d\omega$$

$$f(\omega) = \int_{-\infty}^{+\infty} f(t)e^{-j\omega t}dt$$

$f(\omega)$ is the Fourier Transformation of the signal f(t). It describes the harmonic composition (spectrum) of the signal.
$\rho_\omega d\omega/2\pi$ is the amplitude of the wave of frequency ω, θ_ω is the phase.
The Fourier Transformation is limited to the class of signals for which the above integral exists. Many signals useful in our field do not satisfy this requirement!

Laplace Transformation

Instead of using sinusoids of constant amplitude ($e^{-j\omega t}$) as spectral components of the signal, we can use "generalized" sinusoids ($e^{-st} = e^{-\alpha t} e^{-j\omega t}$), which have an amplitude which varies with time. This help the integral which appears in the Fourier Transformation to converge. We obtain in this way the Laplace Transformation.



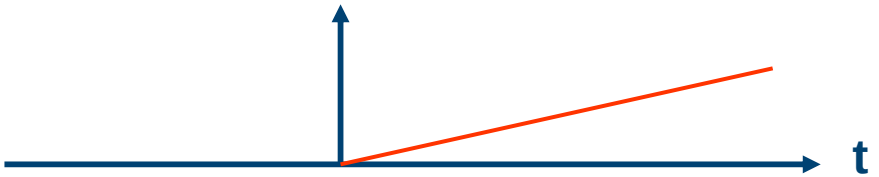
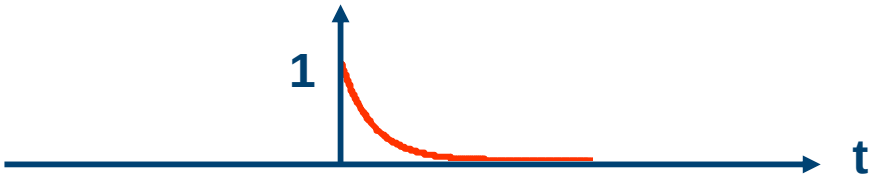
$$f(t) = \frac{1}{2\pi j}\int_{-\infty}^{+\infty} f(s)e^{st}ds$$

$$f(s) = \int_{-\infty}^{+\infty} f(t)e^{-st}dt$$

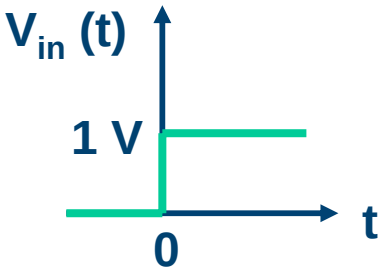
Laplace Transformation properties

Property [t]	Time Function	Transformation	Property [s]
Linearity	$c_1 \cdot f_1(t) + c_2 \cdot f_2(t)$	$c_1 \cdot f_1(s) + c_2 \cdot f_2(s)$	Linearity
Derivation	$\frac{df(t)}{dt}$	$s \cdot f(s)$	Multiplication by s
Integration	$\int f(t)dt$	$\frac{1}{s} \cdot f(s)$	Division by s
Multiplication by t	$t \cdot f(t)$	$-\frac{df(s)}{ds}$	Derivation
Translation in time	$f(t - T)$	$e^{-sT} \cdot f(s)$	Multiplication by an exponential
Convolution	$f(t) * g(t)$	$f(s) \cdot g(s)$	Multiplication

Laplace Transformation examples

f(t)	Graphical representation in the time domain	f(s)
$\delta(t)$		1
$1(t)$		$\frac{1}{s}$
$t \cdot 1(t)$		$\frac{1}{s^2}$
$e^{-t/\tau} \cdot 1(t)$		$\frac{1}{s + 1/\tau}$

Low-pass filter response



$$v_{out}(t) = H(t) * v_{in}(t)$$

$$v_{out}(t) = \int_{-\infty}^{+\infty} H(\tau) v_{in}(t-\tau) d\tau$$

$$v_{out}(t) = 1(t) \cdot \left(1 - e^{-\frac{t}{RC}}\right)$$

L

To follow the "red path" is in general much more difficult than to follow the blue one!

L^{-1}

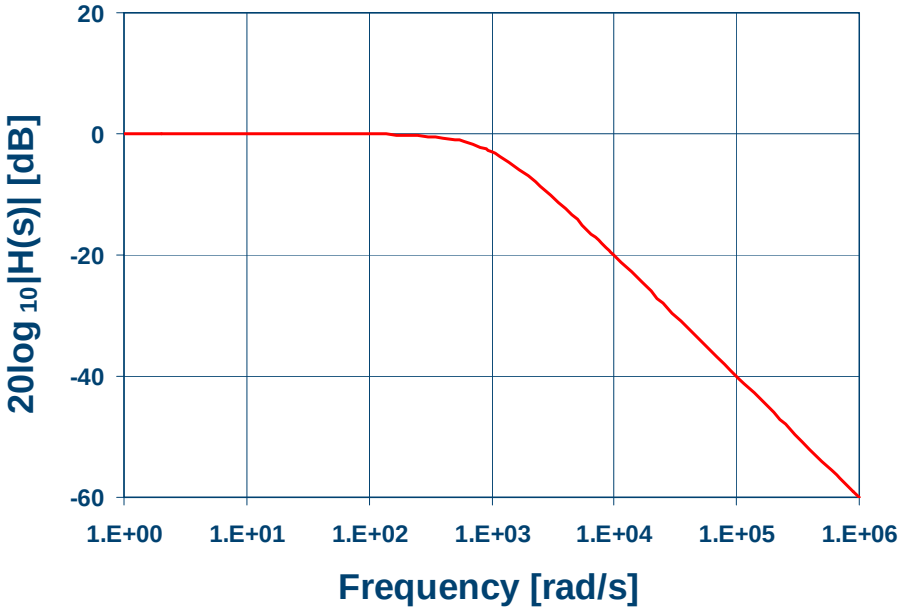
$$v_{in}(s) = \frac{1}{s} \longrightarrow \boxed{H(s) = \frac{1}{1+sRC}} \longrightarrow v_{out}(s) = \frac{1}{s} \cdot \frac{1}{1+sRC} =$$

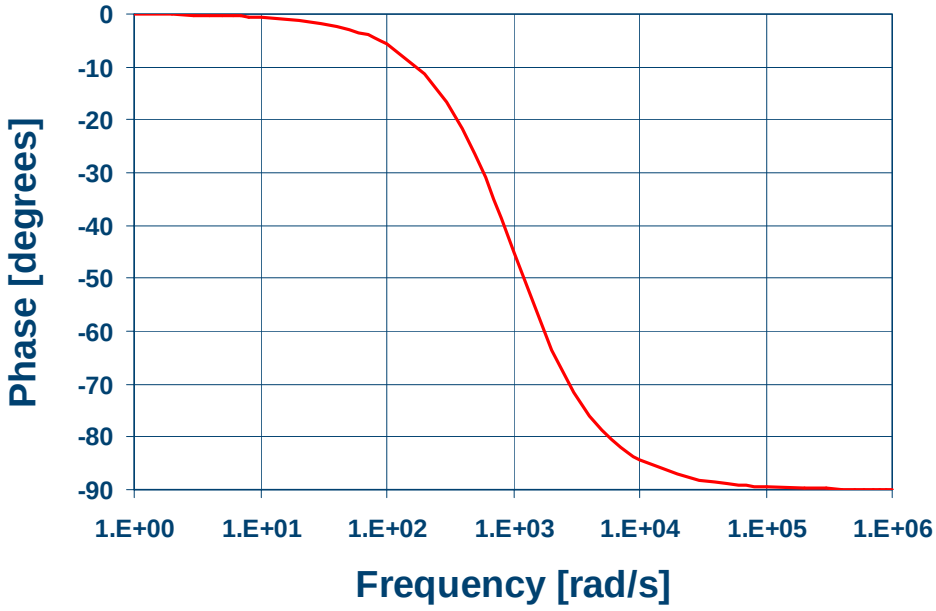
$$= \frac{1}{s} - \frac{1}{1+s/RC}$$

LOW PASS FILTER

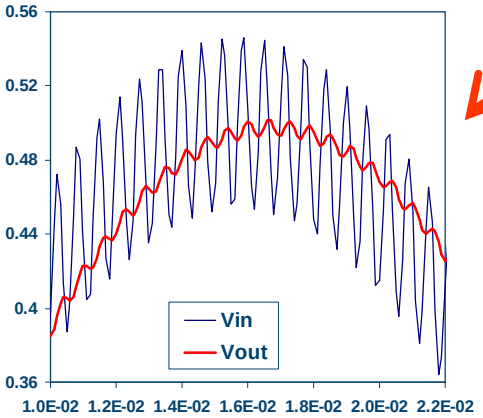
Bode diagrams

Many interesting properties of the frequency behavior of a given circuit can be obtained plotting the module and the phase of the Transfer Function as a function of the frequency. These plots are called Bode diagrams. In the general case, a transfer function is given by the ratio between two polynomials. The roots of the numerator polynomial are called zeros, the roots of the denominator polynomials are called poles. In the case of the already analyzed low-pass filter with RC = 1 ms, the Bode diagrams look like:

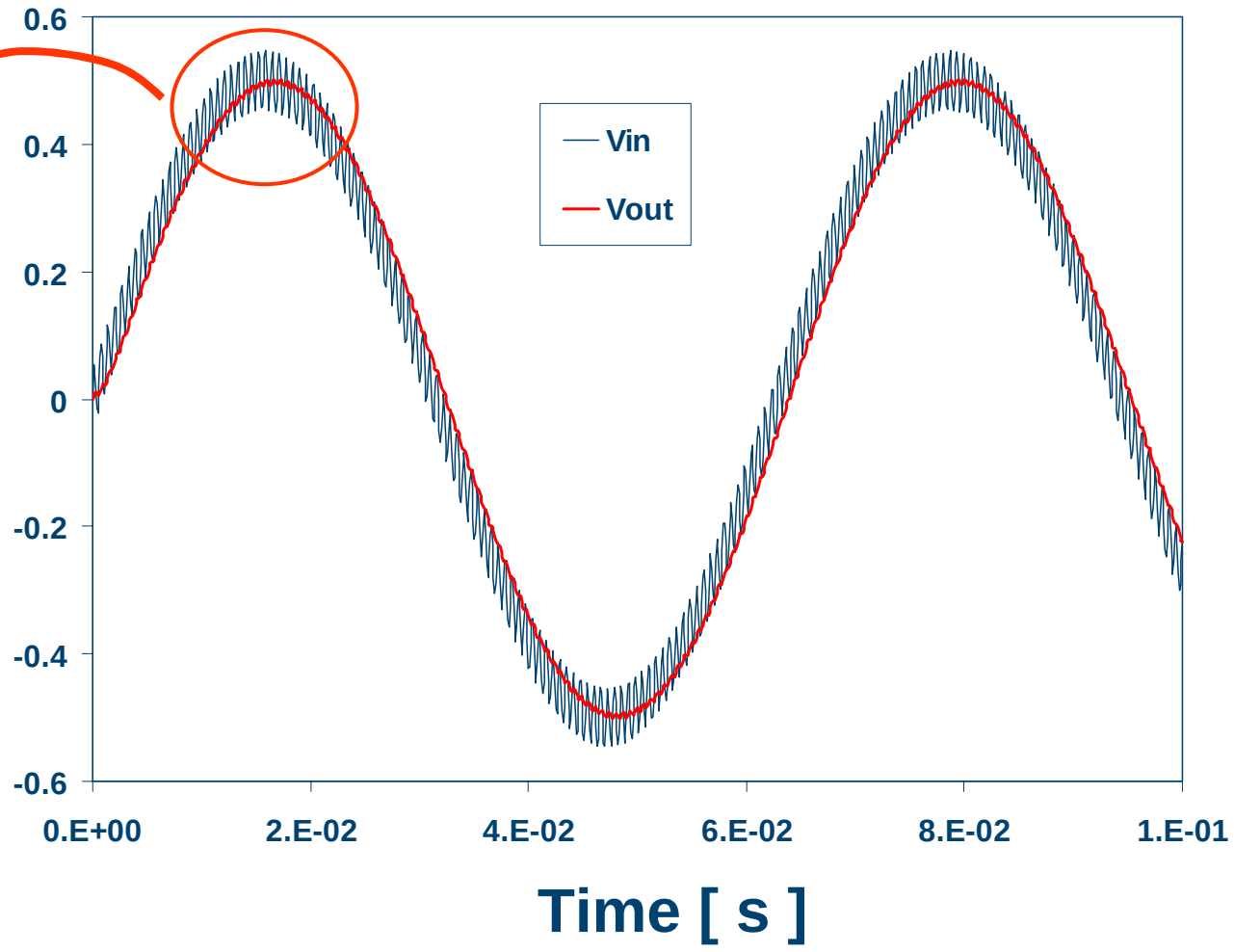




Low pass filter simulation



A the input we have the superposition of two sinusoids with frequencies 100 rad/s and 10 krad/s and peak-to-peak amplitudes 1 V and 100 mV respectively

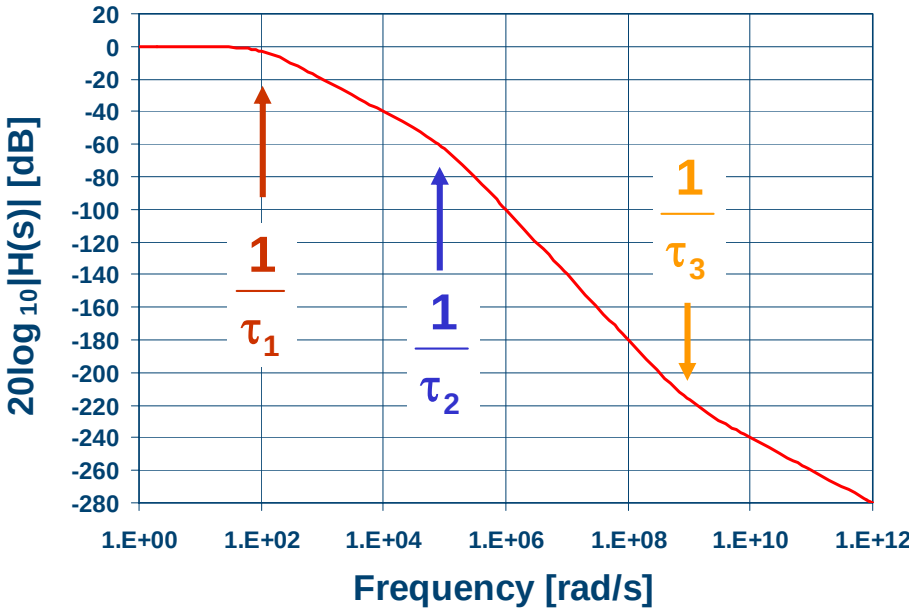


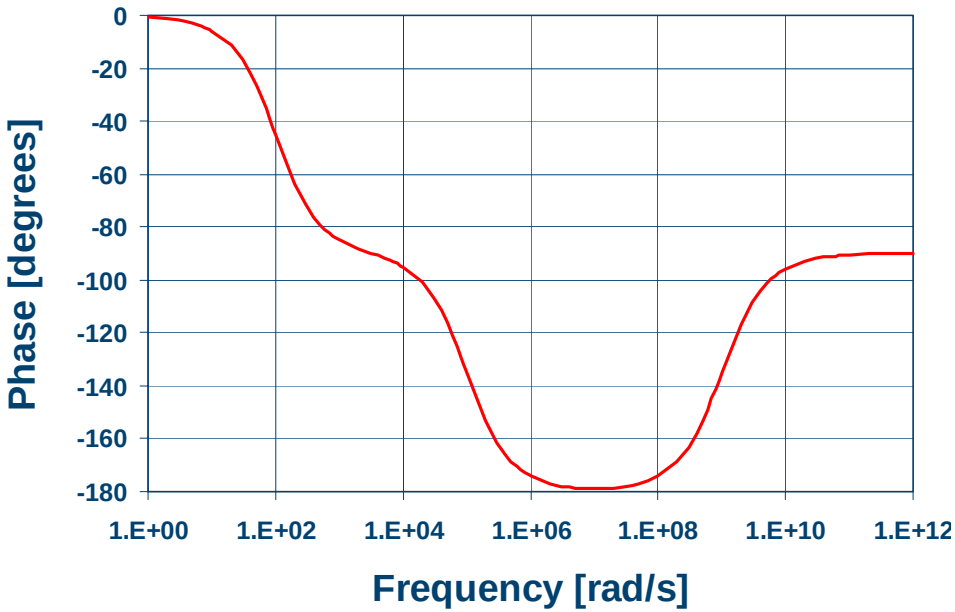
Bode diagrams

An IMMENSE advantage of the Laplace transformation is that the total transfer function of a given circuit made up by several blocks in series can be obtained as the product of the transfer functions of each single block.

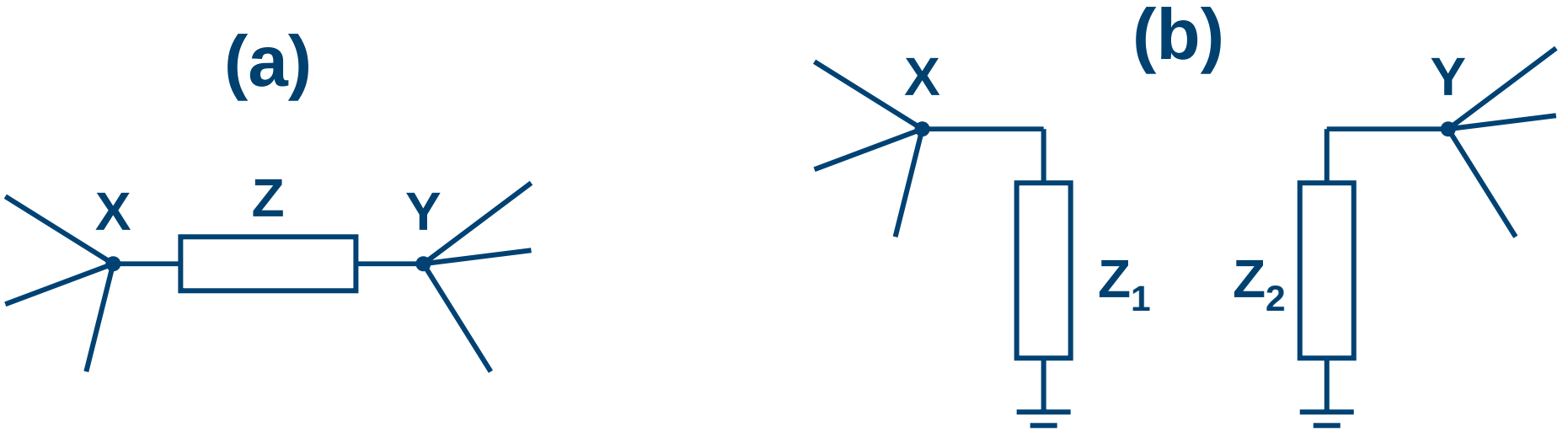
$$H_1(s) = \frac{1}{1 + s\tau_1} \quad \rightarrow \quad H_2(s) = \frac{1}{1 + s\tau_2} \quad \rightarrow \quad H_3(s) = 1 + s\tau_3$$

$$H(s) = H_1(s) \cdot H_2(s) \cdot H_3(s)$$





Miller's theorem

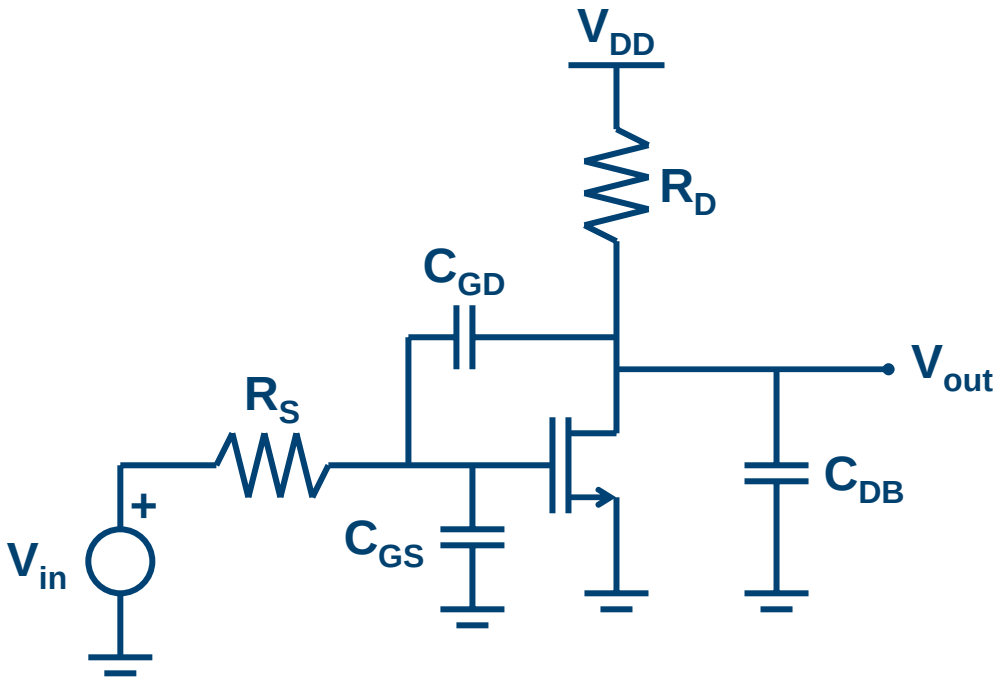


IF the circuit (a) can be converted to the circuit (b), then we can write:

$$Z_1 = \frac{Z}{1-G} \qquad Z_2 = \frac{Z}{1-\frac{1}{G}} \qquad G = \frac{V_Y}{V_X}$$

It is not trivial to find out beforehand if the conversion can be done or not. What it is interesting for us is that Miller's theorem is valid when the impedance Z is in parallel with the main signal. This will always be the case in our examples.

Frequency response of a CSS



To analyze this circuit we have two possibilities:

- **Use the equivalent circuit, mathematics and patience (and obtain the exact result)**
- **Use the Miller's theorem and make some approximations.**

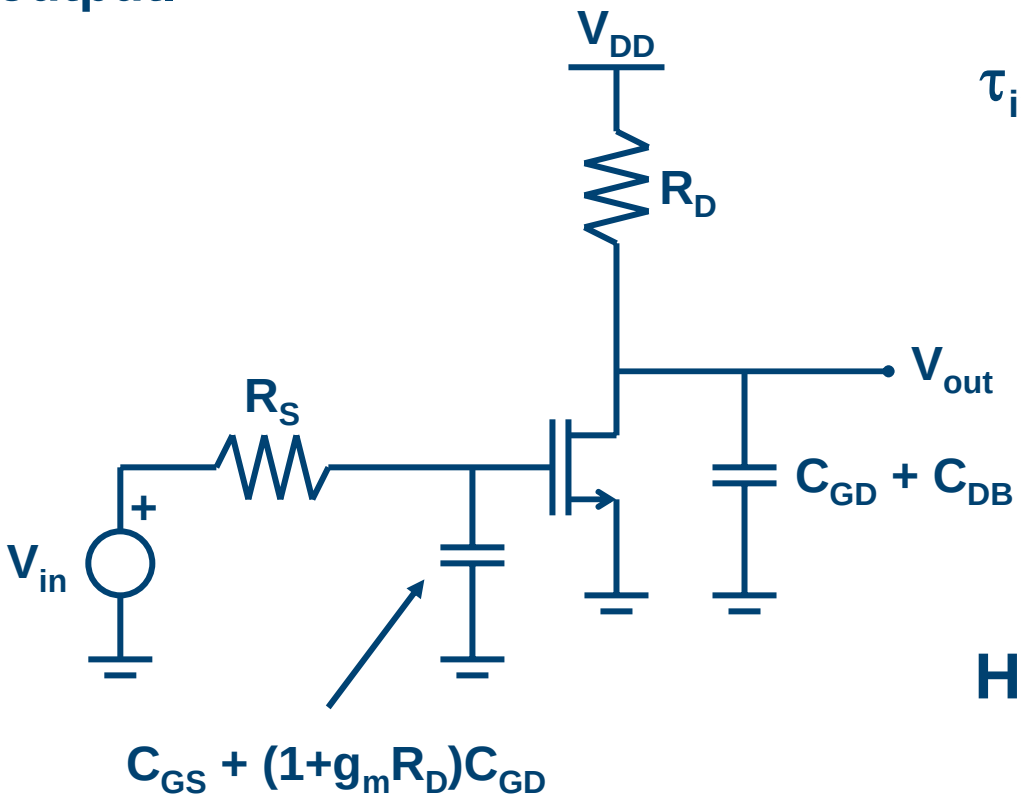
With the small signal equivalent circuit we have:

$$\frac{v_{out}(s)}{v_{in}(s)} = -g_m R_D \frac{1-\frac{C_{GD}}{g_m}s}{R_S R_D(C_{GS}C_{GD}+C_{GS}C_{DB}+C_{GD}C_{DB})s^2+[R_S(1+g_m R_D)C_{GD}+R_S C_{GS}+R_D(C_{GD}+C_{DB})]s+1}$$

And here is quite difficult to conclude something about the frequency behavior of a common-source stage!

Frequency response of a CSS

Using the Miller's theorem, C_{GD} can be split in two capacitances, one put at the input multiplied by (1-G) and one at the output multiplied by (1-1/G). It is quite easy now to see two poles, one at the input and one at the output.



$$\tau_{in} = R_S[C_{GS} + (1+g_mR_D)C_{GD}]$$

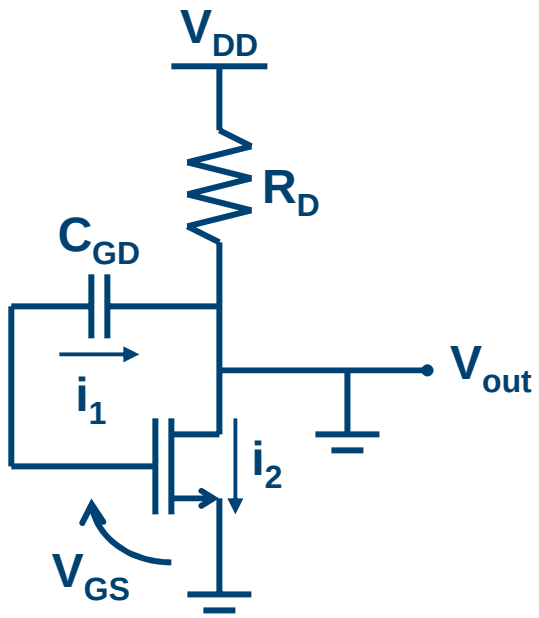
$$\tau_{out} = R_D[C_{GD} + C_{DB}]$$

$$H(s)_{approx.} = \frac{-g_mR_D}{(1+s\tau_1)(1+s\tau_2)}$$

Frequency response of a CSS

From the exact expression of the transfer function we can find the two poles (zeros of the denominator). It is possible to show that the two poles obtained with Miller's theorem are a good approximation. The main difference between the exact and the approximated H(s) is the zero!

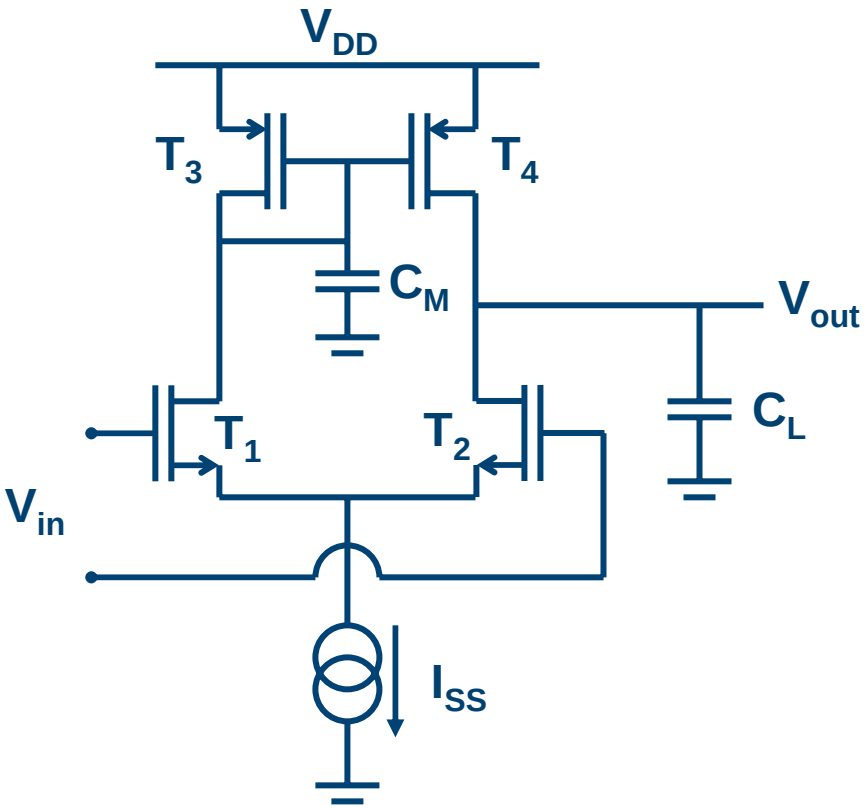
A zero in a transfer function means that at the frequency of the zero $H(s_z) = 0$, and therefore $V_{out}(s_z) = 0$ (for a given input). Moreover, the currents in the capacitor C_{GD} and in the transistor must be equal and opposite. This allows to calculate the frequency of the zero.



$$i_1 = \frac{v_{GS}}{\frac{1}{s_z C_{GD}}} \qquad i_2 = g_m v_{GS}$$

$$i_1 = i_2 \quad \text{gives} \quad s_z = \frac{g_m}{C_{GD}}$$

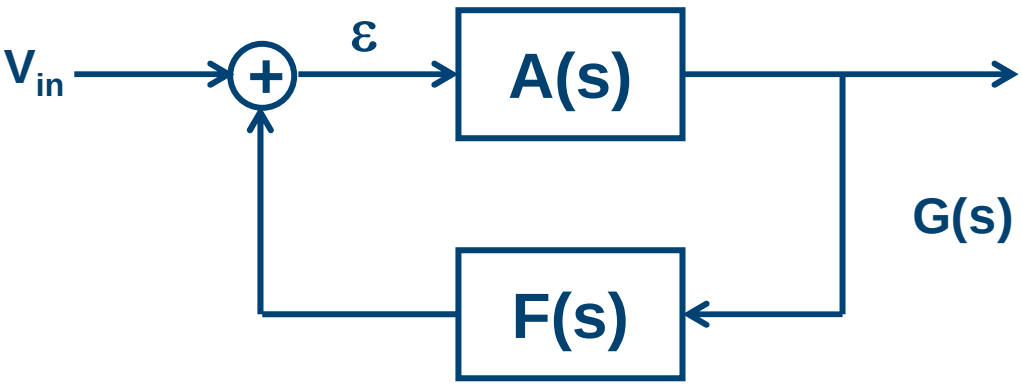
Frequency response of a DP+CM



$$\tau_{mirror} \approx \frac{C_M}{g_{m3}}$$

$$\tau_{out} \approx C_L (r_{02} \,//\, r_{04})$$

Feedback



$$G(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{A(s)}{1 - A(s)F(s)} = \frac{A(s)}{1 - G_{loop}(s)}$$

- A(s) is the open loop transfer function
- F(s) is the feedback network transfer function
- G(s) is the closed loop transfer function
- A(s)F(s) is the loop gain
- If the feedback is negative, the loop gain is negative
- For $|G_{loop}(s)| >> 1$, we have that $G(s) = -\frac{1}{F(s)}$

Properties of negative feedback

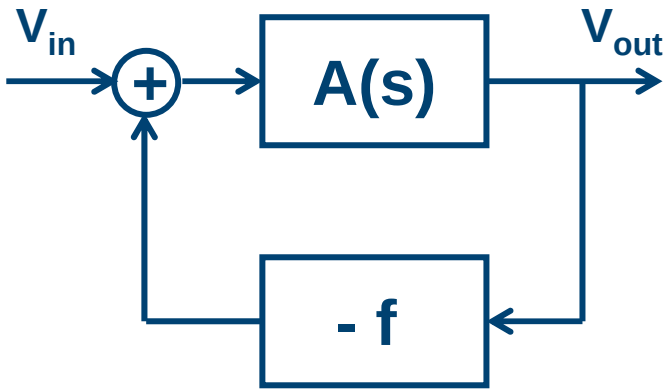
Negative feedback reduces substantially the gain of a circuit, but it improves several other characteristics:

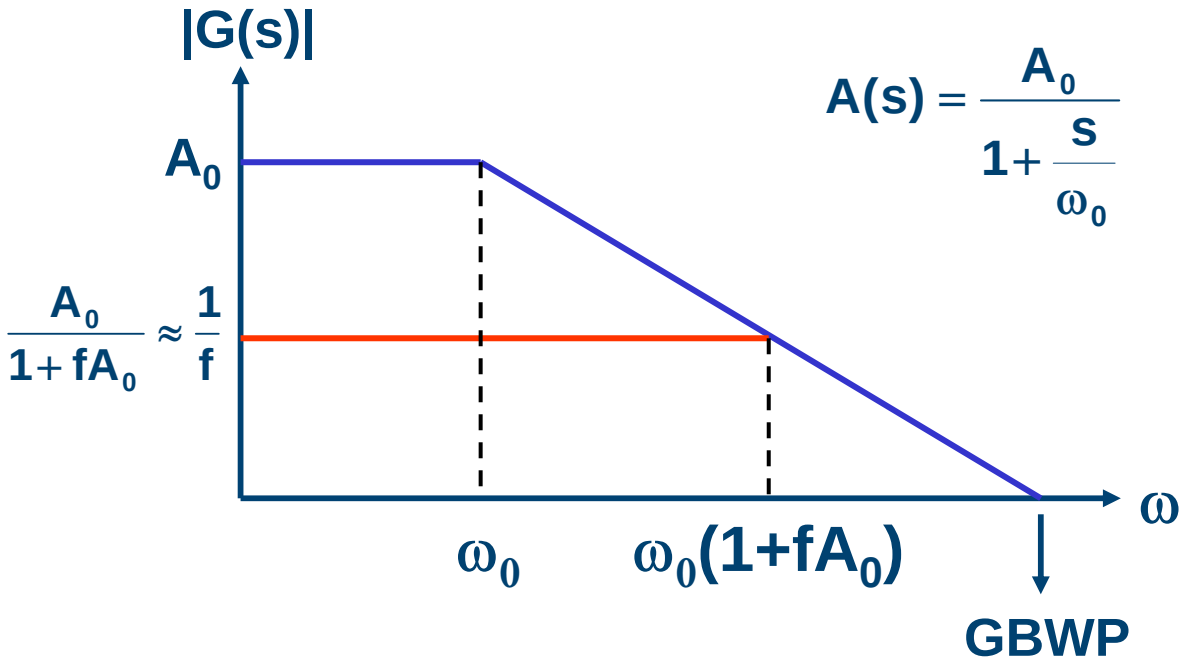
- **Gain desensitization: the open loop transfer function is generally dependent on many varying quantities, given by the active components in the circuit. Using a passive feedback network, we can reduce the dependence of the gain variation on the variations of the open loop transfer function.**

$$\frac{dG}{G} = \frac{dA}{A}\frac{1}{1 - G_{loop}}$$

- **Reduction of nonlinear distortion**
- **Reduction or increase (depending on the feedback topology) of the input and output impedances by a factor $1-G_{loop}$.**
- **Increase of the bandwidth**

Bandwidth increase with feedback

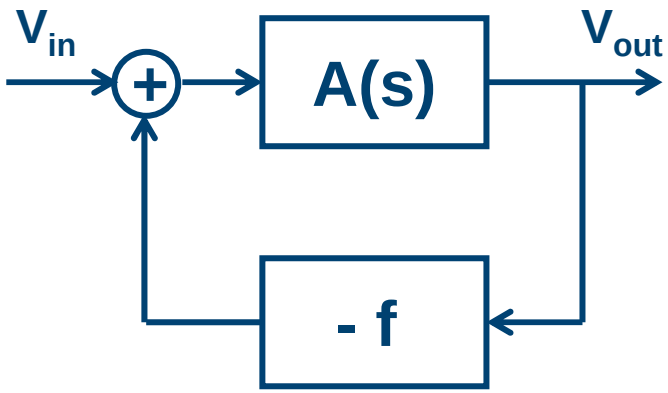




$$G(s) = \frac{A(s)}{1 + f \cdot A(s)} = \frac{\frac{A_0}{1+fA_0}}{1 + \frac{s}{(1+fA_0)\omega_0}}$$

The gain-bandwidth product does not change with feedback!

Stability Criteria



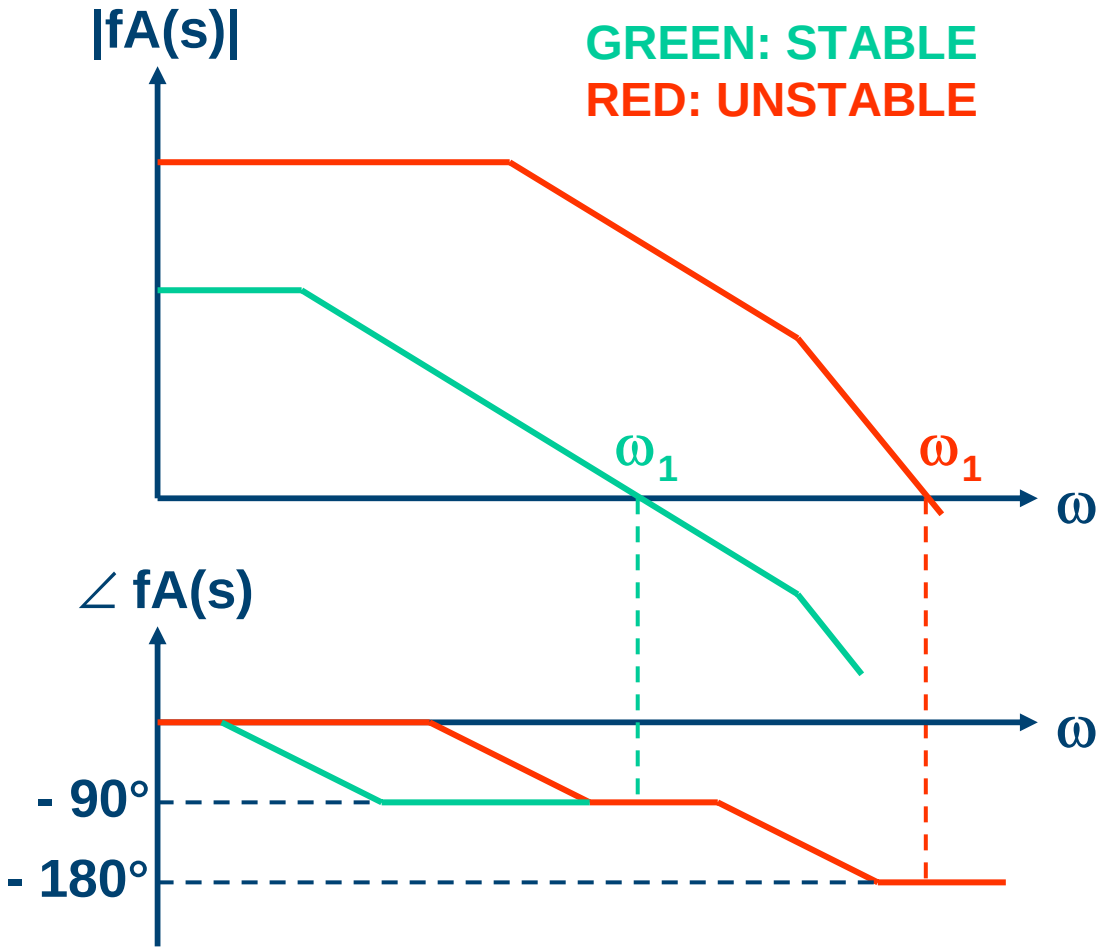
$$G(s) = \frac{A(s)}{1 + f \cdot A(s)}$$

$$1 + f \cdot A(s) = 0$$

Barkhausen's Criteria

$|fA(j\omega_1)| = 1$

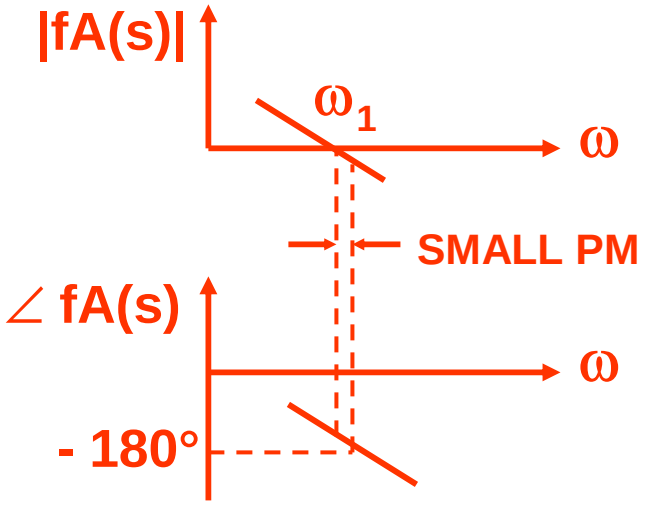
$\angle\, fA(j\omega_1) = -180°$

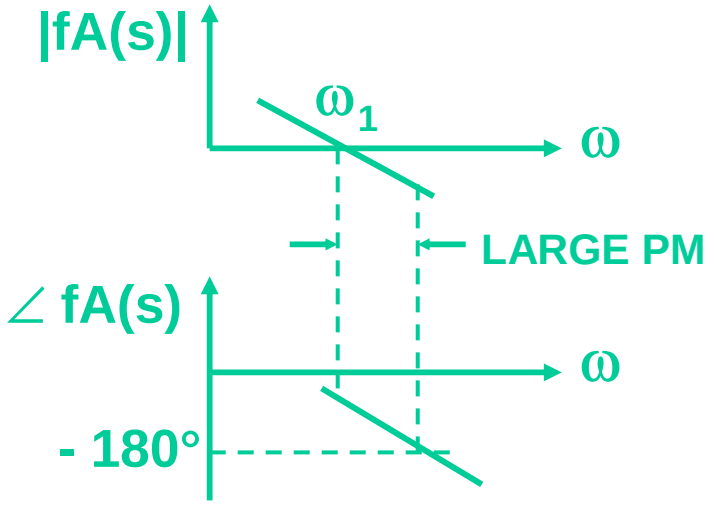


Phase Margin

We have seen that to ensure stability |fA(s)| must be smaller than 1 before ∠ fA(s) reaches - 180°. But, in fact, to avoid oscillation and ringing, we must have a bit more margin.

We define phase margin (PM) the quantity 180° + ∠ fA(ω_1), where ω_1 is the gain crossover frequency. It can be shown that, to have a stable system with no ringing (for small signals) we must have PM > 60°. If we want to have an amplifier which responds to a large input step without ringing, PM must be even higher.





Frequency Compensation

Single-pole op-amps would always be stable (the phase does not go below - 90°). But a typical op-amp circuit always contains several poles (and zeros!). These op-amps can easily be unstable, and they need therefore to be compensated. This is generally done lowering the frequency of the dominant pole.
To do so, we must add a capacitor, which is some cases can be quite large. One way of compensating a two-stage op amps is to add a capacitance across the second stage. This capacitance is multiplied by the Miller effect, and therefore it does not need to be too large!
The Miller compensation capacitor has also the nice property to move the non dominant pole to higher frequencies.
This effect is called pole splitting.

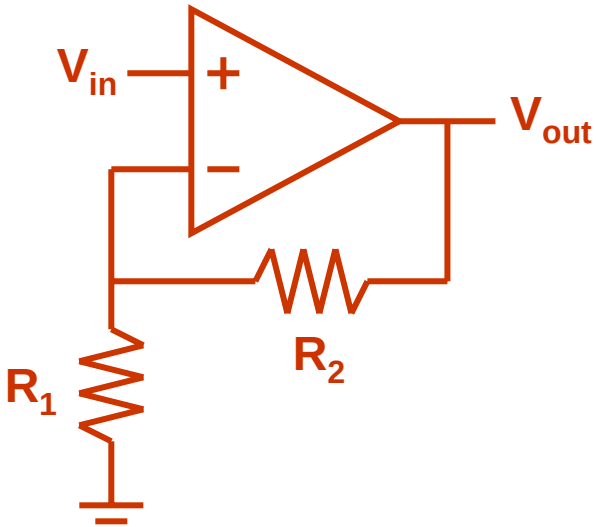
Miller compensation also introduces a zero which contributes a phase shift of - 90°. This can be a serious issue, and it must be taken into account compensating the circuit.

Outline

- Single-stage amplifiers
- The differential pair
- The current mirror
- Differential pair + active current mirror
- Frequency analysis of an amplifier
- Operational amplifier (op amp) design
  - Single-stage op amps
  - Two-stage op amps
  - One simple design example
  - Low voltage issues

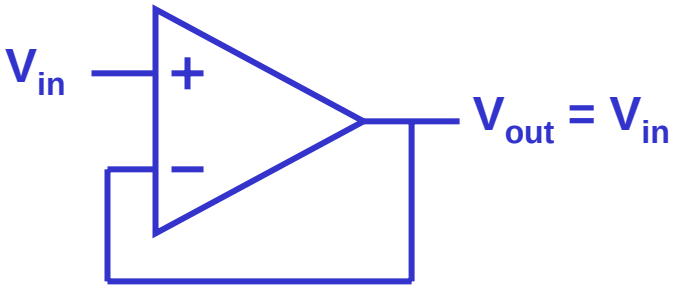
Op-amp application examples

NONINVERTING CONFIGURATION



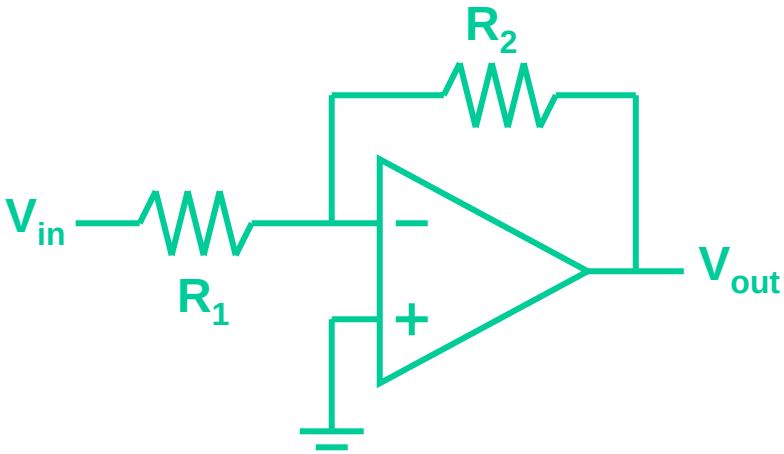
$$G = 1 + \frac{R_2}{R_1}$$

BUFFER



$$G = 1$$

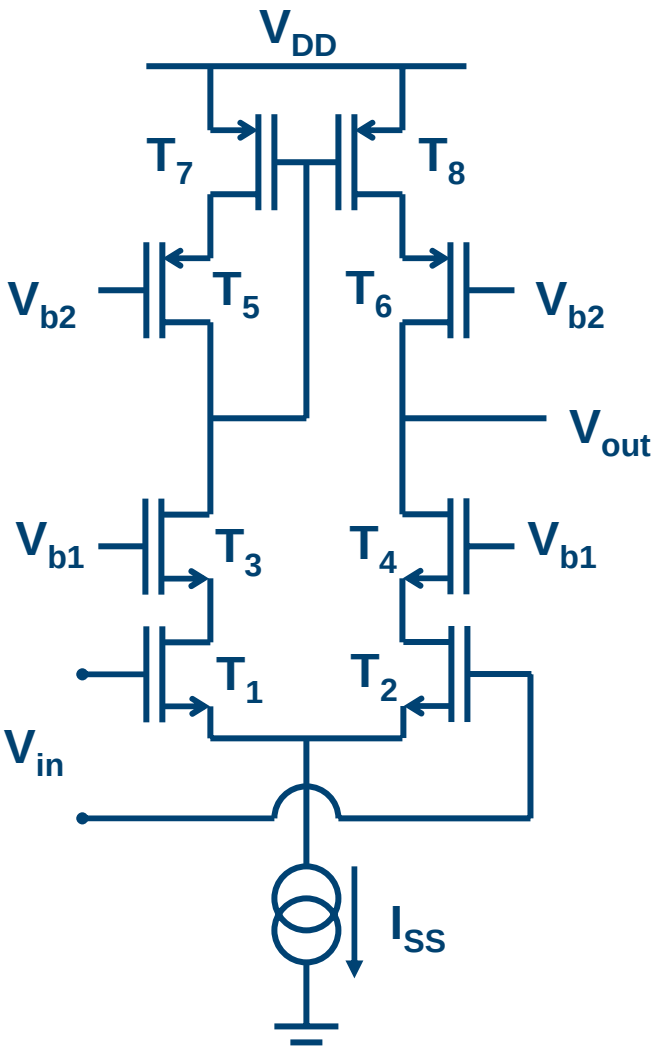
INVERTING CONFIGURATION



$$G = -\frac{R_2}{R_1}$$

The above equations are valid only if the gain of the op-amp is very high!

Single-stage Op Amp



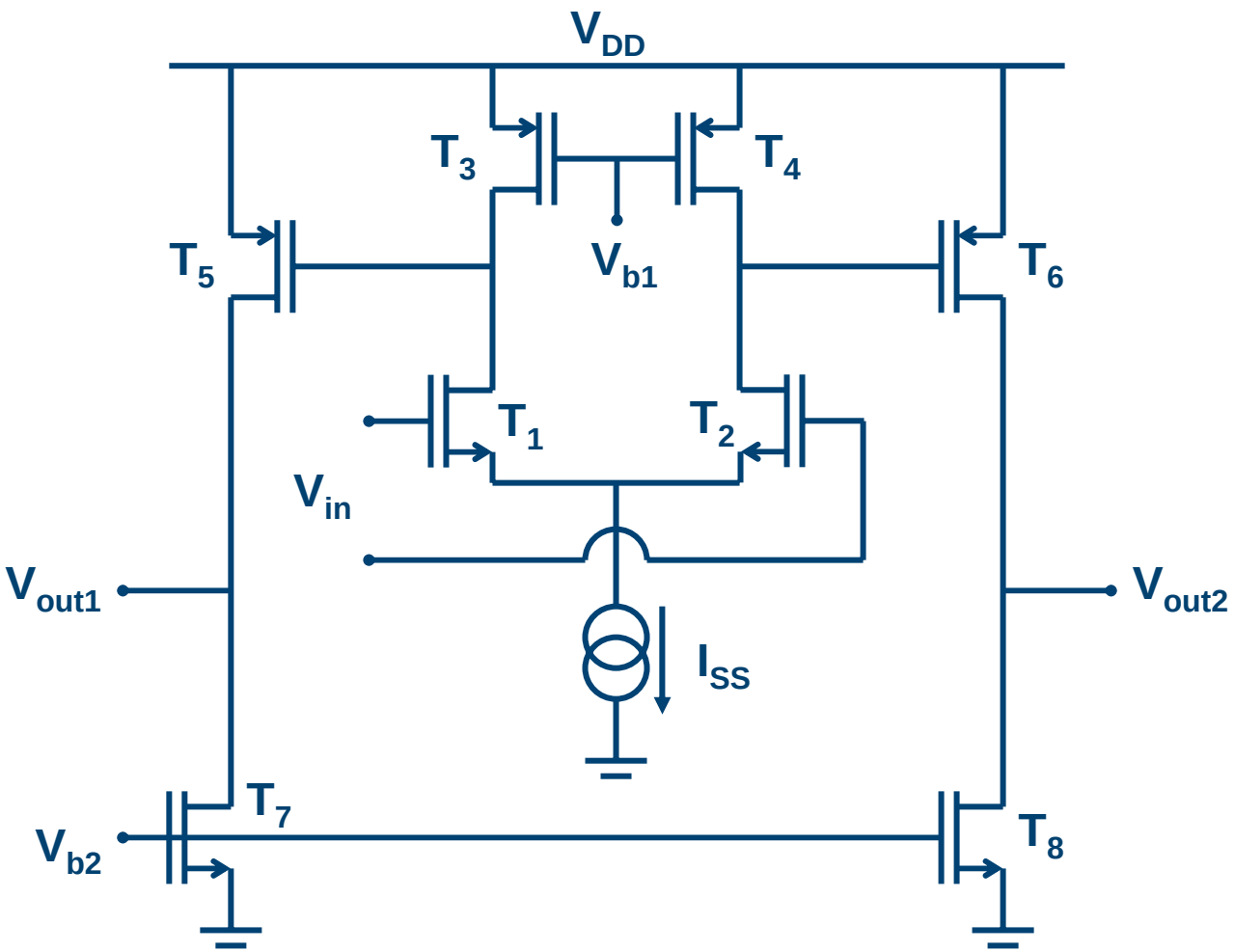
Several different solutions can be adopted to make a Single-stage amplifier. If high gains are needed, we can use, for example, cascode structures.

With single-stage amplifiers it is difficult to obtain at the same time high gain and voltage excursion, especially when other characteristics are also required, such as speed and/or precision.

Two-stage configurations in this sense are better, since they decouple the gain and voltage swing requirements.

Two-stage Op Amp

$$G = g_{m1,2}(r_{01,2} \,//\, r_{03,4}) \cdot g_{m5,6}(r_{05,6} \,//\, r_{07,8})$$

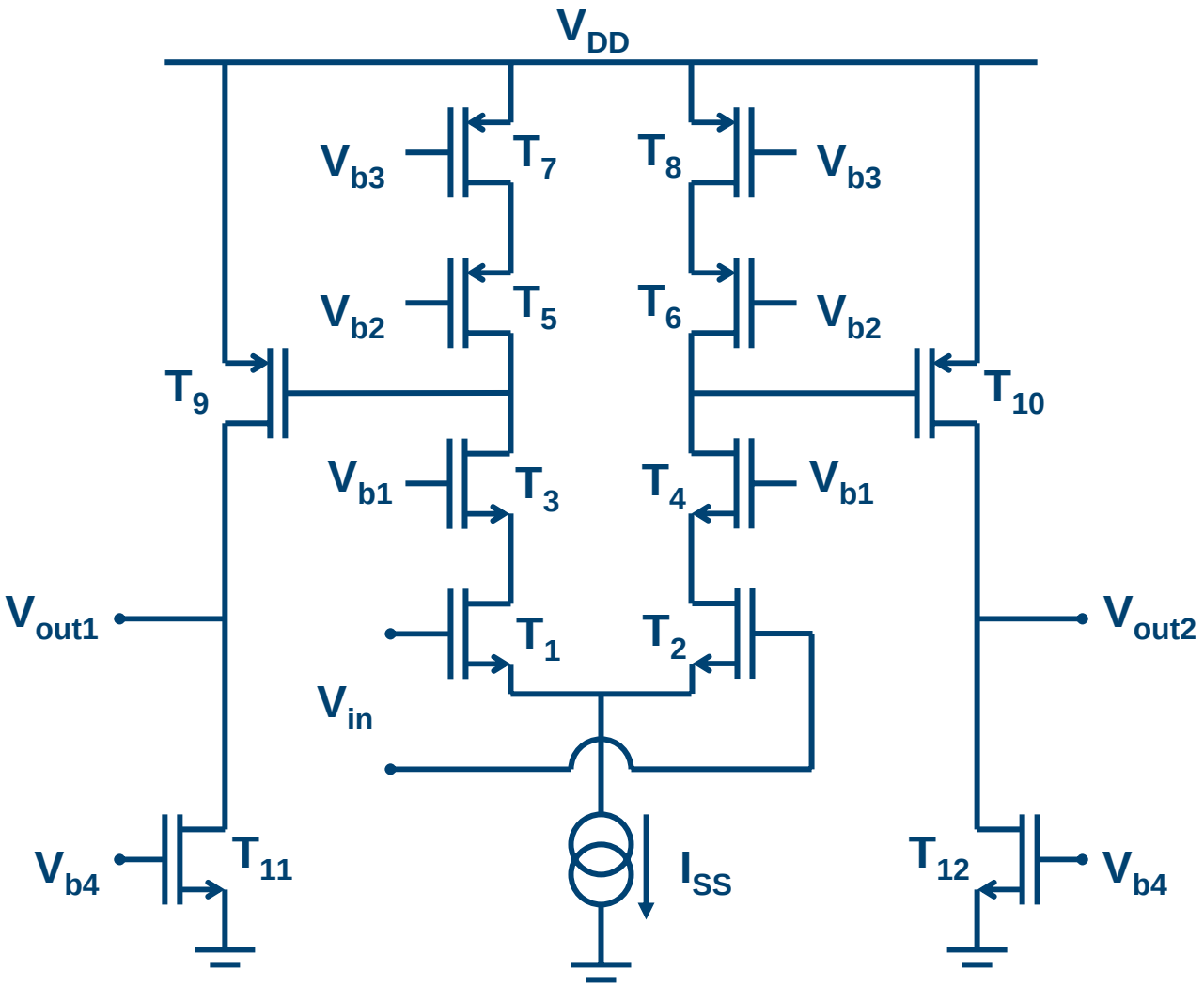


The second stage is very often a CSS, since this allows the maximum voltage swing.

The output voltage swing in this case is V_{DD} - $|2V_{DS\_SAT}|$

Two-stage Op Amp

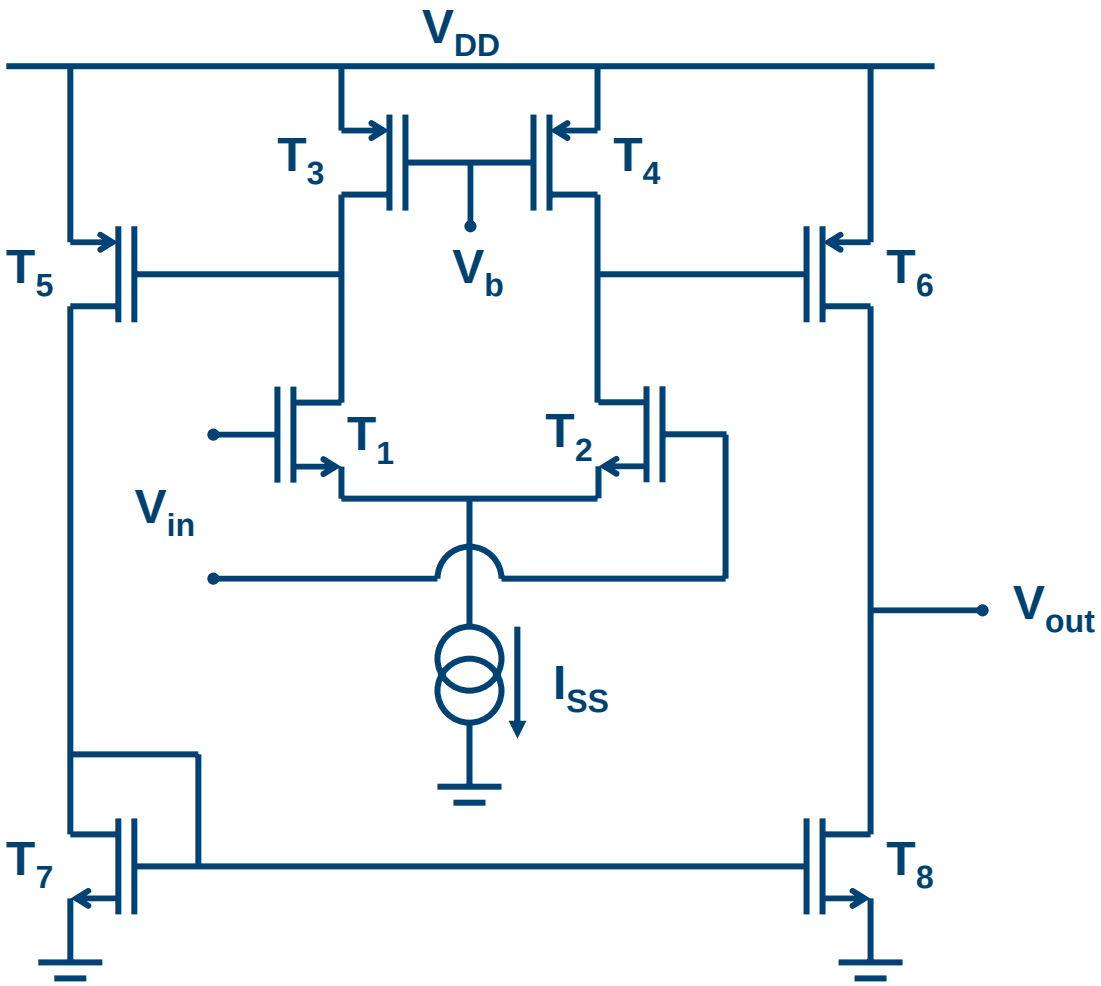
$$G = \left\{ g_{m1,2}\left[(g_{m3,4} + g_{mb3,4})r_{03,4}r_{01,2}\right] // \left[(g_{m5,6} + g_{mb5,6})r_{05,6}r_{07,8}\right] \right\} \cdot g_{m9,10}\left(r_{09,10} // r_{011,12}\right)$$



To increase the gain, we can again make use, in the first stage, of cascode structures.

Two-stage Op Amp

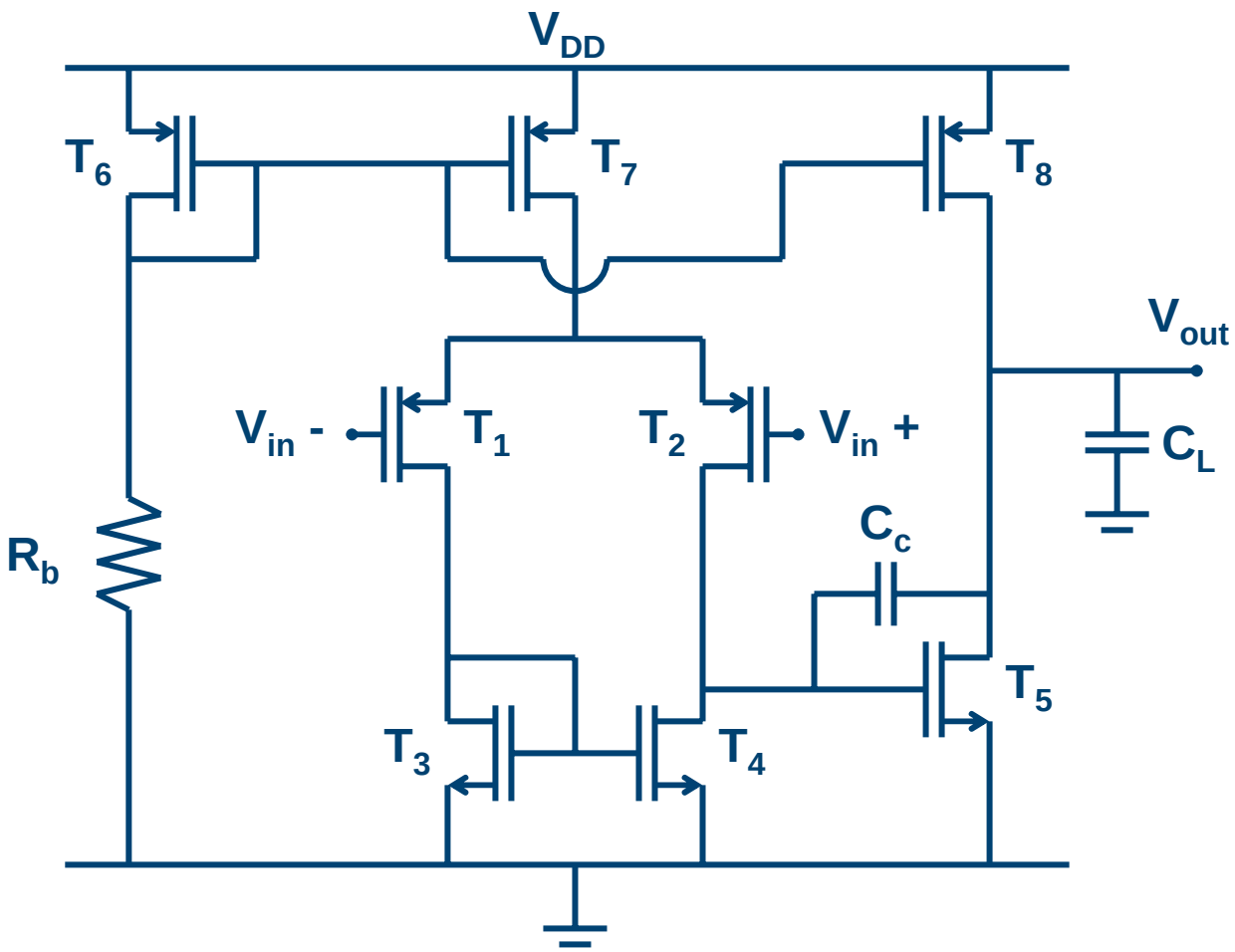
$$G = g_{m1,2}(r_{01,2} \,//\, r_{03,4}) \cdot g_{m6}(r_{06} \,//\, r_{08})$$



Two-stage op amps can also have a single-ended output. In this case, we kept the differential behavior of the first stage, and is the current mirror T7-T8 which does the differential-to-single ended conversion.

Design Example

OTA Miller – Two stage op-amp with Miller compensation



$$G = g_{m2}(r_{02} \,//\, r_{04}) \cdot g_{m5} r_{out}$$

$$G = g_{m2} r_{024} \cdot g_{m5} r_{out}$$

$$\omega_D = BW \approx \frac{1}{g_{m5} r_{out} C_c r_{024}}$$

$$\omega_{ND} \approx \frac{g_{m5}}{C_{out}}$$

$$\omega_Z \approx \frac{g_{m5}}{C_c}$$

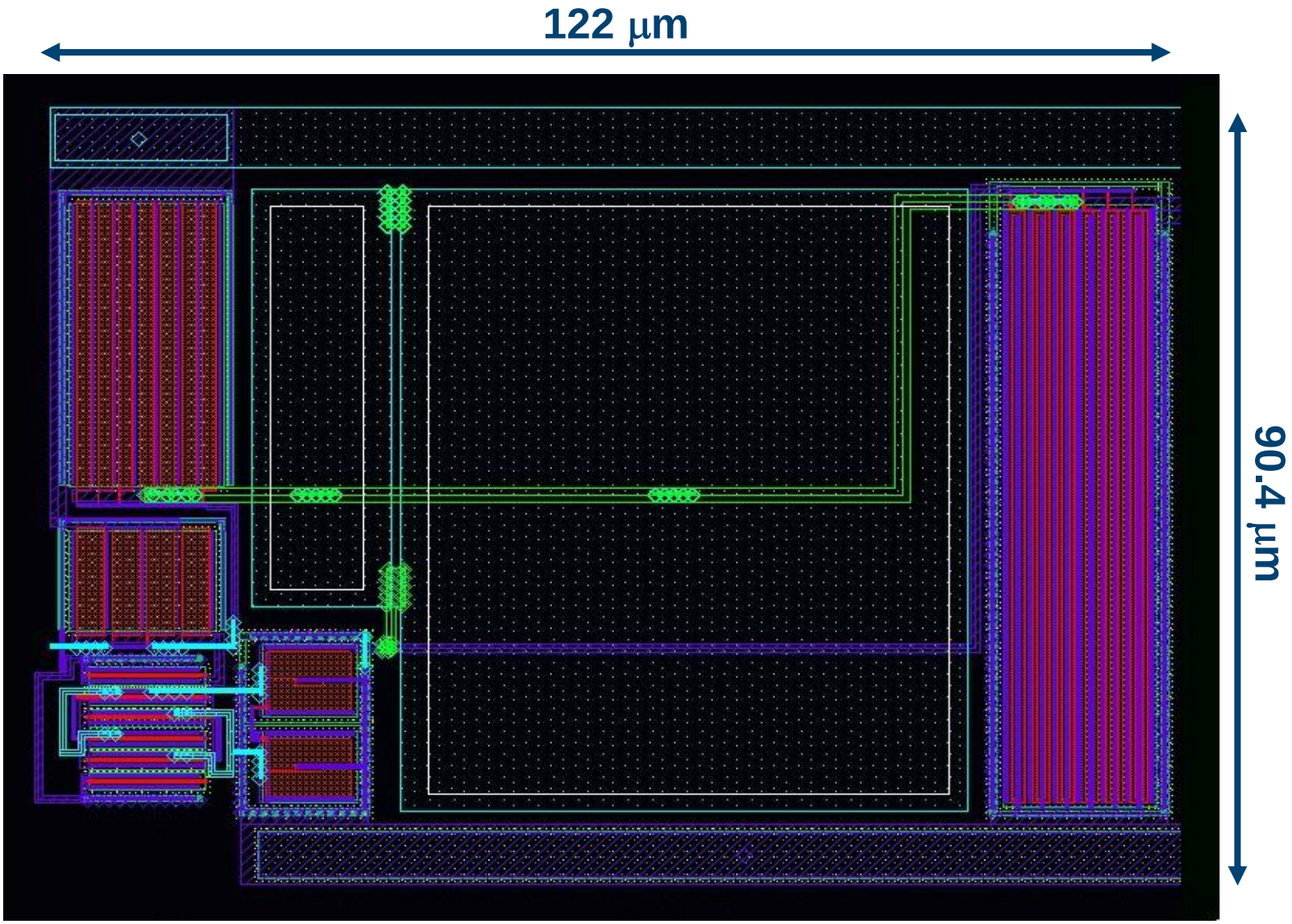
$$GBWP \approx \frac{g_{m2}}{C_c}$$

Design Example Performance

Conditions: I_{bias} = 120 μA, C_L = 20 pF

- **Power consumption = 3.5 mW**
- **Rise time = 10.5 ns**
- **Slew rate = 34 V/μs**
- **Gain Bandwidth Product = 22 MHz**
- **Phase Margin = 70°**

Design Example Layout

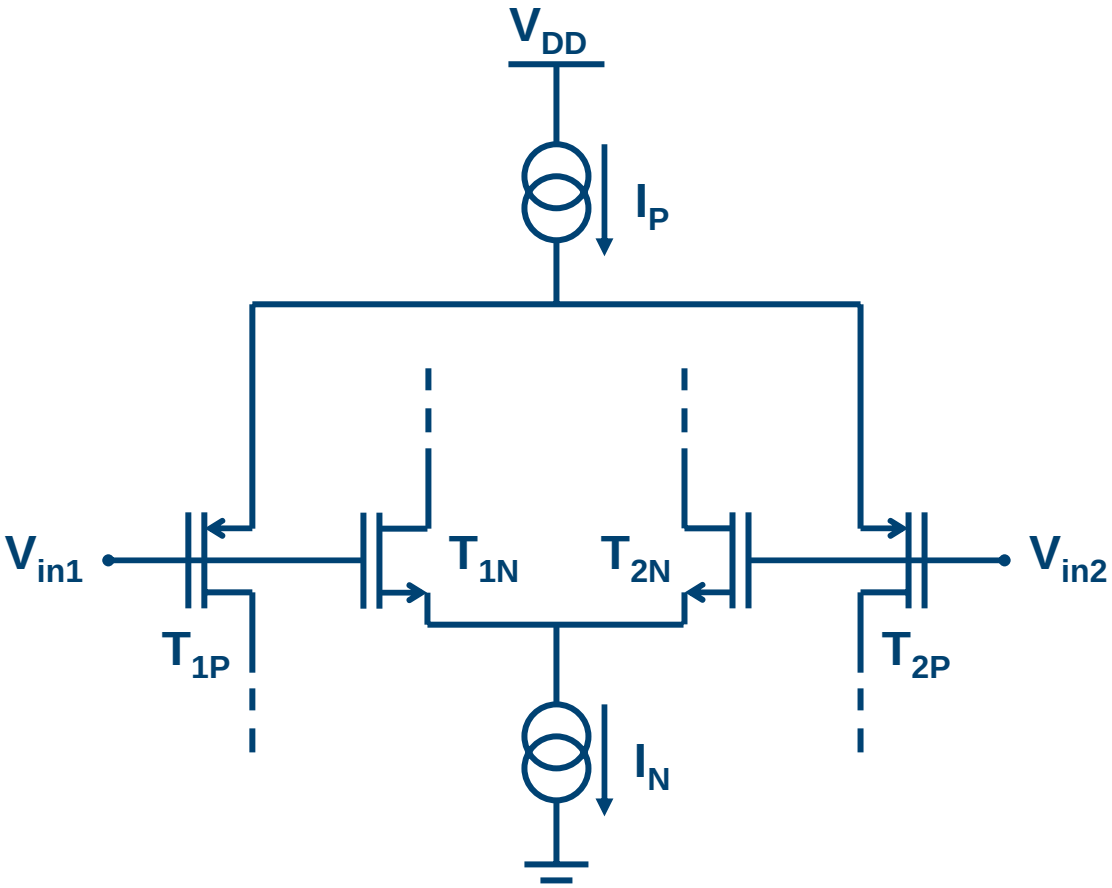


Low voltage issues

- **Use rail-to-rail input stages**
- **Low V_{DS_SAT} → Big transistors → Low speed**
- **Use low-V_T or 0-V_T transistors**
- **Use multi-gain systems to have high dynamic range**
- **Use devices in W.I. (low V_{DS_SAT} and high g_m/I_D)**
- **Use current-mode architectures**
- **Use bulk-driven MOS**
- **If very low-power is needed, this can also be obtained at the system level**

Rail-to-rail input stage

In all the solutions that we have seen up to now, the common-mode input voltage range is about V_{DD} - V_{GS} – V_{DS_SAT}. This can cause some problems, especially if we want to use the op amp as a buffer or if the power supply voltage is quite low.



This solution has the drawback of having a variable total transconductance