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Introduction to Switched Capacitor Circuits



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Outline



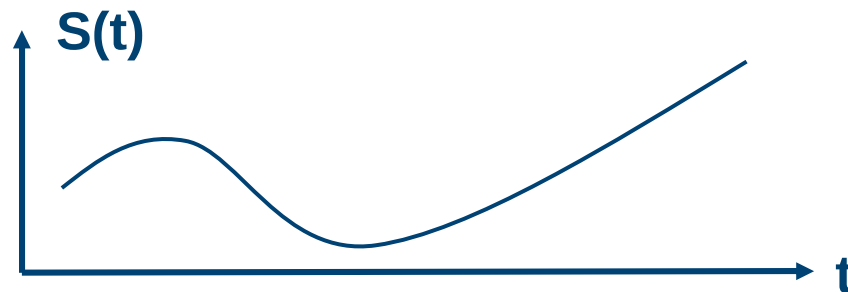
- Introduction
 - Sampled-data analog system
 - Why Switched-Capacitor Circuits?
- The basic idea behind Switched-Capacitor Circuits
- Capacitors and Switches in CMOS processes
- 2 circuit examples
- Low-voltage Switched-Capacitor Circuits design
- Conclusions



Analog and digital systems

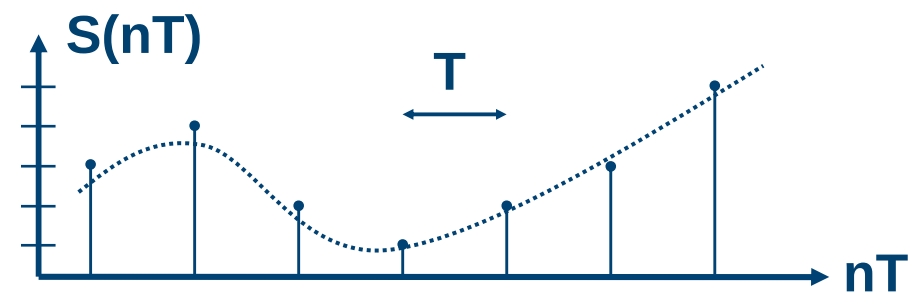
ANALOG

- The signals (represented by voltages, currents, charges) are **continuous** functions of the **continuous** time variable.
- Both dependent and independent variables are continuous.
- Examples: amplifiers, passive or active RC filters.



DIGITAL

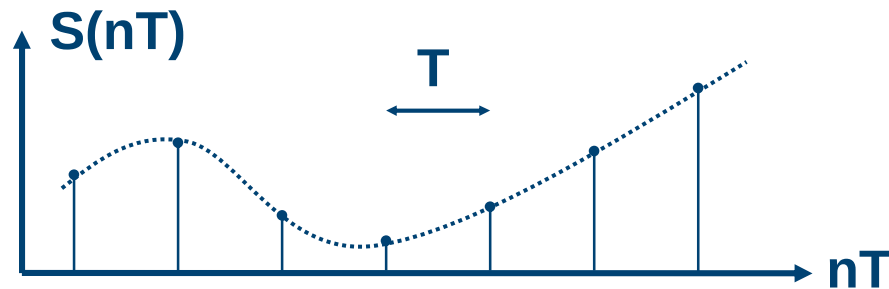
- Each signal is represented by a sequence of numbers (bits in a binary system). The signals can have only **discrete** values, taken at **discrete** time instances.
- Both dependent and indep. variables are discrete.
- Example: microprocessors.



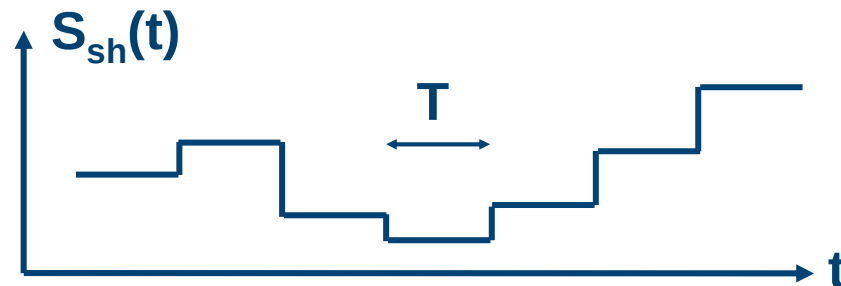


Sampled-data analog systems

As in the analog systems, the signals (dependent variable) can take any value within a given range. However, the signal amplitude is sampled only at discrete time instances, as in digital systems. Therefore, sampled-data analog systems as well as digital systems need a **clock**.



$$S(nT) = S(t)|_{t=nT}, n=0,1,2\dots$$



$$S_{sh}(t) = S(nT), nT \leq t < (n+1)T$$

Sampled and held signal



Why Switched Capacitor Circuits?

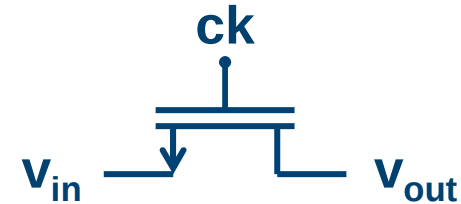
- Switched-Capacitor (**SC**) circuits were introduced, at the beginning, mainly to make integrated filters
- Historically, filters were first realized as passive circuits, with resistors (R), capacitors (C) and inductors (L)
- Since inductors (L) have several drawbacks, people started to design active-RC filters (still hybrid construction), which use operational amplifiers, resistors and capacitors.
- The next step was to make fully integrated filters, but monolithic active-RC filters are sometimes difficult to make, mainly because of area and accuracy constraints.
- This led to the invention of SC filters: we are going to see why in the following.
- Today, the switched-capacitor principle is used not only for integrated filters, but also for ADCs, DACs, programmable gain amplification and non linear circuits (multipliers, modulators,...).

R. Gregorian and G. C. Temes, *Analog MOS Integrated Circuits for Signal Processing*, J. Wiley & Sons, 1986.



Why in CMOS technology?

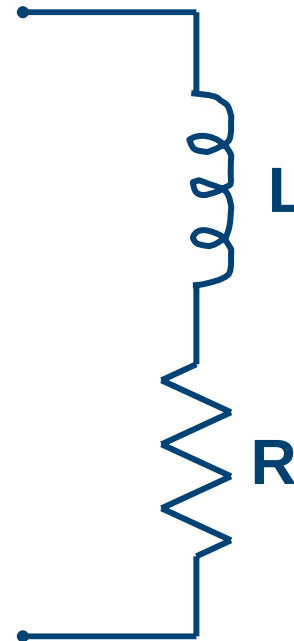
- Availability of “good” switches
 - No voltage offset
 - Low off-state leakage
 - Good on-state conductance
- Availability of high-quality capacitors
 - Precise ratios
 - Linearity
 - Low temperature coefficient
- Possibility to store a charge on a node for a long time (up to 1 second) due to the low leakage
- Possibility to sense a charge nondestructively and continuously (due to the high gate impedance)
- Switched-capacitor circuits can be built in any “digital” CMOS process, and can therefore be integrated together with complex digital functions





Inductors drawbacks

- Inductors are generally very lossy
- For low frequencies, large inductors are needed
- Inductors radiate and pick up electromagnetic disturbances
- Inductors **can not** be scaled without decreasing the quality factor



$$Q_L = \frac{\omega L}{R}$$

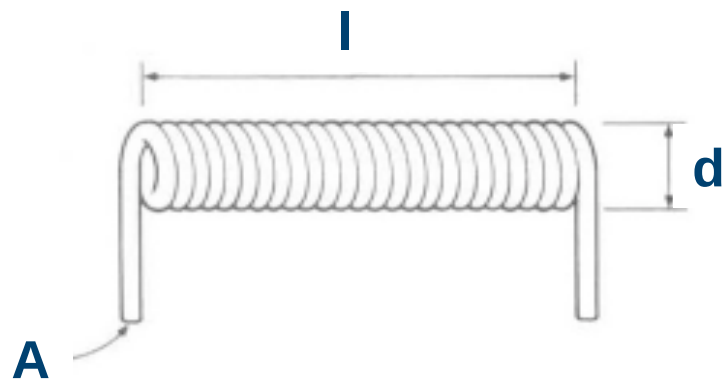
Inductors are also very difficult to integrate, and this is one of the major problems of today's RF integrated circuits

T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 1988.



Difficulties in scaling inductors

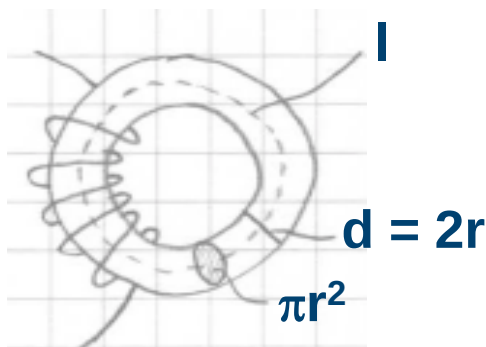
If we reduce all the dimensions by a factor $x > 1$



$$L = \mu \cdot n^2 \cdot F\left(\frac{d}{l}\right) \cdot d \longrightarrow L_x = \frac{L}{x}$$

$$R = \rho \cdot \frac{l_w}{A} = \rho \cdot \frac{n\pi d}{A} \longrightarrow R_x = R \cdot x$$

$$Q_L = \frac{\omega L}{R} \longrightarrow Q_{Lx} = \frac{\omega L_x}{R_x} = \frac{Q_L}{x^2}$$



$$L = \mu \cdot n^2 \cdot \frac{\pi r^2}{l}$$

G. C. Temes and J. W. LaPatra, *Introduction to Circuit Synthesis and Design*, McGraw-Hill, 1977.



Integrated Active-RC filters

- There are several difficulties when making monolithic active-RC filters:
 - Limited capacitance per unit area (**around 1 fF/ μm^2**)
 - Limited resistance per unit area (**50-200 $\Omega/\text{sq.}$**)
 - Poor resistance and capacitance absolute value accuracy (**10-20 %**)
- For example, if we need an RC of 10^{-4} (voice band application), we would need a 10 pF capacitor (**100 μm by 100 μm**) and a 10 M Ω resistor (**1000 μm by 1000 μm if each square is 3 μm by 3 μm**).
- The error on the RC time constant will be $> 20 \%$, since the errors in R and C are not correlated.
- Temperature and aging coefficients of capacitors and resistors do not track. This increases even more the already poorly controlled RC constant spread.
- **For many applications the accuracy that can be obtained with integrated active RC filters is not good enough.**





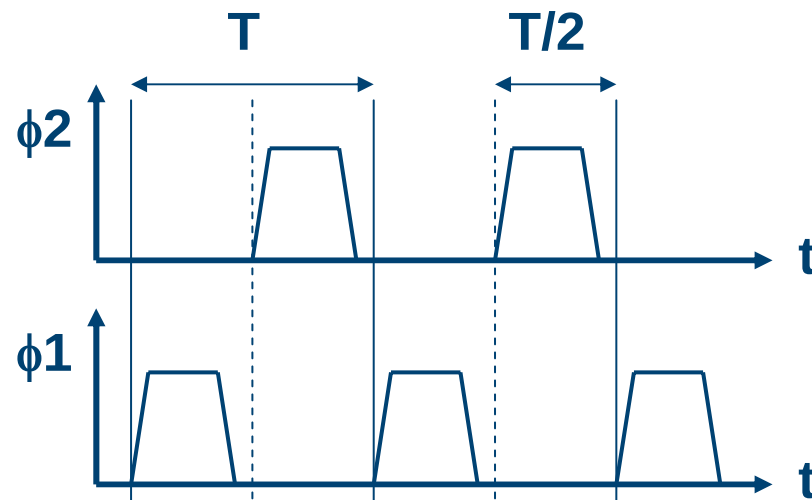
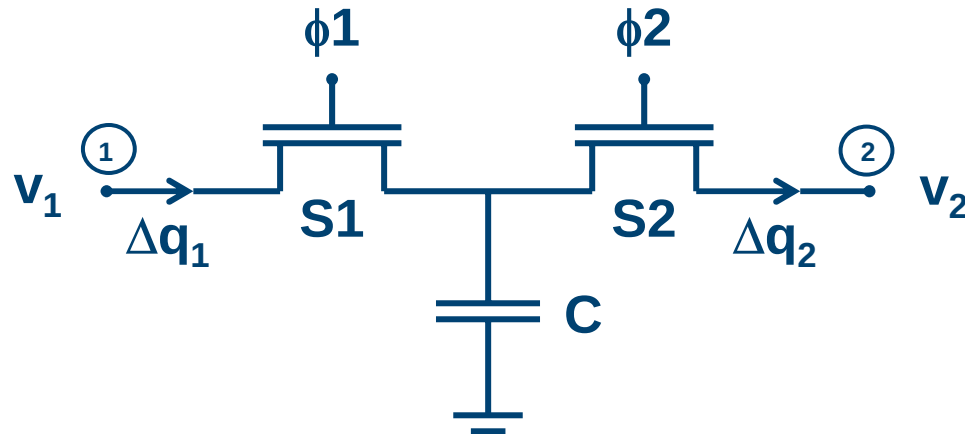
Outline



- Introduction
- The basic idea behind Switched-Capacitor Circuits
 - How to replace a resistor with a capacitor and two switches
 - The origin of this idea (and of its application)
- Capacitors and Switches in CMOS processes
- 2 circuit examples
- Low-voltage Switched-Capacitor Circuits design
- Conclusions



Resistor emulation



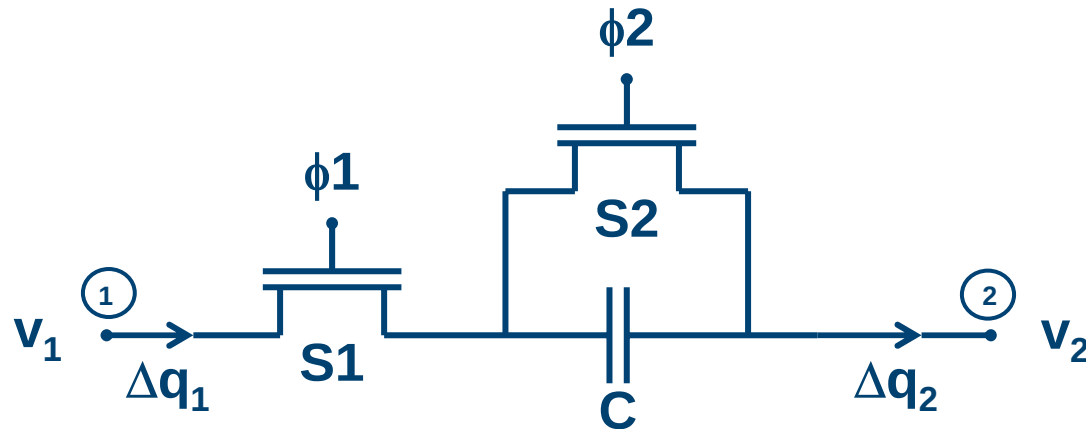
- v_1 and v_2 are supposed to be slow varying signals (compared to T)
- Each clock cycle T , a charge Δq goes from 1 to 2, where
$$\Delta q = \Delta q_1 = \Delta q_2 = C(v_1 - v_2)$$

- The average current flowing from 1 to 2 is
$$i = (v_1 - v_2) \cdot \frac{C}{T}$$
- C , $S1$ and $S2$ emulate therefore a resistor

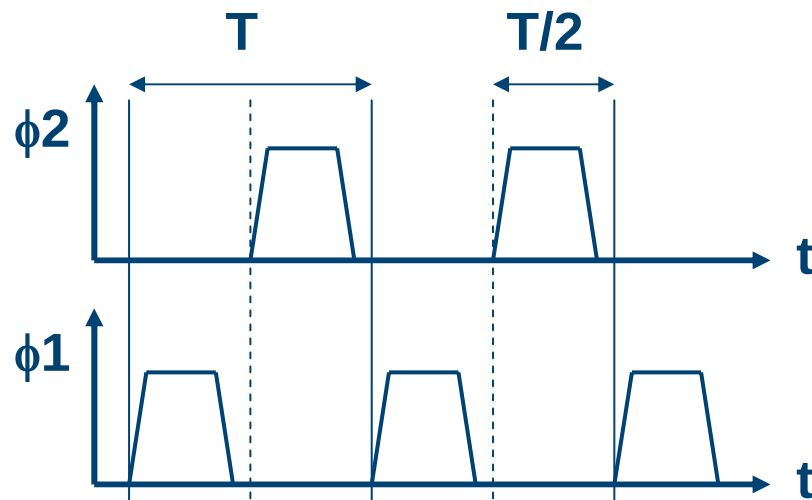
$$R = \frac{T}{C}$$



Resistor emulation (2)



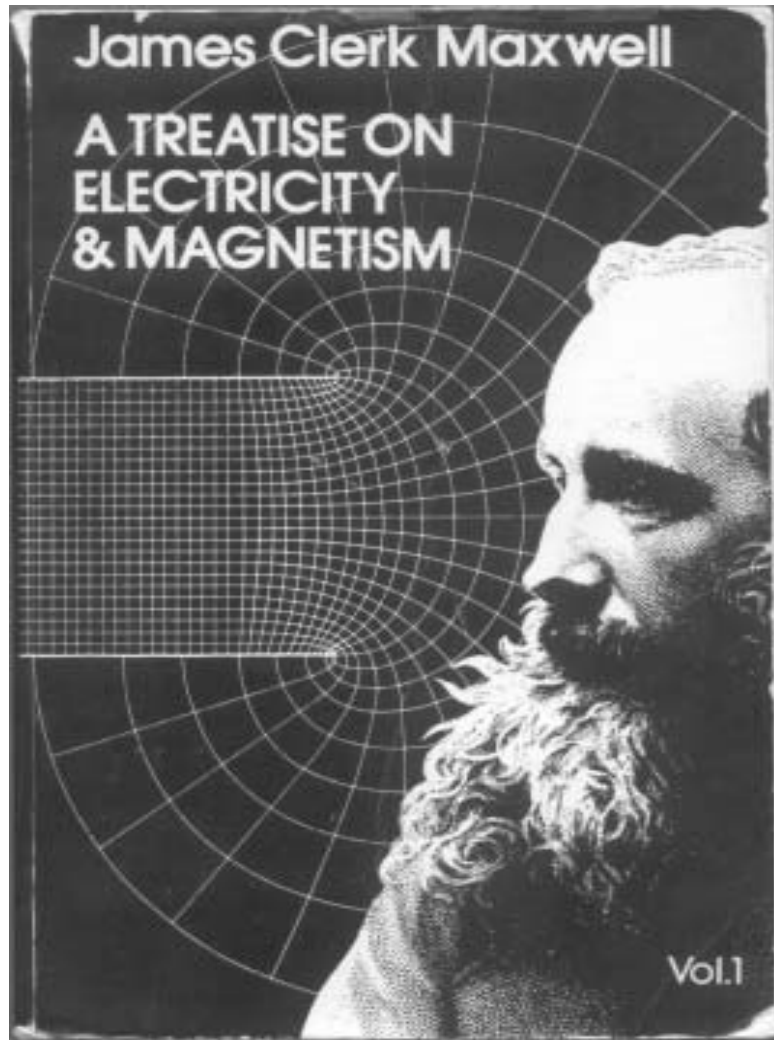
$$R = \frac{T}{C}$$



$$R_1 C_2 = \frac{C_2}{C_1} \cdot T = \frac{C_2}{C_1} \cdot \frac{1}{f_c}$$



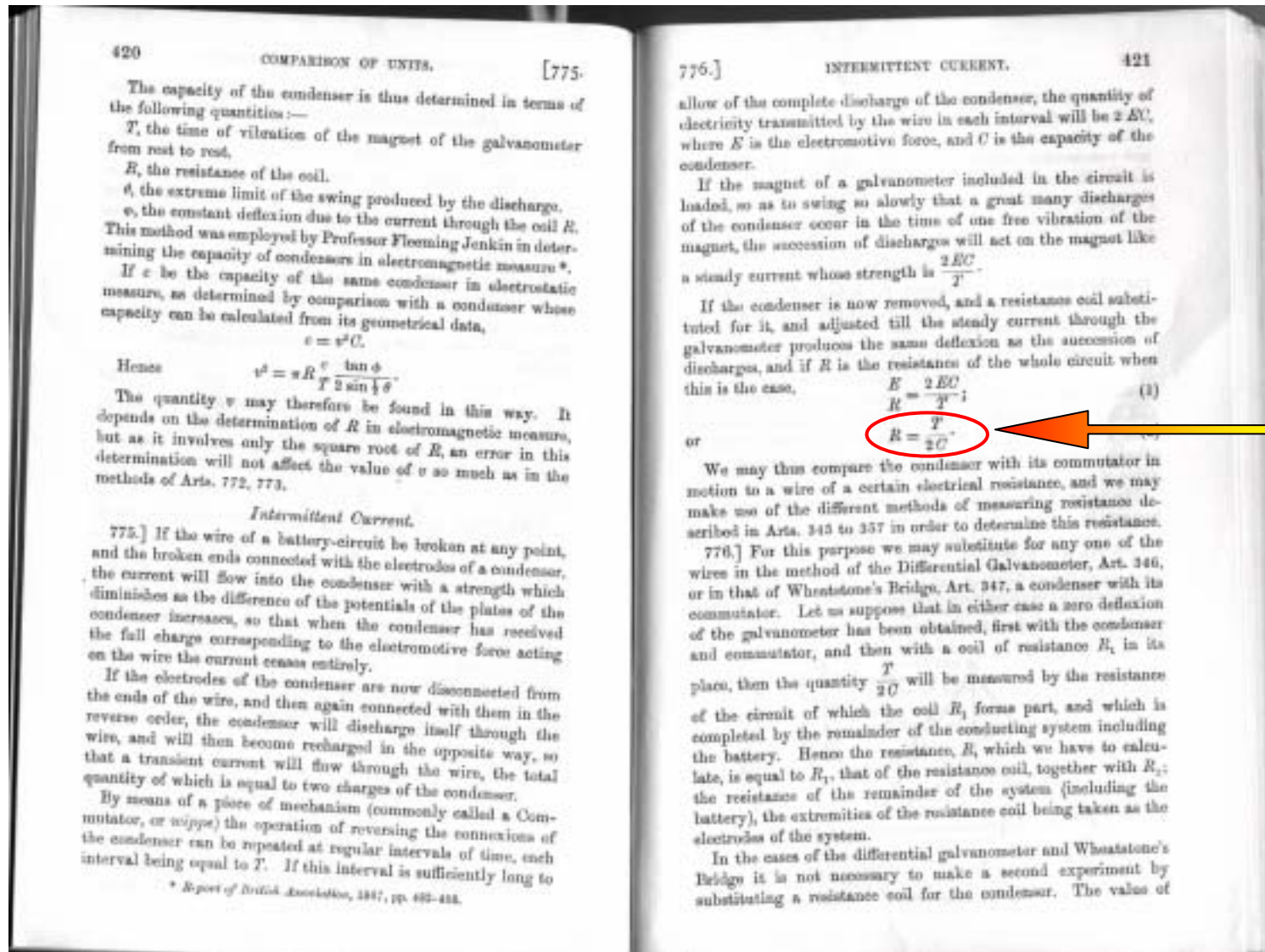
The origins!



The idea that the dc behavior of a capacitor C with periodically interchanged terminals is the same as that of a resistor was already present in a book first published in **1873!!!**

James Clerk Maxwell, *A Treatise on Electricity & Magnetism*, Dover Publications, 1954, Second volume, pp. 420-421.

The origins!



And the first application

IEEE JOURNAL OF SOLID-STATE CIRCUITS, AUGUST 1972

Analog Sample-Data Filters

DAVID L. FRIED

Abstract—An analog sample-data filter exactly equivalent, in the sample-data limit, to a simple RC low-pass filter is demonstrated. The implementation requires only capacitors, MOSFETS, and a pulse generator. The filter time constant can be adjusted by changing the generator's pulse rate. The basic concept is then extended to apply to high-pass and to very-high- Q bandpass filters.

We would like to call attention to what we believe is a rather interesting and previously unrecognized filter-design concept. This concept, indicated in what is probably its simplest form by the 3-dB/octave low-pass filter shown in Fig. 1, should be classified as an analog sample-data filter. While the concept of analog sample-data signal processing is certainly not new [1], [2], we believe that the particular approach taken here seems to represent a minimum in component requirements and design complexity. Variations of the basic concept that provide high-pass, low-pass, bandpass, and comb filter-type options are possible.

Implementation requires only FET gates, capacitors, and a set of timing signals, thus offering potential compatibility with monolithic device technology. Because the characteristic frequencies of the filters are determined by the periodicity of the timing signals, these frequencies can be changed by merely changing the setting of the timing signal generator, a very powerful advantage in certain applications; for example, where a (gang of) filter(s) needs to be varied, precisely, rapidly, and/or under electronic control.

Manuscript received May 26, 1971; revised February 15, 1972. This work was supported, in part, by funding from TRW Systems. The basic concepts presented in this paper are the subject of a patent application, which is assigned to TRW Systems by the inventors, D. L. Fried and G. F. Sochi.
The author is with the Optical Science Consultants, Yorba Linda, Calif. 92686.

The useful frequency range for these filters is probably limited to below a few hundred kilohertz. Like all sample-data devices, these filters have ambiguities associated with aliasing of frequencies above the sample rate, the procedures for suppressing aliasing are straightforward. Output impedance of the filters is high and it is generally necessary to follow the filter with a MOSFET source follower or similar impedance transformer.

Figs. 1-3 illustrate low-pass, high-pass, and high- Q bandpass analog sample-data filters, respectively. An understanding of the principles of operation of these configurations is provided by a study of the low-pass configuration operation. In a simple RC filter, which the low-pass configuration is equivalent to, the resistor slowly transfers charge to or away from the capacitor so that the voltage across the capacitor slowly follows the input voltage. This is exactly the function that the capacitor C_1 in Fig. 1 performs. It transports charge to or away from capacitor C_2 so that the voltage across C_2 follows V_{in} . For the RC filter, the charge-transfer rate is inversely proportional to R . For the low-pass analog sample-data filter shown in Fig. 1, the charge-transfer rate is inversely proportional to T , the repetition period of the pulses controlling the gates and directly proportional to C_1 . Thus, we would expect that $(T/C_1)C_2$ is the time constant for the low-pass analog sample-data filter. Below we show analytically that the circuit in Fig. 1 is, indeed, within the limits of a sample-data approximation, a low-pass filter with a 3-dB frequency of the order of $[2\pi(T/C_1)C_2]^{-1}$.

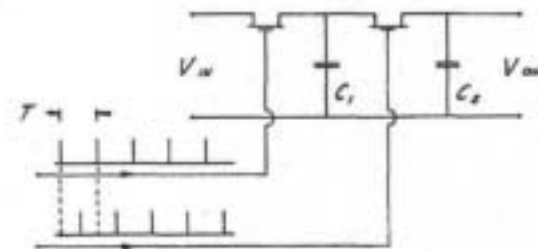


Fig. 1. Low-pass analog sample-data filter.

D. L. Fried, "Analog Sample-Data Filters", *IEEE Journal of Solid-State Circuits*, vol. 7, August 1972, pp. 302-304.



Area and precision advantages

- Let's take again the already discussed example: $RC = 10^{-4}$. Suppose we use a clock frequency $f_c = 100$ kHz.

From $R_1 C_2 = \frac{C_2}{C_1} \cdot \frac{1}{f_c}$ we obtain $\frac{C_2}{C_1} = 10$. This means that

instead of a 10 M Ω resistor (1000000 μm^2) we need a 1 pF capacitor.
We gain a factor 1000 in area!

- The ratio between integrated capacitors can be very well controlled (down to the 0.1 %).
- The clock frequency is also a parameter which can be very precisely controlled.



Outline

- Introduction
- The basic idea behind Switched-Capacitor Circuits
- Capacitors and Switches in CMOS processes
 - Capacitors
 - NMOS, PMOS and CMOS switches
 - Non-idealities introduced by the switches
- 2 circuit examples
- Low-voltage Switched-Capacitor Circuits design
- Conclusions



Capacitors in CMOS

- There are several possibilities of building a capacitor in a CMOS process:

1. Metal (or Poly) over diffusion
2. Metal (or Poly) over Poly
3. Metal over metal

The structure “Poly over diffusion” is present in **ANY** process

- The matching between two capacitors on the same integrated circuit can be very good. For two identical capacitors, we have that

$$\frac{\Delta C}{C} = A \cdot \sqrt{\frac{B}{WL} + C \cdot S^2}$$

where WL is the capacitor area, S it the distance between their centers and A, B and C are constants characteristic of a given technology

- Example: two 1 pF capacitors and $S = 100 \mu\text{m}$. Supposing **$A = 3 \%$** , **$B = 1.8 \mu\text{m}^2$** and **$C = 10^{-4} \mu\text{m}^{-1}$** , we obtain $\Delta C/C = 0.4\%$



NMOS switch

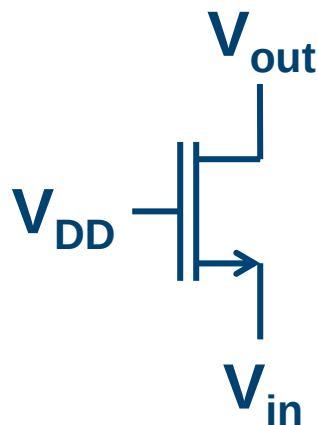
An NMOS transistor can be used as a switch. When the switch is “on” the transistor works in the linear region.

$$I_{DS} = \beta (V_{GS} - V_T - \frac{nV_{DS}}{2}) V_{DS}$$

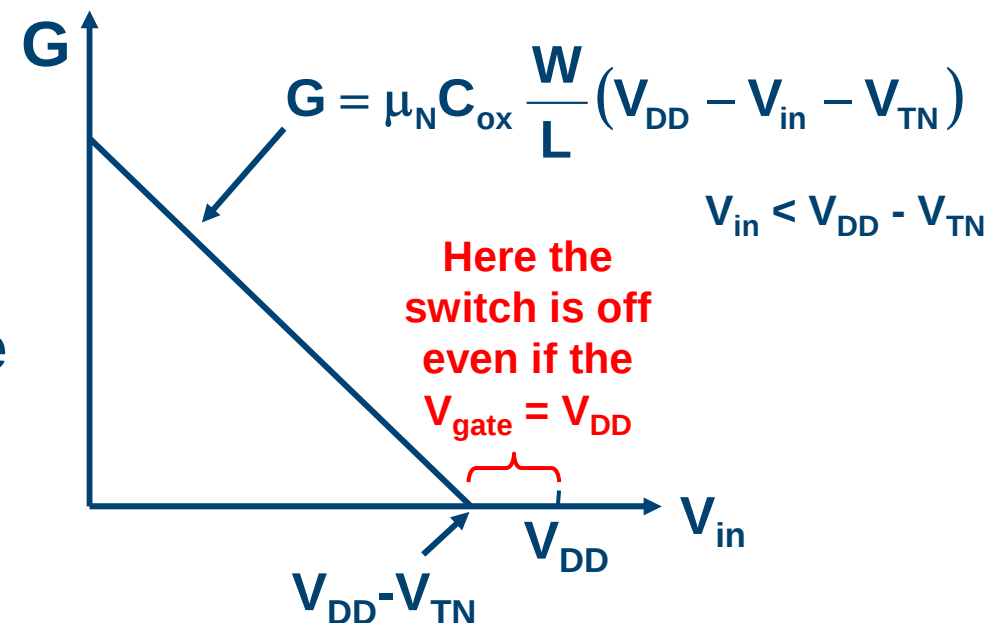
The conductance of the switch is given by

$$G = \frac{\partial I_{DS}}{\partial V_{DS}} = \beta (V_{GS} - V_{TN} - nV_{DS}) = \mu_N C_{ox} \frac{W}{L} (V_{GS} - V_{TN})$$

The switch is on when $V_{gate} = V_{DD}$, it is off when $V_{gate} = 0$ V.



Plot of the
“on”
conductance





PMOS switch

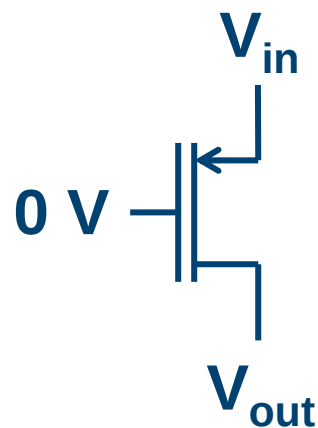
Similar considerations hold for a PMOS transistor.

Remember that for a PMOS transistor the threshold voltage is negative. In the following, V_{TP} is the absolute value of the threshold voltage.

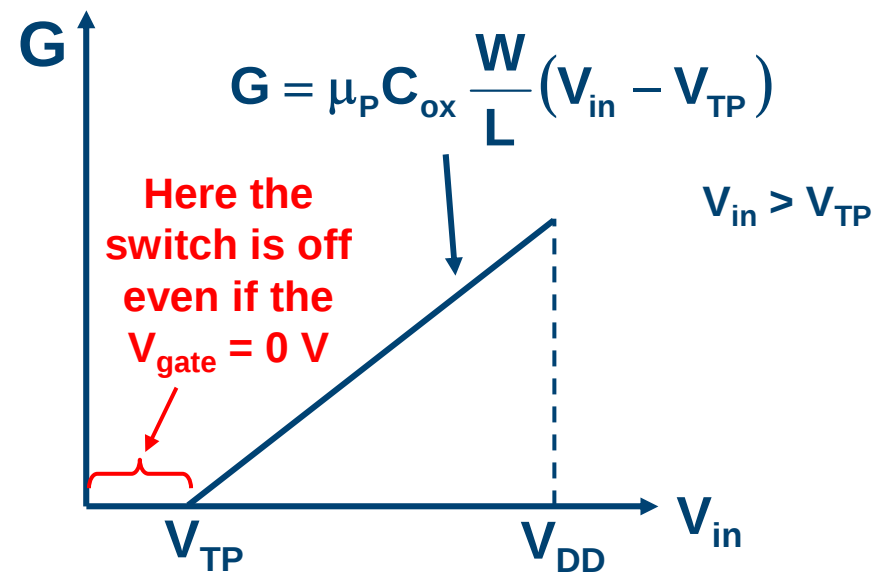
The conductance of the switch is given by:

$$G = \mu_P C_{ox} \frac{W}{L} (-V_{GS} - V_{TP})$$

The switch is off when $V_{gate} = V_{DD}$, it is on when $V_{gate} = 0$ V.



Plot of the
“on”
conductance





CMOS switch

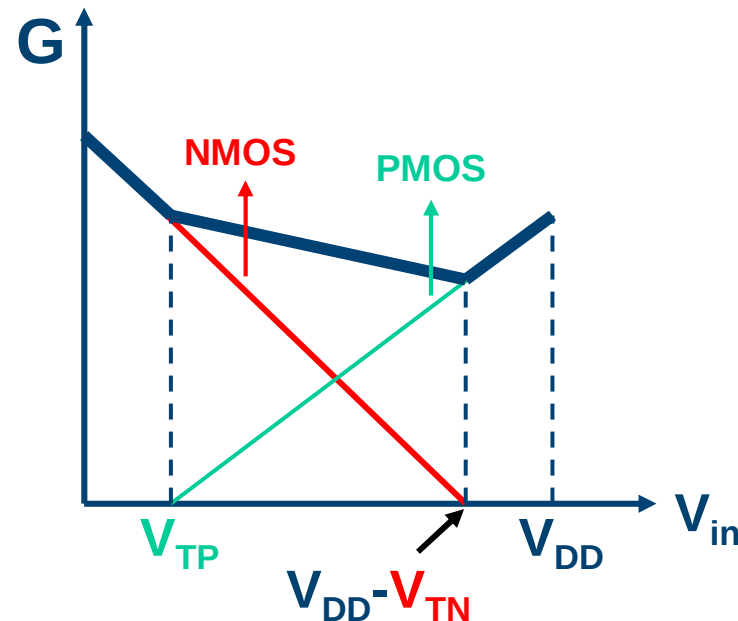
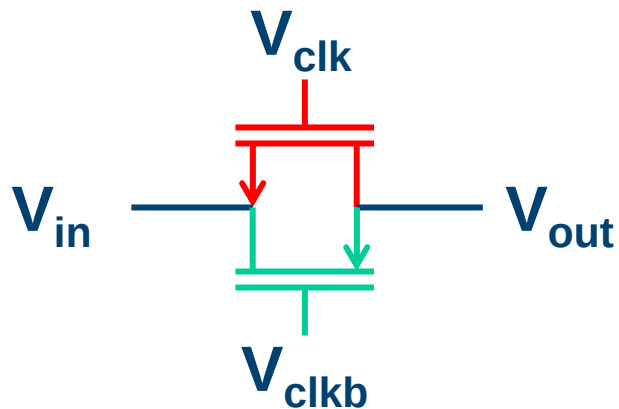
Connecting two transistors (one NMOS and one PMOS) in parallel we obtain a switch with an improved conductance from 0 V to V_{DD} .

The switch is on when: $V_{clk} = V_{DD}$ and $V_{clkb} = 0$ V

$$G_N = \mu_N C_{ox} \left(\frac{W}{L} \right)_N (V_{DD} - V_{in} - V_{TN})$$

$$G_P = \mu_P C_{ox} \left(\frac{W}{L} \right)_P (V_{in} - V_{TP})$$

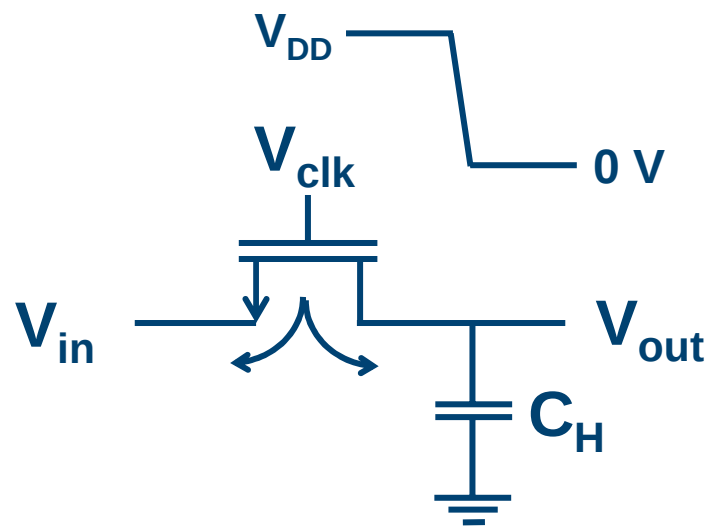
$$G = \begin{cases} G_N & \text{if } V_{in} < V_{TP} \\ G_N + G_P & \text{if } V_{TP} < V_{in} < V_{DD} - V_{TN} \\ G_P & \text{if } V_{DD} - V_{TN} < V_{in} < V_{DD} \end{cases}$$





Channel Charge injection

When a switch is turned off the charge Q_{ch} which constitutes the inversion layer exits through the source and drain terminals. It is difficult to determine which fraction of charge will go on the sampling capacitor C_H . For a worst-case calculation, we will assume that all the charge goes on C_H .



$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_T)$$

$$V_{out} \approx V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_T)}{C_H}$$

$$V_{out} \approx V_{in} \left(1 + \frac{WLC_{ox}}{C_H} \right) - \frac{WLC_{ox}}{C_H} (V_{DD} - V_T)$$

Charge injection introduces therefore a gain and an offset error.



Channel Charge injection

In the previous slide, we did not take into account the bulk effect!

If we do, we see that charge injection also gives **non linearity** errors.

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{V_{sb} + \phi_{Si}} - \sqrt{\phi_{Si}} \right) \quad \gamma = \frac{\sqrt{2q\epsilon_{Si}N_a}}{C_{ox}}$$

$$V_{out} \approx V_{in} \left(1 + \frac{WLC_{ox}}{C_H} \right) + \gamma \frac{WLC_{ox}}{C_H} \sqrt{\phi_{Si} + V_{in}} - \frac{WLC_{ox}}{C_H} (V_{DD} - V_{T0} + \gamma \sqrt{\phi_{Si}})$$

The non linearity comes from the dependence of V_T upon V_{IN} .

From this formula we see that to minimize the effect of the charge injection we should make the switch as small as possible.

B. J. Sheu and C. Hu, "Switch-Induced Error Voltage on a Switched Capacitor", *IEEE JSSC*, vol. 19, no. 4, August 1984, pp. 519-525.

J. B. Kuo et al., "MOS Pass Transistor Turn-Off Transient Analysis", *IEEE TED*, vol. 33, no. 10, October 1986, pp. 1545-1555.

J.-H. Shieh et al., "Measurement and Analysis of Charge Injection in MOS Analog Switches", *IEEE JSSC*, vol. 22, no. 2, April 1987, pp. 277-281.

G. Wegmann et al., "Charge Injection in Analog MOS Switches", *IEEE Journal of Solid-State Circuits*, vol. 22, no. 6, Dec. 1987, pp. 1091-1097.



Speed-precision trade-off

To be less sensitive to charge injection we can:

- make the sampling capacitor bigger
- make the switch smaller (in area)

Both these solutions increase the RC constant of the circuit, making it slower. To evaluate the speed-precision trade-off, we calculate the product $\tau \cdot \Delta V$, where $\tau = RC$ represents the inverse of the speed and ΔV the error. We obtain:

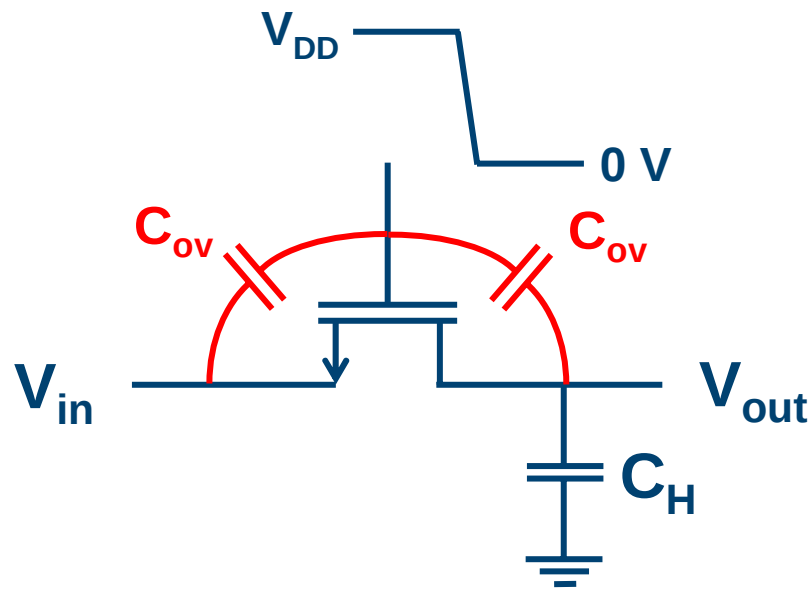
$$\tau = R_{\text{on}} C_H = \frac{C_H}{\mu C_{\text{ox}} \frac{W}{L} (V_{\text{DD}} - V_{\text{in}} - V_{\text{T}})} \quad \Delta V = \frac{W L C_{\text{ox}} (V_{\text{DD}} - V_{\text{in}} - V_{\text{T}})}{C_H}$$
$$\tau \cdot \Delta V = \frac{L^2}{\mu}$$

It is interesting to note that this product does not depend on the switch width nor on the sampling capacitor, **and that it improves (becomes smaller) with scaling!**



Clock Feedthrough

The overlap capacitances between gate and source or drain couple the clock transition to the sampling capacitance when the switch is switched off. This also introduces an error, which is proportional to the width W of the transistor.



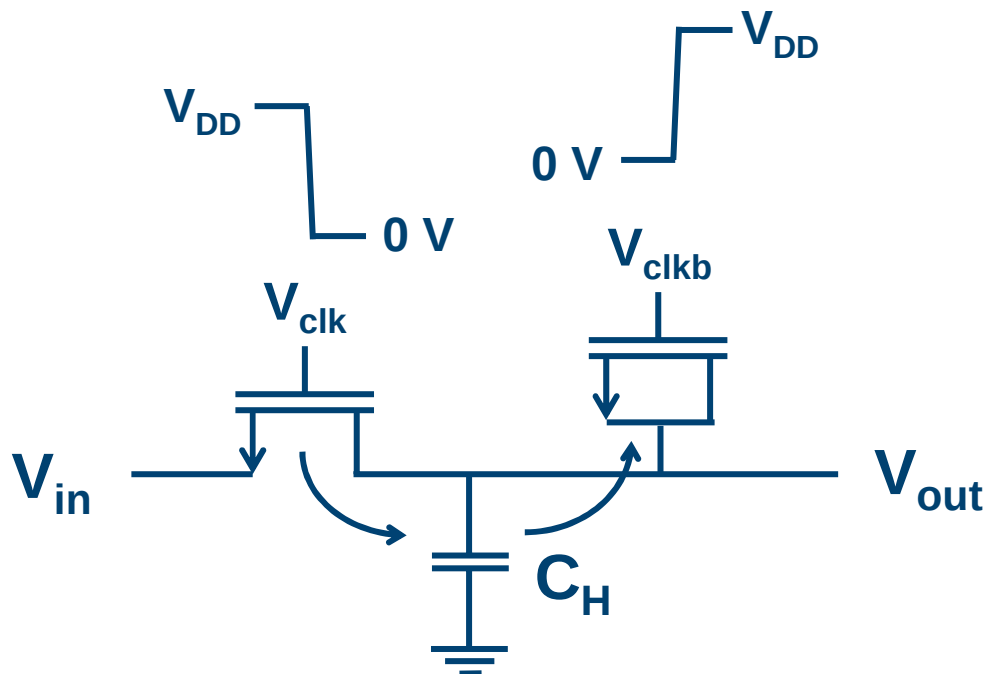
$$V_{out} \approx V_{in} - V_{DD} \frac{WC_{ov}}{WC_{ov} + C_H}$$

The clock feedthrough introduces an offset error.



Charge injection cancellation

To reduce the charge injection problem we can use dummy switches.



If we assume that half of the charge in the switch channel goes towards the sampling capacitor, then

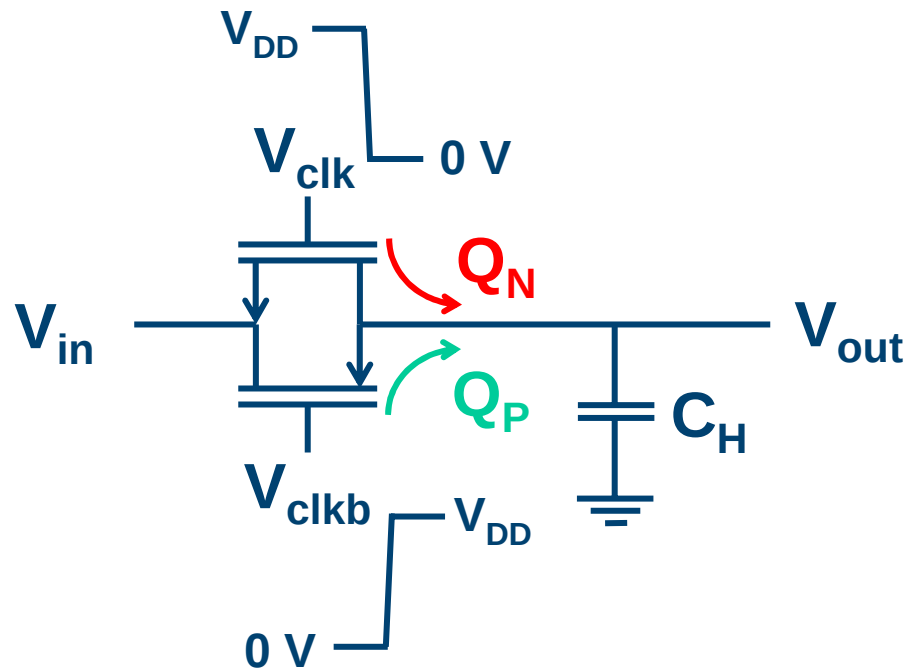
$$W_{dummy} = \frac{1}{2} W_{switch}$$

The assumption we made is not exact, and therefore this method is not perfect. On the other hand, it is interesting to note that dummies eliminate the clock feedthrough problem (with the sizing of the transistors indicated).



Charge injection cancellation

Another (not much more effective) technique is to use CMOS switches.



$$Q_N = W_N L_N C_{ox} (V_{DD} - V_{in} - V_{TN})$$

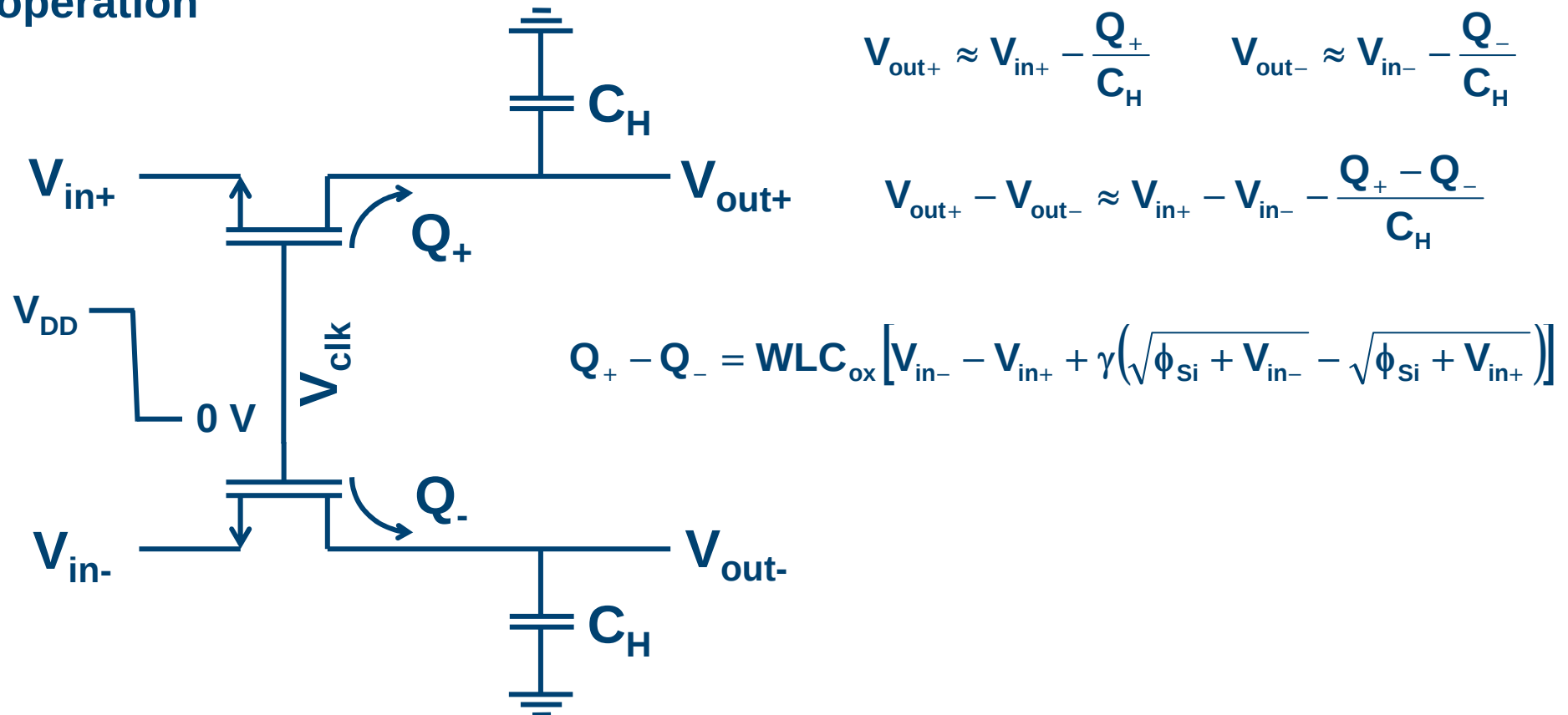
$$Q_P = W_P L_P C_{ox} (V_{in} - V_{TP})$$

In this case, perfect cancellation is provided only for one input level. This technique is not perfect for clock feedthrough either, since the overlap capacitances for NMOS and PMOS are slightly different.



Charge injection cancellation

The third possibility to fight charge injection is to use differential operation



This technique removes the constant offset and reduce the nonlinear component. It is also effective for the clock feedthrough.



Other non-idealities

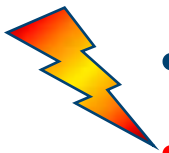
There are several other things which can create problems in SC circuits:

- Switches junction leakage
- Parasitic capacitances of the sampling capacitor and of the switches
- Timing differences between clk and clkb in CMOS switches
- Op-amp DC offset voltage
- Op-amp finite DC gain
- Op-amp finite bandwidth
- Op-amp finite slew rate
- Op-amp nonzero output resistance
- Noise in switches and op-amps
- Noise injection from power, ground and clock lines and from the substrate



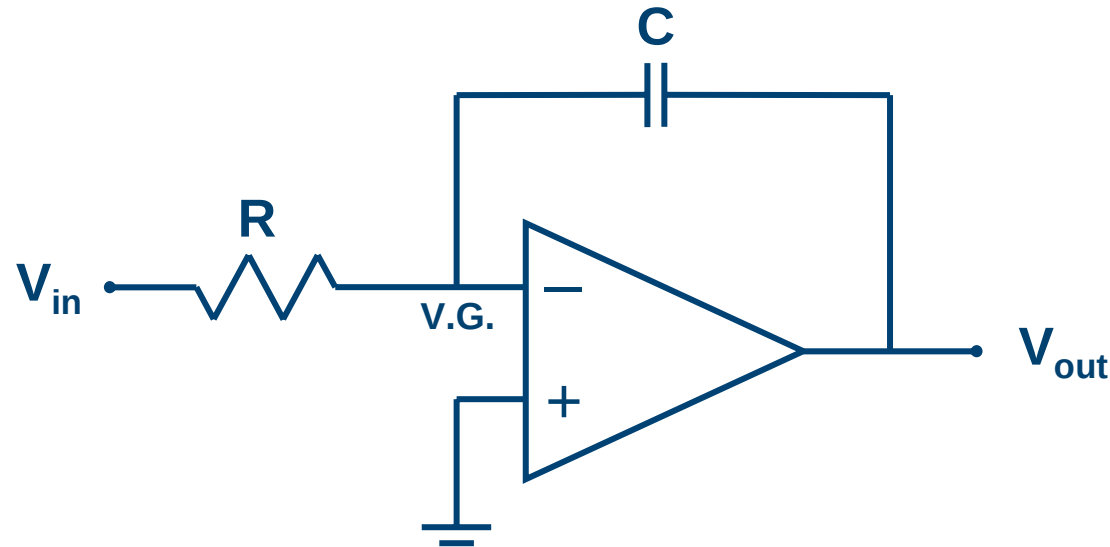
Outline

- Introduction
- The basic idea behind Switched-Capacitor Circuits
- Capacitors and Switches in CMOS processes
- 2 circuit examples
 - SC integrator
 - Non-filtering applications of SC Circuits
 - Multiply-by-two circuit
- Low-voltage Switched-Capacitor Circuits design
- Conclusions





Active RC integrator



Integrators are very useful analog blocks, extensively used in filters and oversampled Analog-to-Digital Converters. If the gain of the operational amplifier is very high (and therefore the negative input behaves as a virtual ground), we can write:

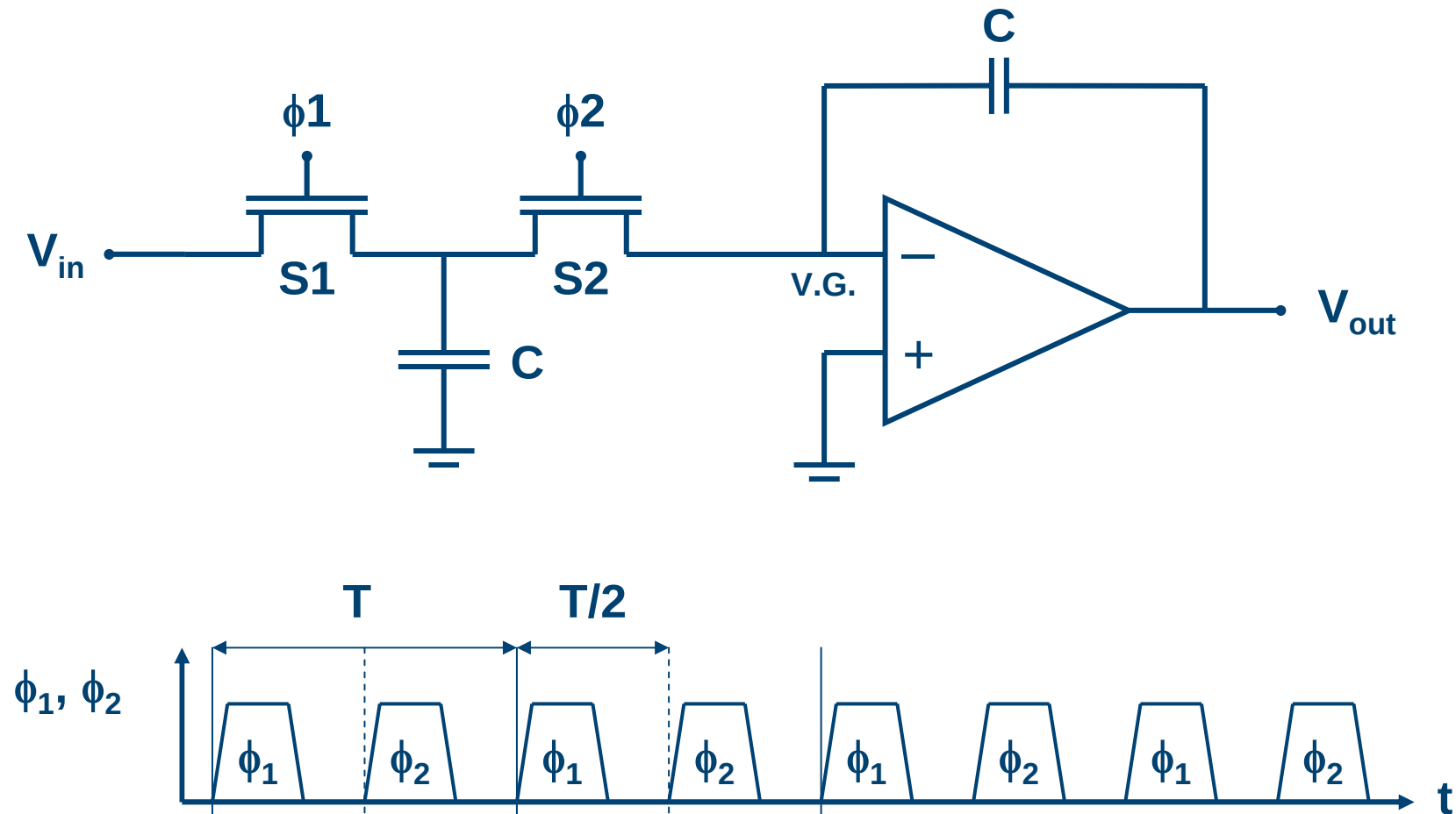
$$H(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = -\frac{1}{sRC}$$

$$V_{\text{out}}(t) = -\frac{1}{RC} \int V_{\text{in}}(t) dt$$

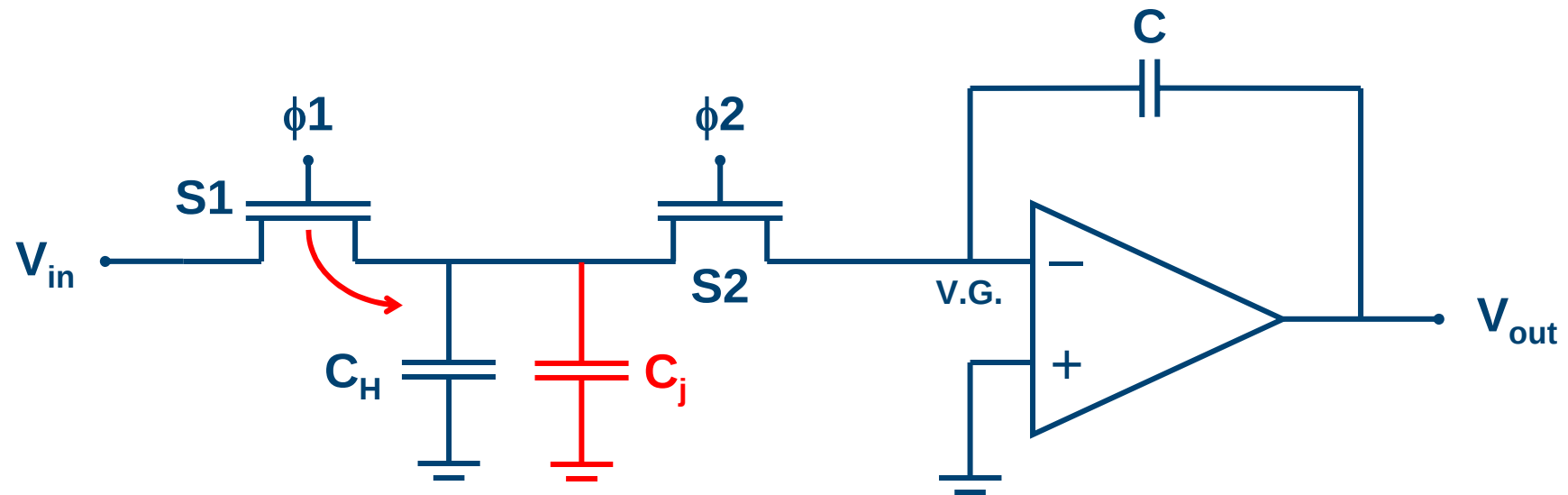


Switched-capacitor integrator

Substituting the resistor with its switched-capacitor equivalent we obtain:



Non idealities effects

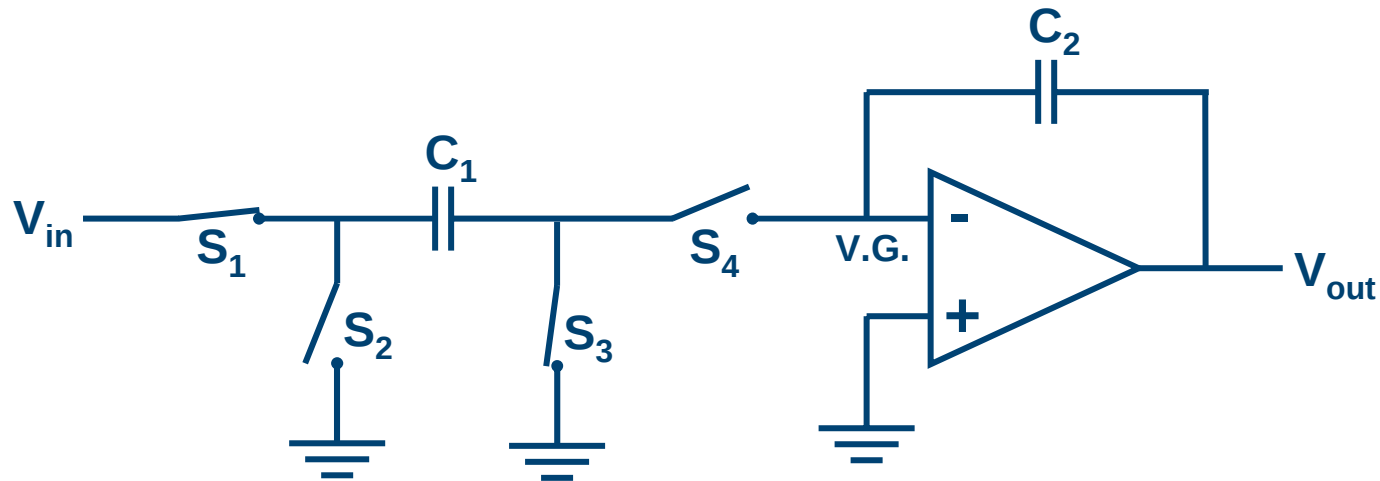


This implementation of a SC integrator suffers from two important effects:

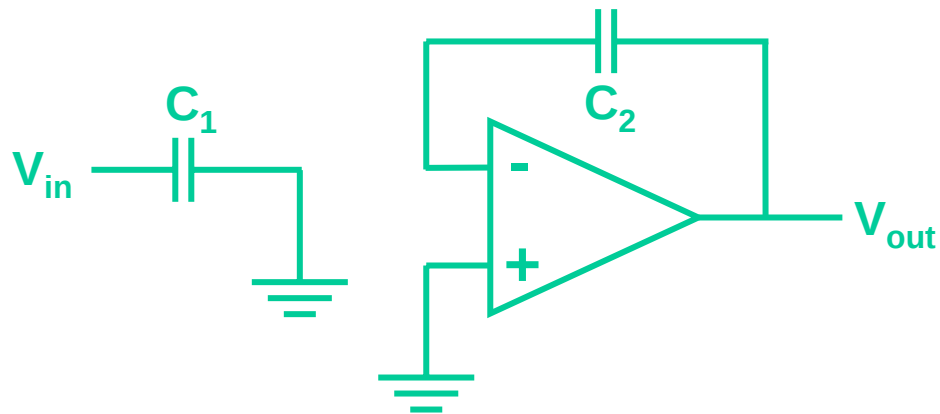
- The input-dependent charge injection from $S1$
- The voltage dependent parasitic (stray) capacitances of the diffusions of the two switches $S1$ and $S2$ give origin to nonlinearities.



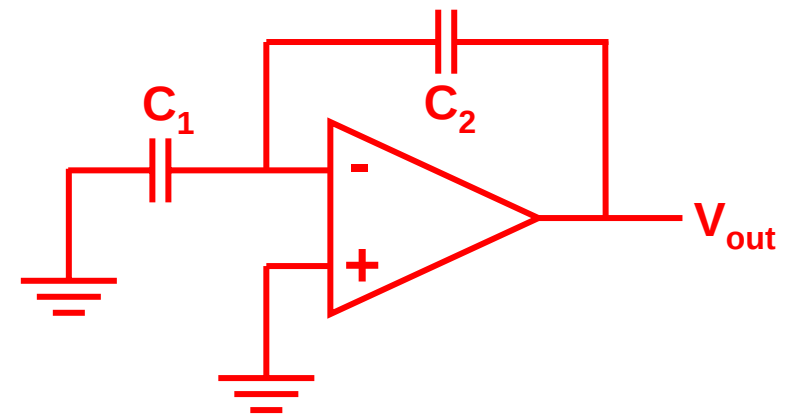
Stray-insensitive SC integrator



SAMPLING MODE

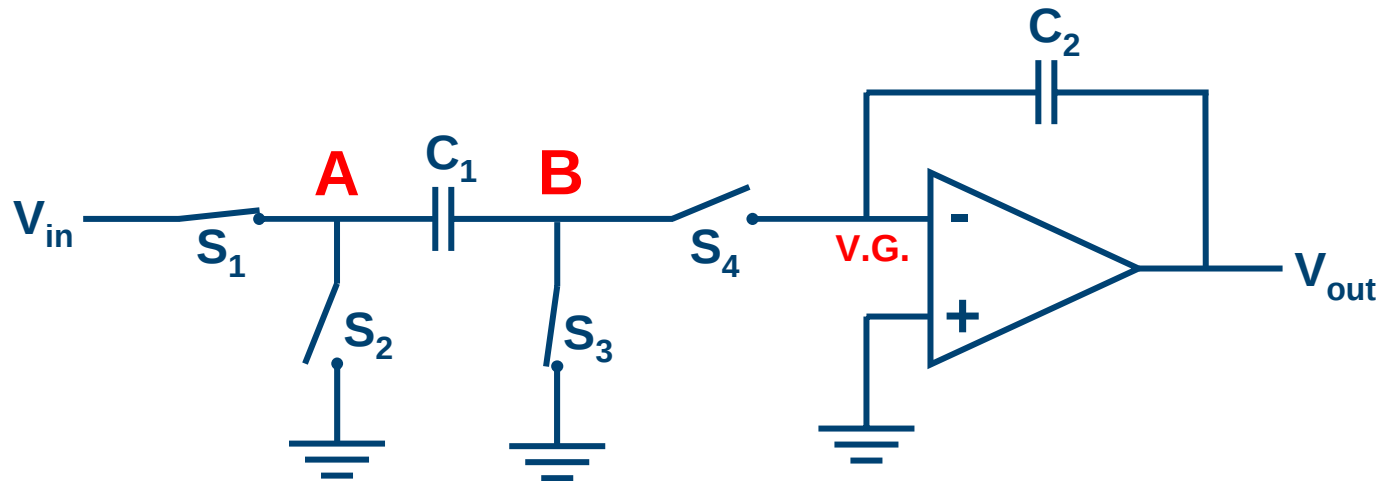


INTEGRATION MODE





Stray-insensitive SC integrator



The stray capacitances @ the nodes **A**, **B** and **V.G.** do not count anymore because:

C_A (Node A) is constantly switched between V_{in} and ground.

C_B (Node B) is grounded at both terminals.

C_C (Node C) is grounded at both terminals.

In the transition from sampling mode to integration mode **S3** turns off first, and its charge injection introduces a constant offset. **S1** turns off after **S3**, so that its charge injection does not count.



SC filters disadvantages

- SC filters must be preceded by an Anti-Aliasing filter and followed by a Smoothing Filter. This complicates the overall system and increase the power consumption.
- The accuracy is limited to about 0.1 %. This is “only” 10-bit. For some applications, higher accuracies are needed.
- The dynamic range (which is basically the maximum SNR) is rarely more than 100.000 (100 dB). This is due to the various sources of noise coming from the amplifiers, the switches and the substrate.
- Digital filters are more easily programmable and more flexible.
- Sampled signals systems can not be analyzed with Laplace or Fourier transformations. They need a special mathematical tool, called z-transformation. We will not have the time to see it here...
- SC filters are integrated circuits. The economical advantage is there only for great numbers!

$$\text{Development cost} + \text{IC_cost} * N < \text{Hybrid_circuit_cost} * N$$



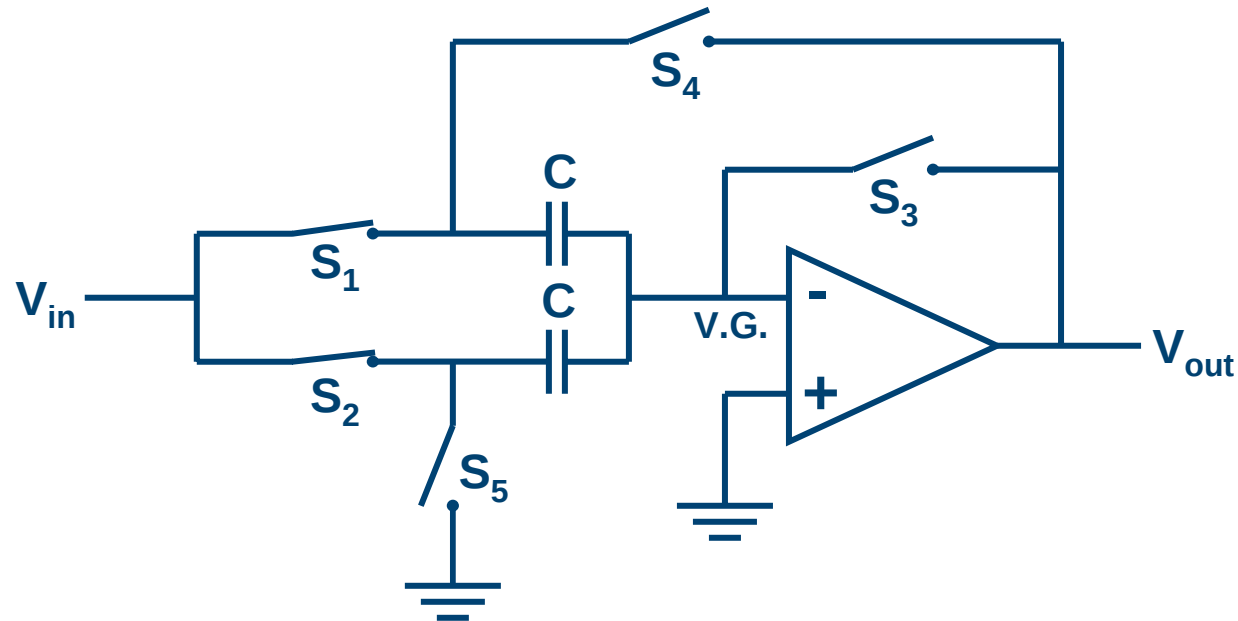
Non filtering application of SCC

A part from filtering purposes, switched-capacitor circuits are widely used in many other analog signal processing applications:

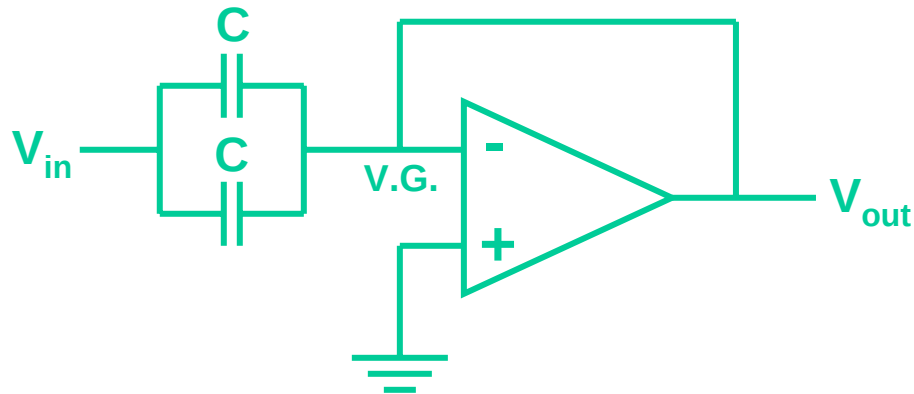
- **Voltage amplifiers**
- **Analog-to-Digital Converters**
- **Digital-to-Analog Converters**
- **Voltage comparators**
- **Modulators**
- **Rectifiers**
- **Peak detectors**
- **Oscillators**



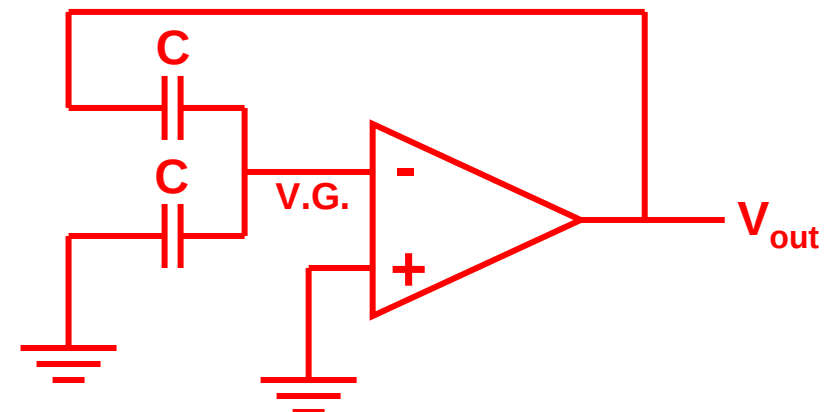
Multiply-by-two circuit



SAMPLING MODE

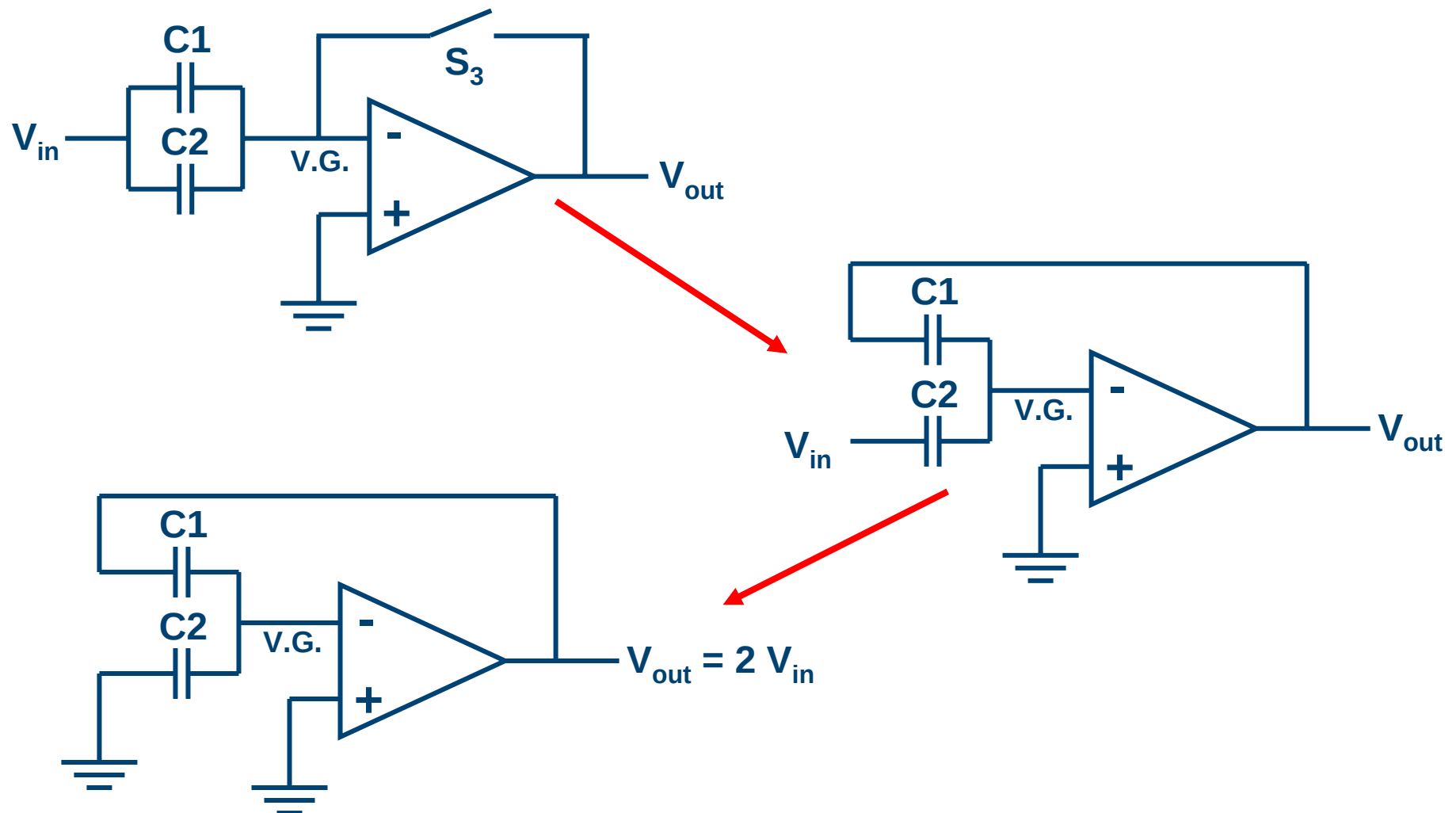


AMPLIFICATION MODE



Multiply-by-two circuit

Transition from sampling mode to accumulation mode.





Outline

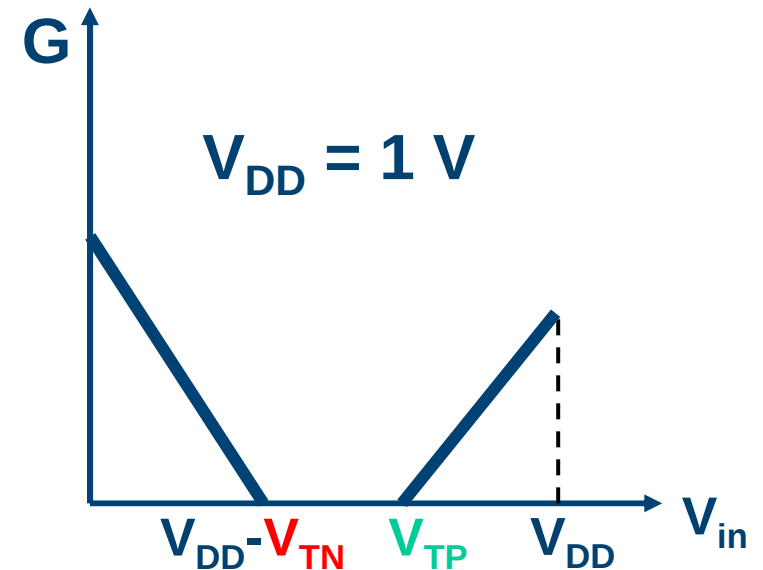
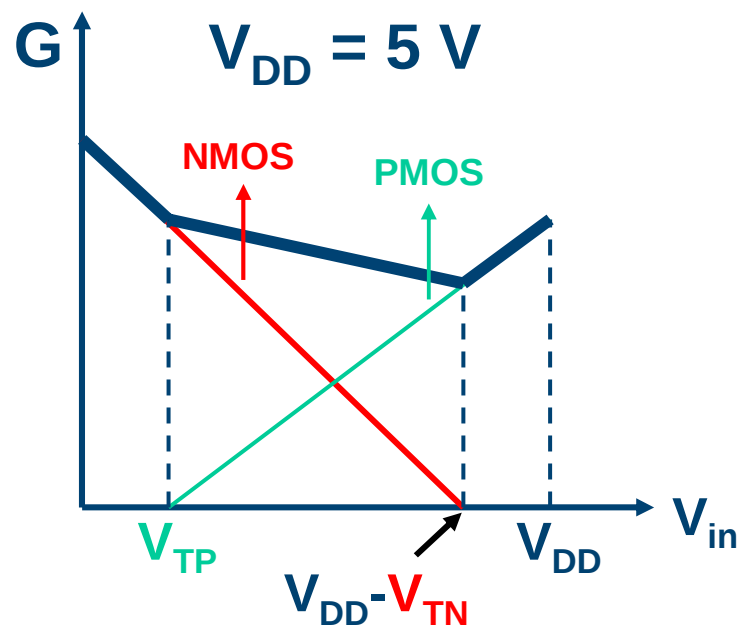
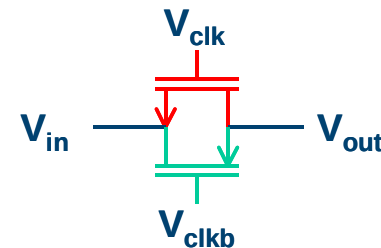
- Introduction
- The basic idea behind Switched-Capacitor Circuits
- Capacitors and Switches in CMOS processes
- 2 circuit examples
- **Low-voltage Switched-Capacitor Circuits design**
 - The problem: MOS switches @ low V_{DD}
 - Possible solutions
- Conclusions





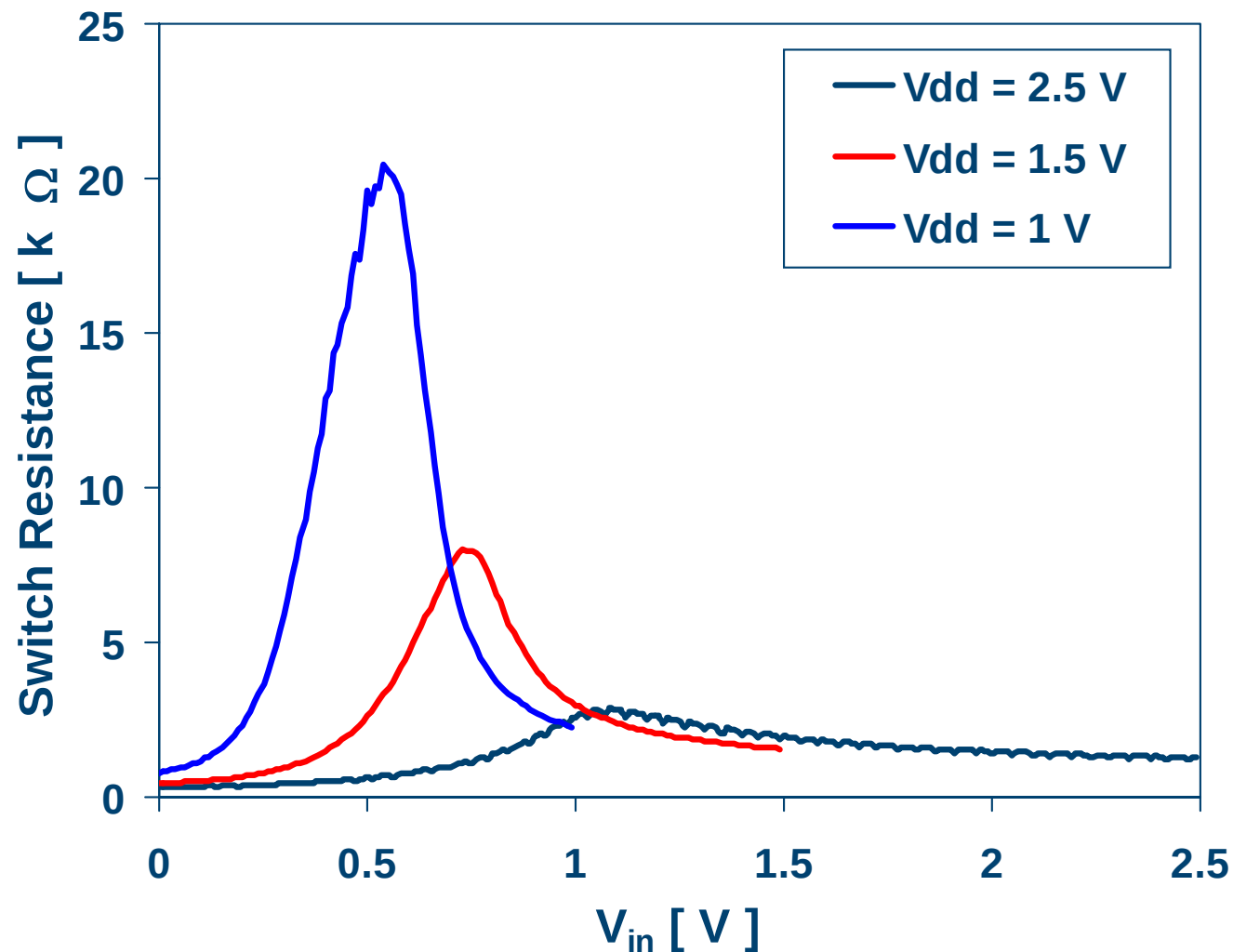
CMOS switch @ low V_{DD}

The maximum voltage which can drive the gates of the switch is V_{DD} . If V_{DD} is not high enough (at least $> V_{TN} + V_{TP}$), we can have a “hole” in the conduction curve of the switch.





Measured switch “on” resistance



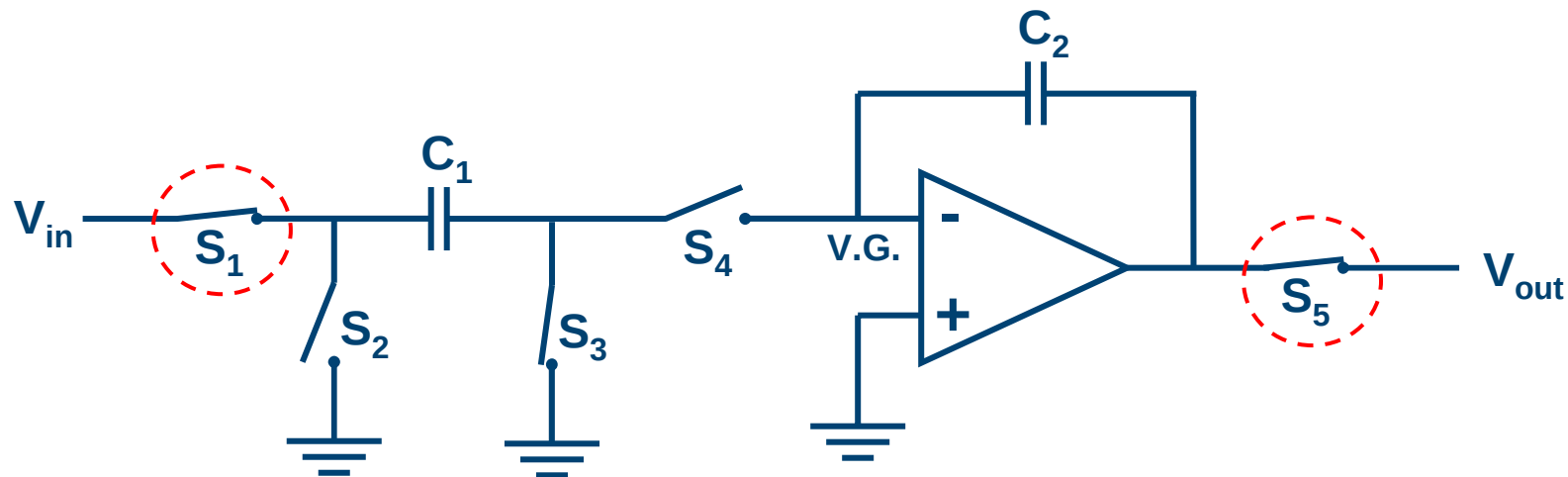
CMOS switch made in a $0.25\text{ }\mu\text{m}$ process. The NMOS and the PMOS transistors have the same size.

The three measurements are made @ three different V_{DD}



Low-voltage SC Circuits

The problem of the switches is seen at the circuit level. If we take, as an example, the stray insensitive SC integrator shown below, we see that the switches S_1 and S_5 are not capable to transmit the signal as desired. These switches are called “**floating**” switches. All the other switches are connected to ground (or virtual ground), so they do not give problems.



M. Keskin et al., “A 1-V 10-MHz Clock-Rate 13-Bit CMOS $\Delta\Sigma$ Modulator Using Unity-Gain-Reset Opamps”, *IEEE JSSC*, vol. 37, no. 7, 2002, p. 817.

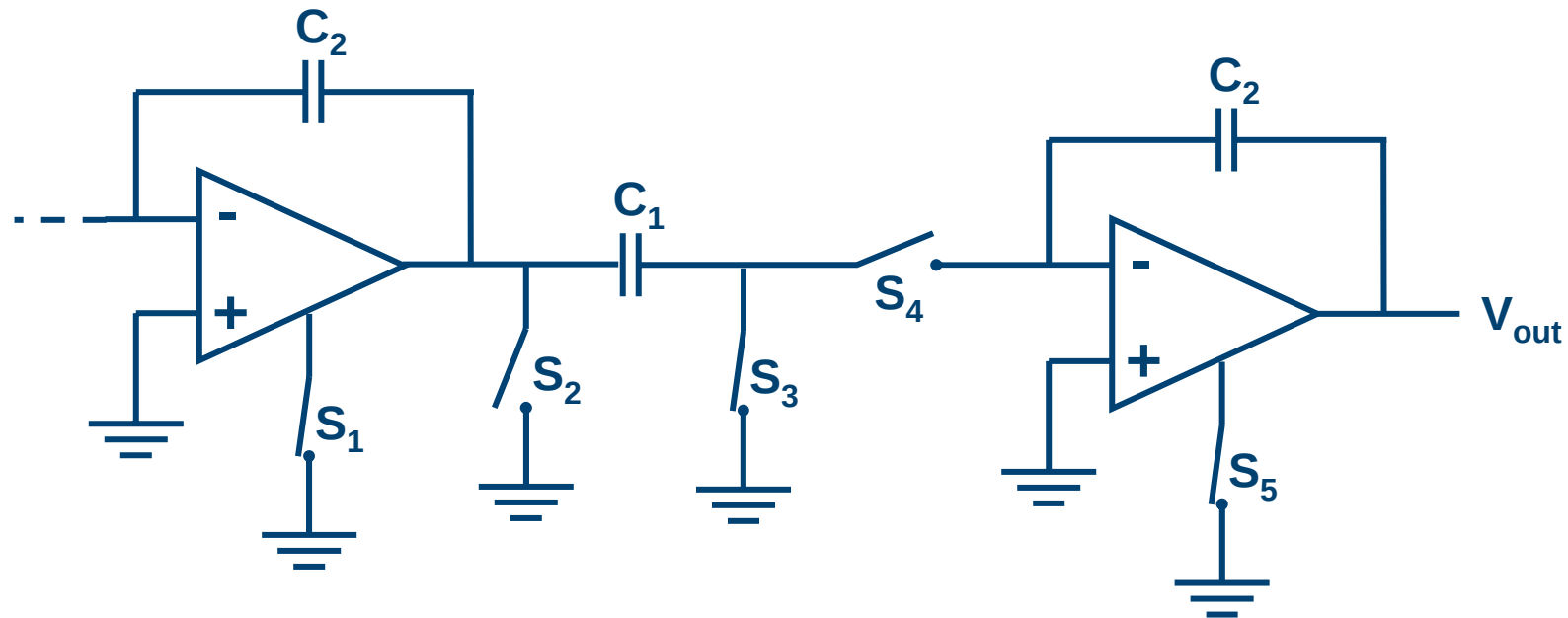
J. Crols and M. Steyaert, “Switched-Opamp: An Approach to realize Full CMOS Switched-Capacitor Circuits at Very Low Power Supply Voltages”, *IEEE Journal of Solid-State Circuits*, vol. 29, no. 8, August 1994, p. 936-942.

J.-T. Wu and K.-L. Chang “MOS Charge Pumps for Low-Voltage Operation”, *IEEE JSSC*, vol. 33, no. 4, April 1998, p. 592-597.



Switched op-amp technique

The switched op-amp technique replaces the floating switches with operational amplifiers, which are switched on and off. When the op-amp is off, its output is grounded.



This technique solve the problem but limits the maximum speed of the circuit because of the time required for the powerup / powerdown of the op-amps. Moreover, it requires the design of special low-voltage op-amps



Other solutions

Other possible solutions are:

Low-threshold voltage devices. This solve the problem of the high R_{on} of the switches in the middle of the dynamic range, but it introduces other problems due to the high leakage currents when the switch is off. This can lead to unacceptable charge losses. Moreover, low-threshold voltage devices are not always available or imply an additional cost.

Charge-pump circuits. These circuits allow multiplying on chip a low voltage. The multiplied voltage can then be used to drive the switches. Besides the fact that charge-pump circuits require chip area and power, the main drawback of this techniques is that for some signals the gate oxide can undergo an important stress. This can have a severe impact on the reliability of the circuit.

Reset op-amp technique. It is similar to the switched op-amp technique, since it uses op-amps to replace the floating switches. In this case, the op-amps are always on, and therefore this technique allows a faster operation of the circuits.



Outline

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Pros and Cons of SC filters

- + Accuracy: center frequency accuracy in the order of 0.2 %
- + Frequency range: from < 0.1 Hz to > 100 kHz
- + Tunability: simply change the clock frequency!
- + Low-cost when speed and accuracy are needed
- + High dynamic range (despite the noise)
- + System design effort
- + Components Count / Circuit Board Area
- Noise: they use op-amps, switches and a clock
- Offset voltage
- Aliasing: a low-pass filter is needed before the SC filter if the input signal has components at a frequency higher than $f_{ck}/2$