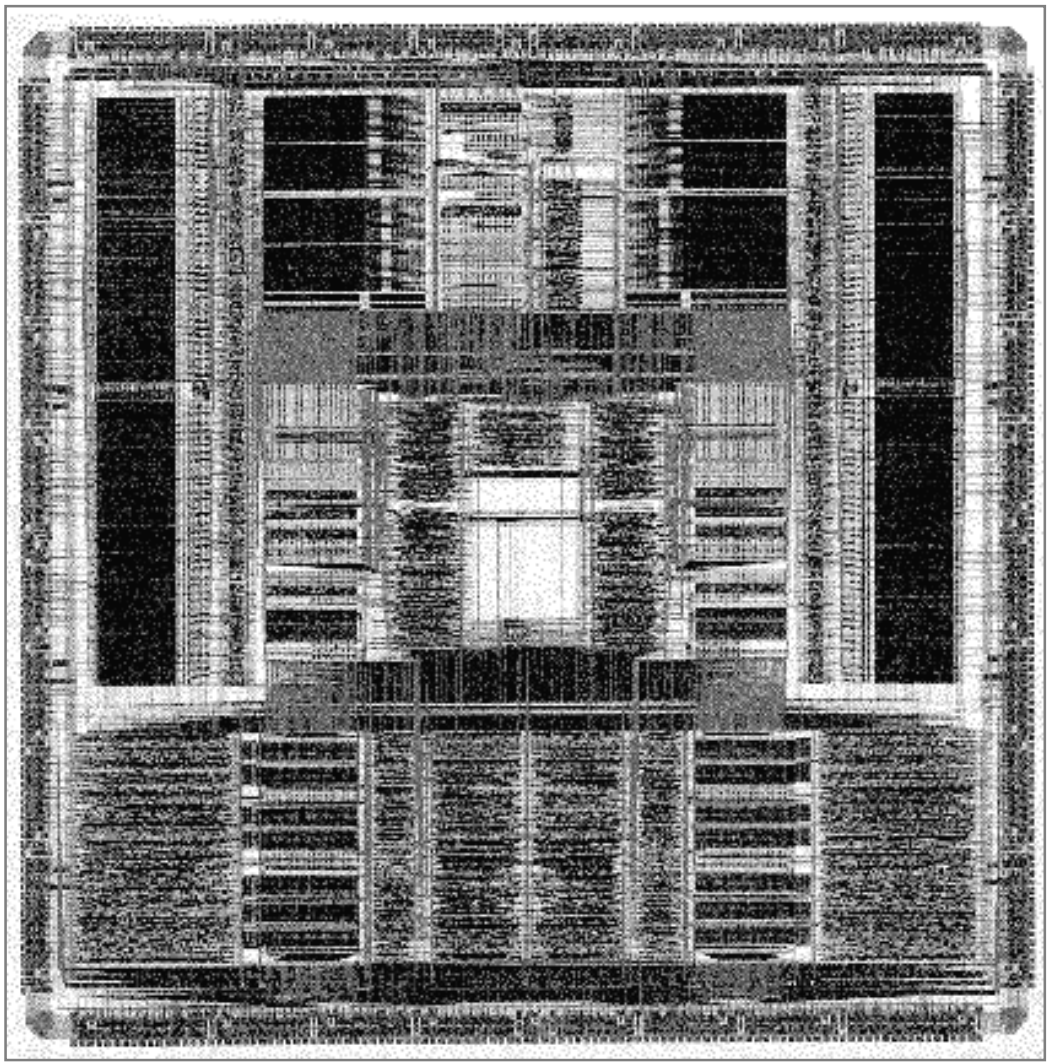
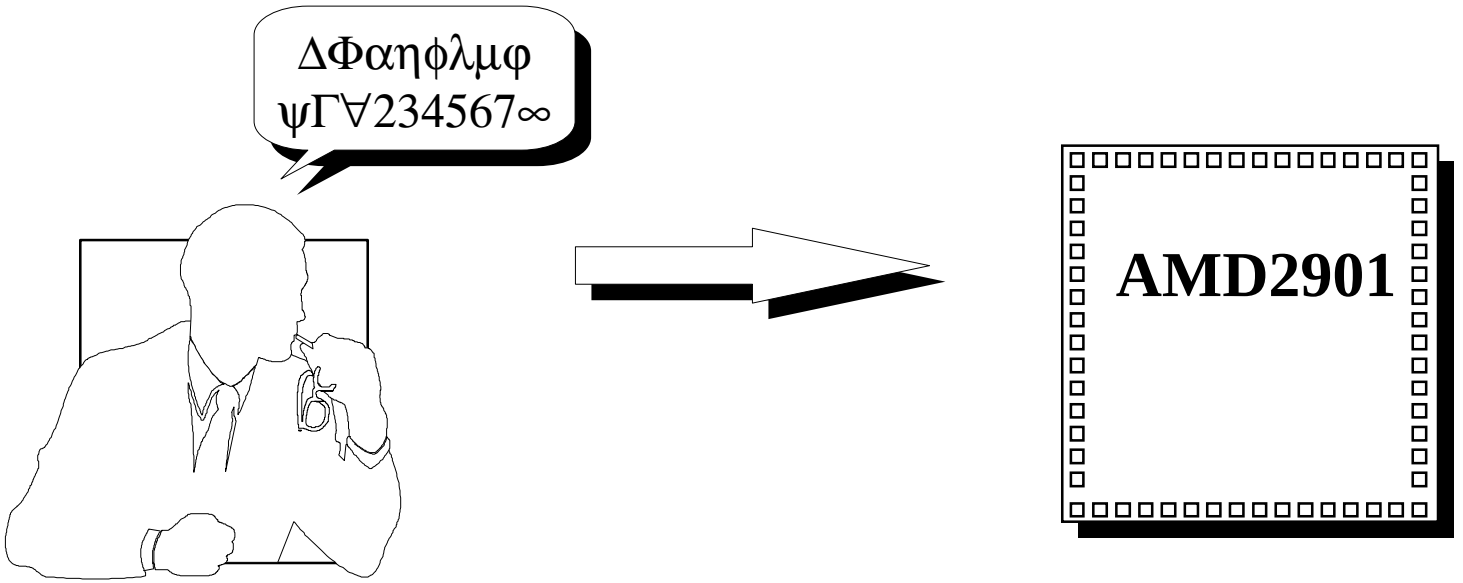
OUTLINE

I - INTRODUCTION

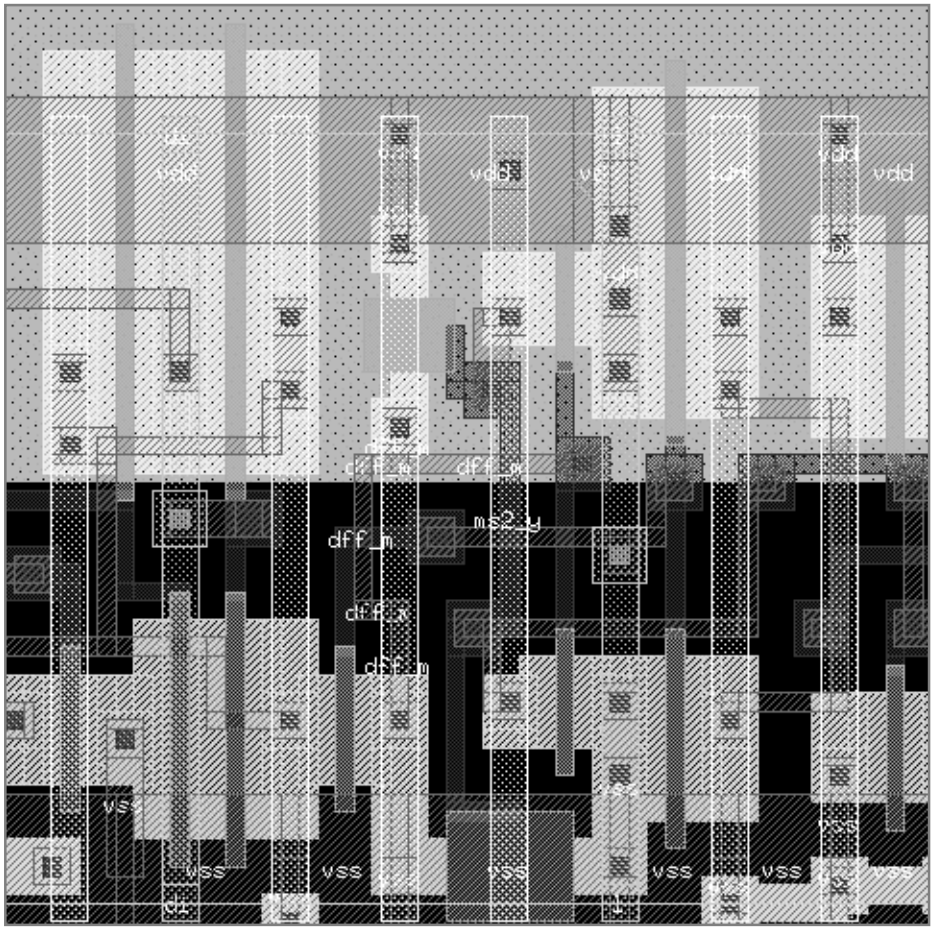
II - DESIGN METHODOLOGY : AN OVERVIEW



DESIGNER'S DREAM

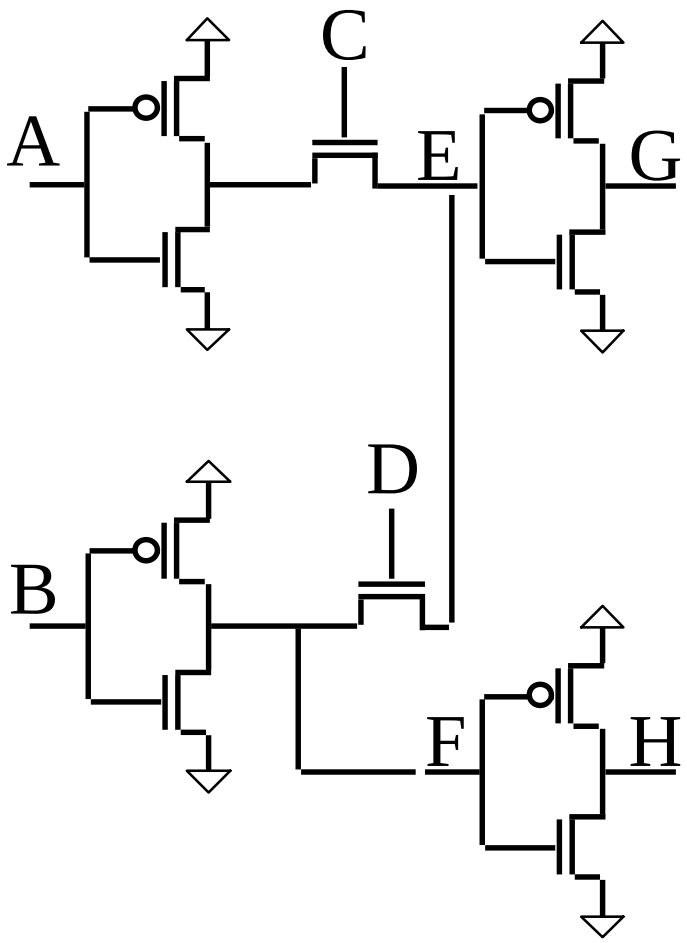


Millions of Segments Put Together



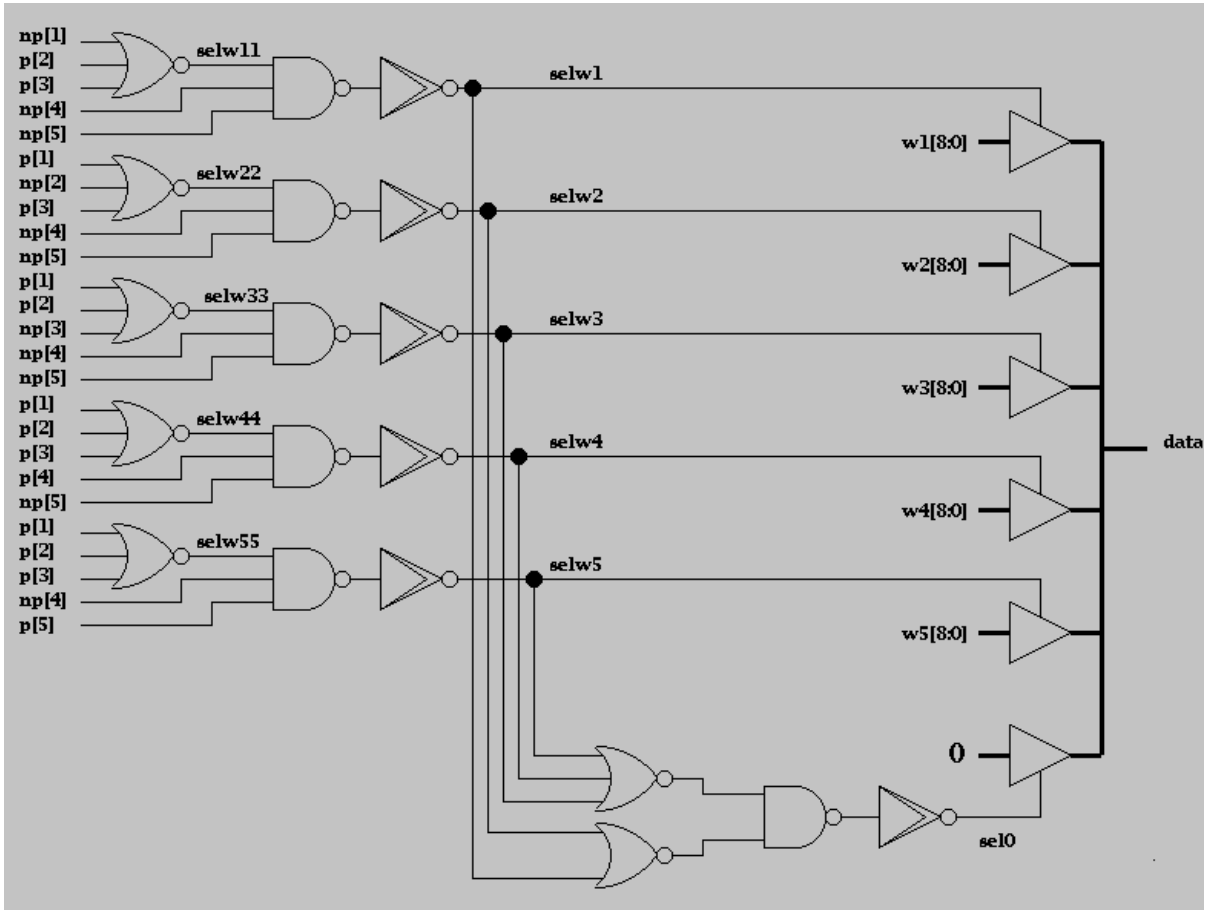
How to deal with such complexity ?

Millions of Transistors Connected Together



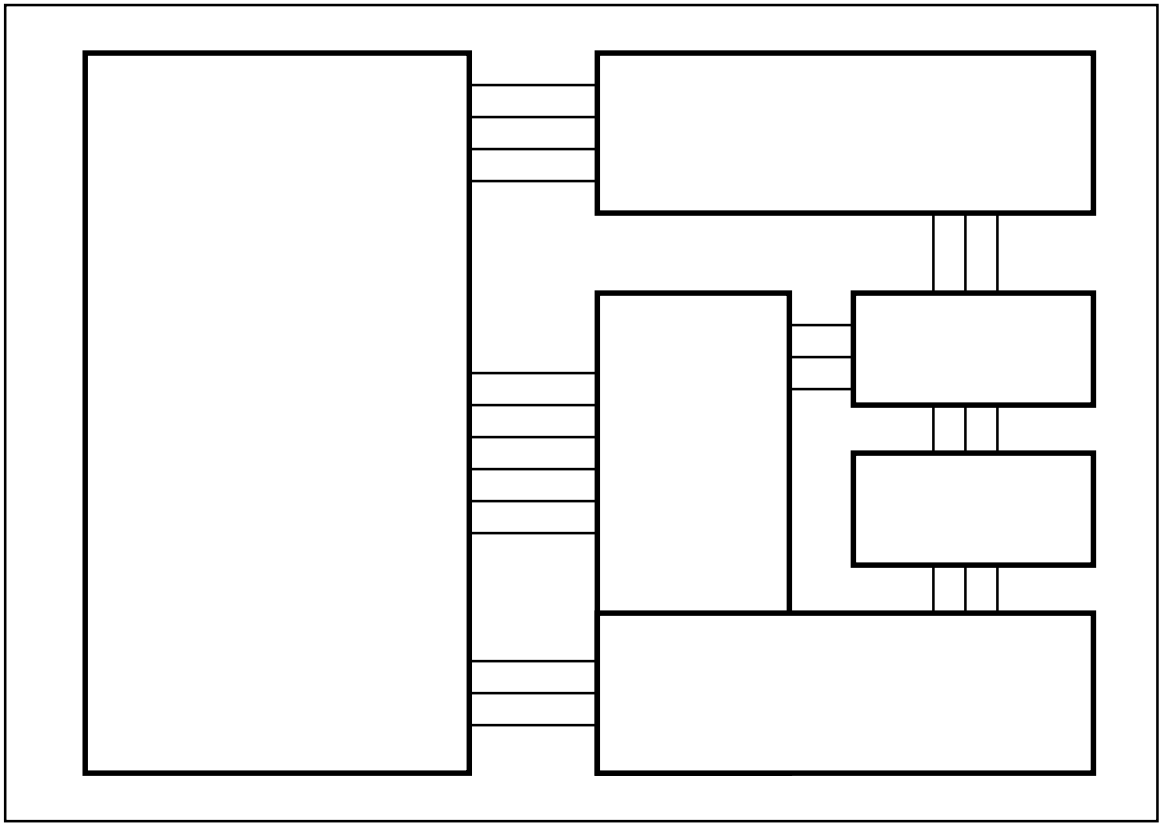
- **Still Too Complex.....!!!**

Thousands of Cells Connected Together



- **Still Too Complex.....!!!**

Dozen of Functional Blocks Communicating Together



😐 I'm Starting to Understand

A Set of Equations Reflecting the Circuit's functionality

```
entity  simple is
port (
        a, b: Bit;
         c, d : bit
       );

architecture  simple is

a <= b or c
d <= b and c;
end;
```

- ✓ **I Understand What this Circuit is Supposed to Do**

SO,

How to deal with such complexity ?

- ✓ ABSTRACTION
- ✓ HIERARCHY

LEVELS OF ABSTRACTION

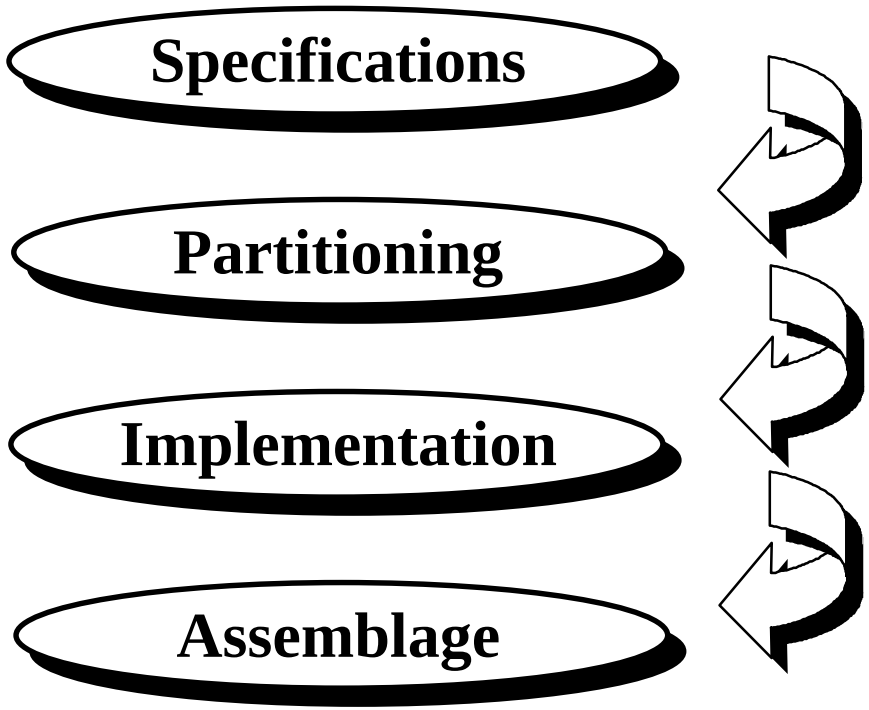
To Go Across These Different Levels of Abstraction

I Need

A Design **M E T H O D O L O G Y**

DESIGN METHODOLOGY

TOP-DOWN METHODOLOGY



STEP 1: SPECIFICATIONS (1)

Put Down the Circuit Concept

Two reasons:

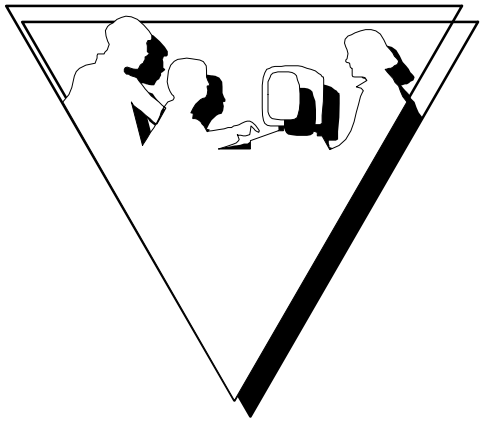
- To be able to check it before manufacturing
- To have a reference manual for communication

STEP 1: SPECIFICATIONS (2)

Communication Language

Between People on the Project
Between People and Computers

- No Ordinary Language
- Accurate Language
- A Language that Can Be Simulated



STEP 2: PARTITIONING (1)

Divide and conquer strategy

Very difficult step: Relays on the know-how of the designer.

Main idea: To split into several small parts

H I E R A R C H Y

STEP 2: PARTITIONING (2)

The cutting is guided by:

1 – REGULARITY OR NOT

- ✓ Identify regular blocks
- ✓ Identify random logic blocks

STEP 2: PARTITIONING (3)

The cutting is guided by:

2 – TIMING ASPECTS

- ✓ Coarse Estimation of Timing
- ✓ Looking for a Good Balance

STEP 2: PARTITIONING (4)

The cutting is guided by:

3 – TOPOLOGY

✓ Already in mind the circuit form

✓ An idea about the size of each part

✓ An idea about the routing

✓ Optimizing silicon area usage

STEP 2: PARTITIONING (5)

The cutting is guided by:

4 – TECHNOLOGY

- ✓ Using GAAS or CMOS ?
- ✓ Using PALs or Standard Cells ?

STEP 2: PARTITIONING (6)

The cutting is guided by:

5 – CAD TOOLS

✓ What tools do I have to make my circuit ?

STEP 3: IMPLEMENTATION

EACH PART WILL BE IMPLEMENTED USING A PARTICULAR METHOD. WHEN I SPLIT MY CIRCUIT, I ALREADY HAVE DECIDED WHICH ONE

STEP 4: ASSEMBLAGE

THE ASSEMBLAGE IS DONE IN A HIERARCHICAL WAY, STARTING FROM THE LOWEST LEVEL

CONCLUSION (1)

At each step, the information is enhanced:

1. From the idea down to the specifications
2. When structuring the model in an other way
3. .....

➡ At each step, a verification is to be done

CONCLUSION (2)

All along the methodology, we handled different views:

1 – EQUATIONS

2– NETLISTS

3– LAYOUT

CONCLUSION (3)