

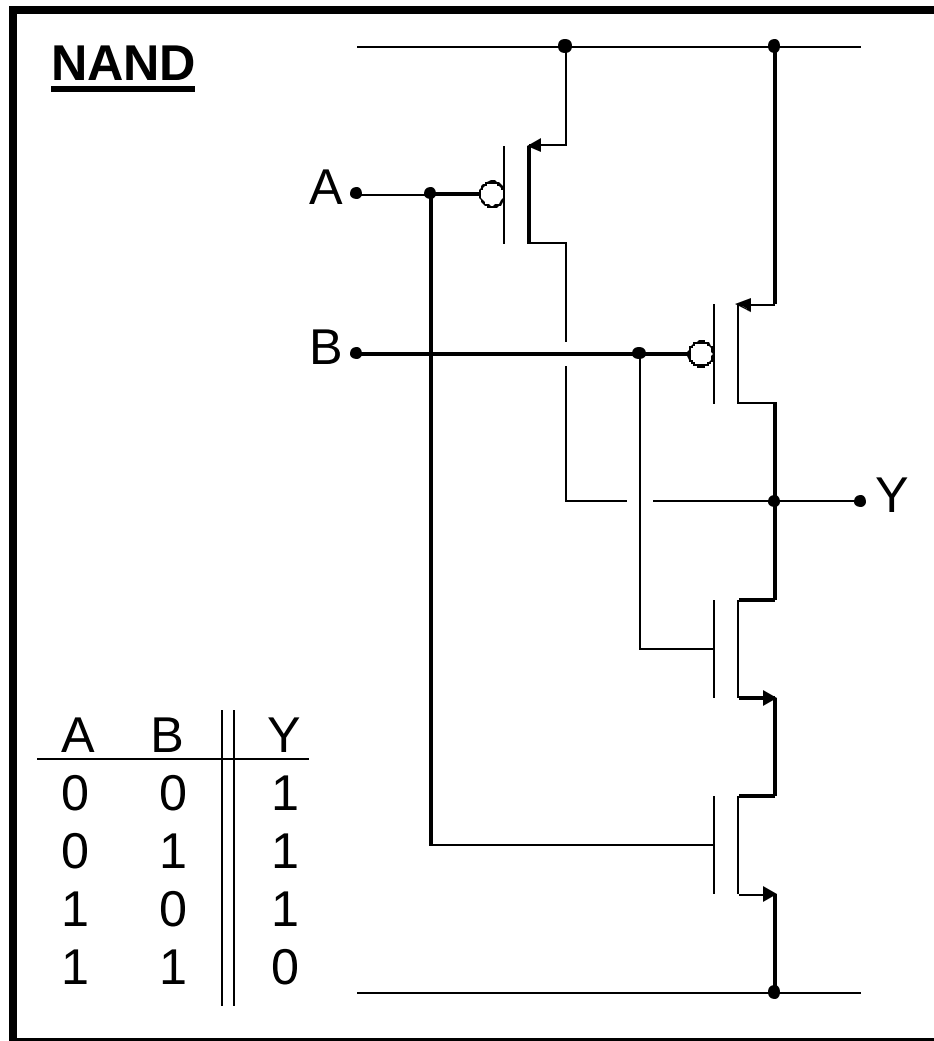
Outline

- Introduction – *“Is there a limit?”*
- Transistors – *“CMOS building blocks”*
- Parasitics I – *“The [un]desirables”*
- Parasitics II – *“Building a full MOS model”*
- The CMOS inverter – *“A masterpiece”*
- Technology scaling – *“Smaller, Faster and Cooler”*
- Technology – *“Building an inverter”*
- **Gates I – *“Just like LEGO”***
- The pass gate – *“An useful complement”*
- Gates II – *“A portfolio”*
- Sequential circuits – *“Time also counts!”*
- DLLs and PLLs – *“A brief introduction”*
- Storage elements – *“A bit in memory”*

“Just like LEGO”

- The NAND gate
- “Reading” CMOS gates
- Designing CMOS gates

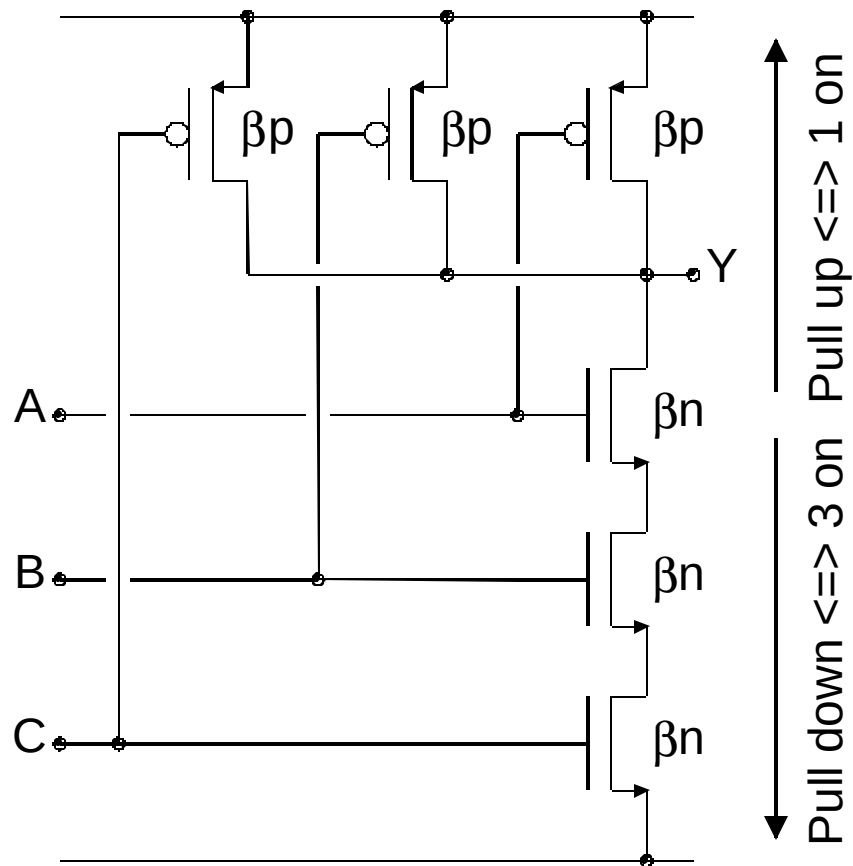
NAND 2-inputs



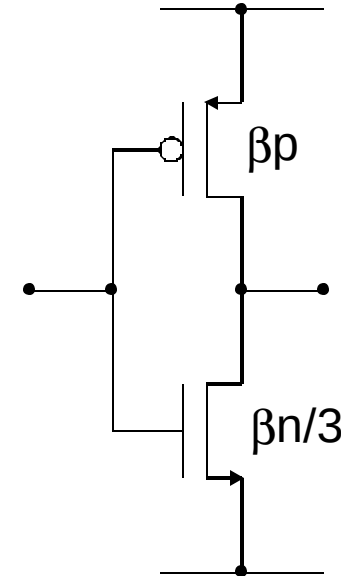
“Gates are
inverters in
disguise!”

NAND 3-inputs

NAND 3 inputs

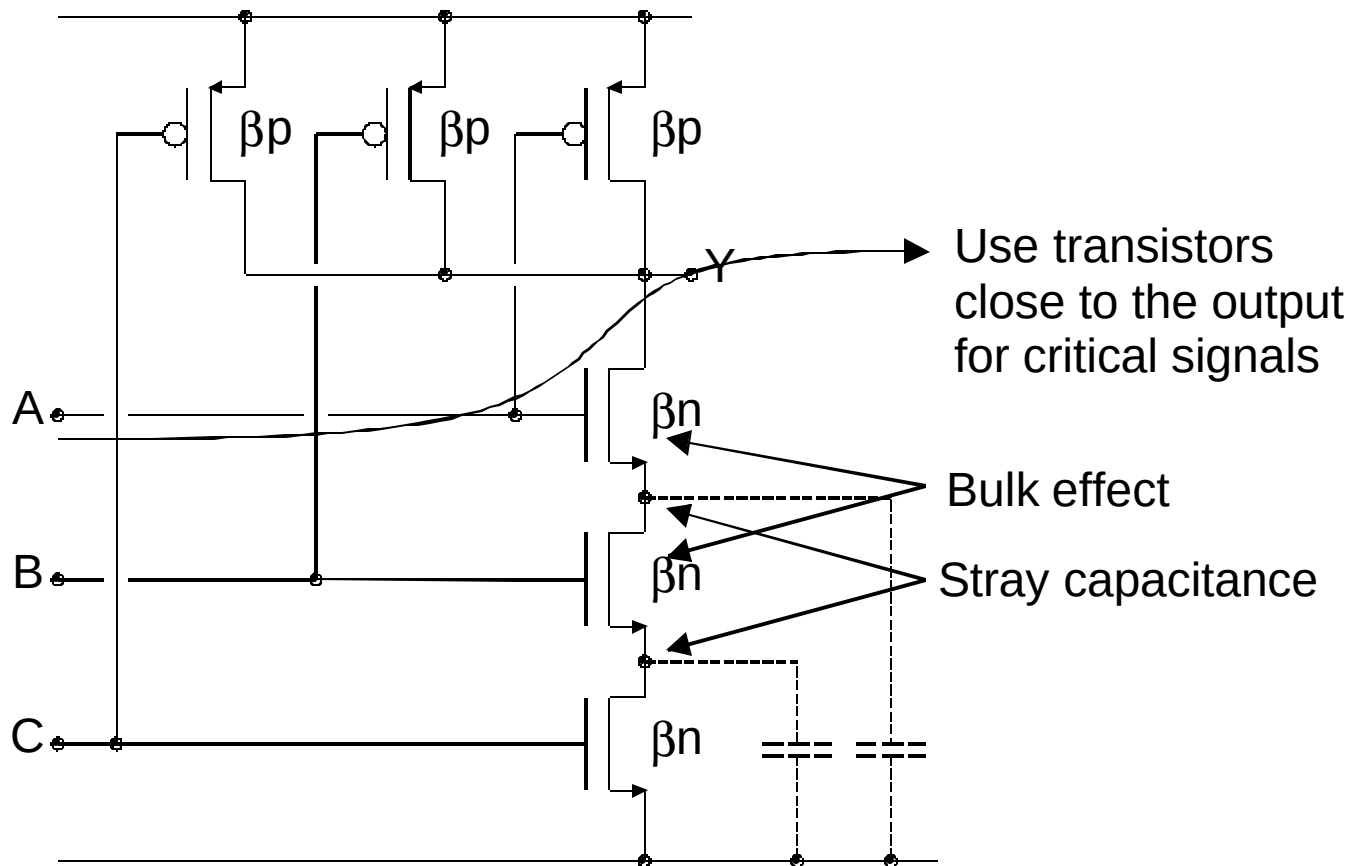


"Delay equivalent" inverter

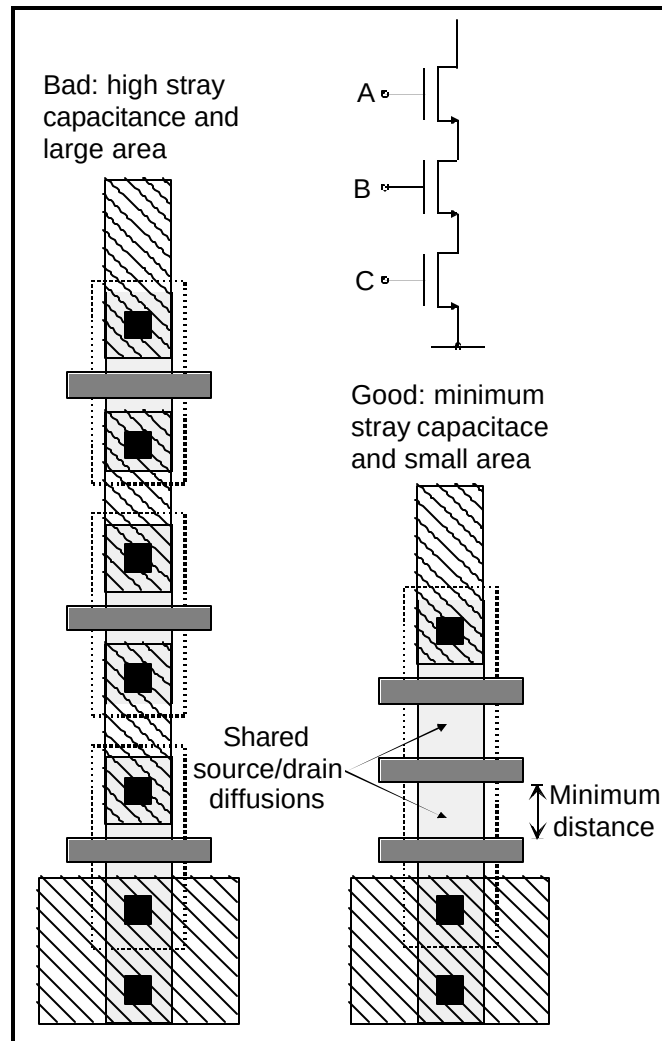


NAND 3-inputs

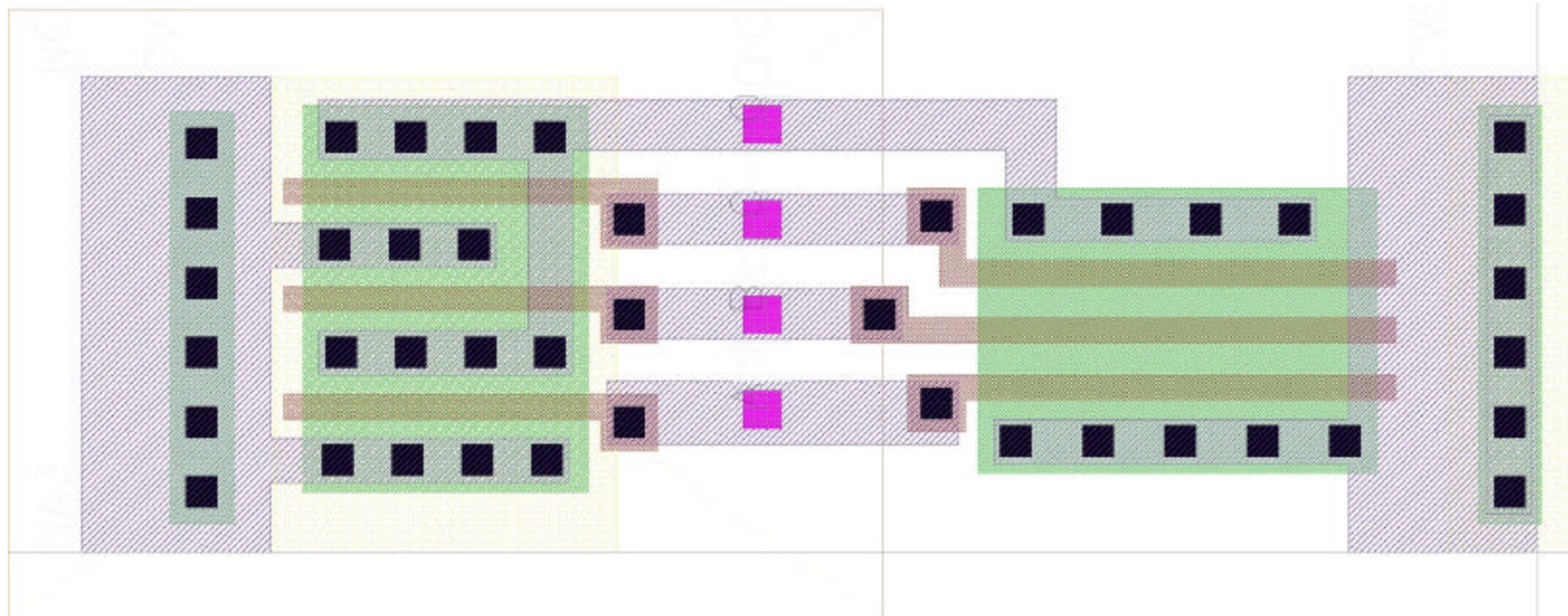
NAND 3 inputs



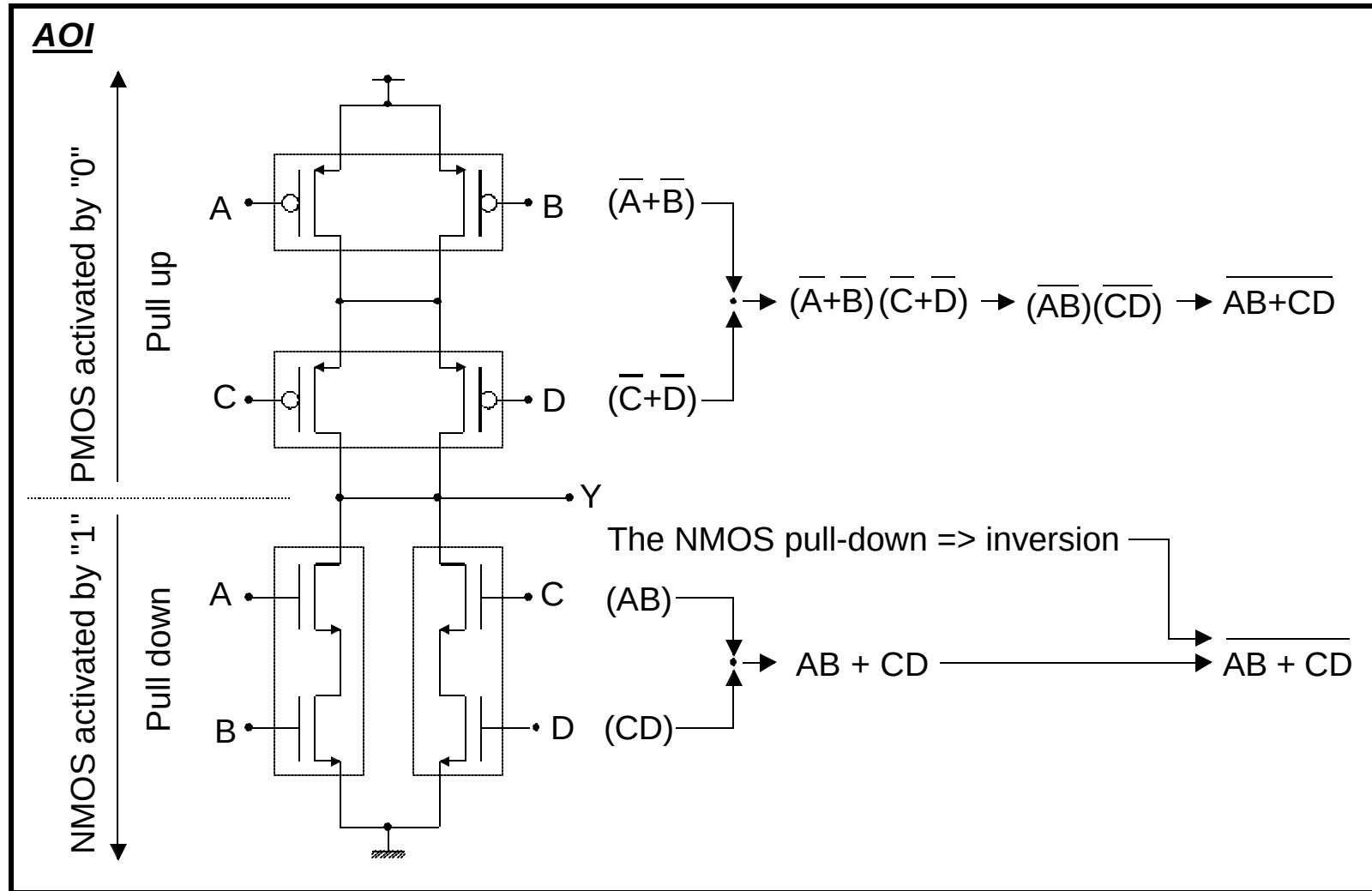
NAND 3-inputs



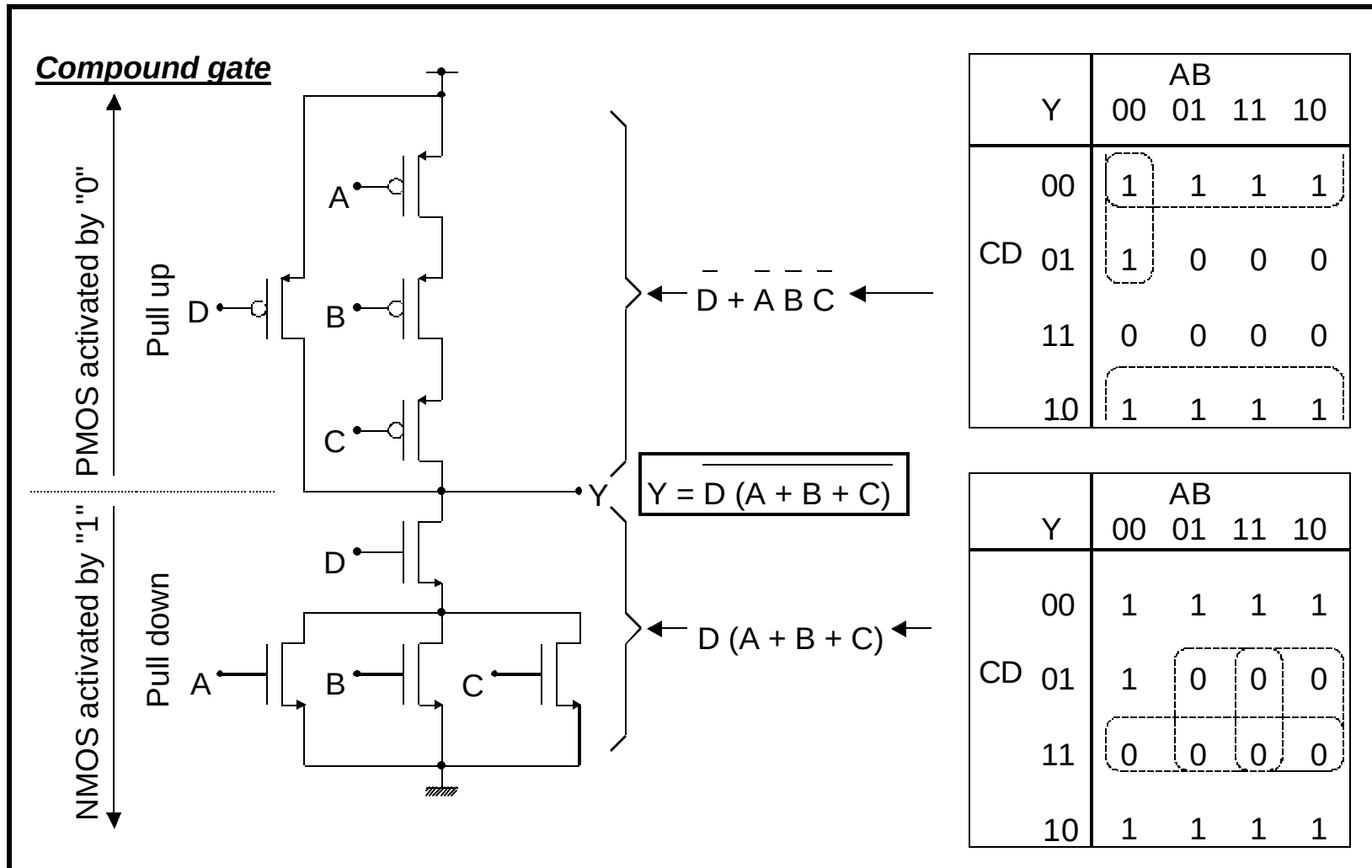
NAND 3-inputs



“Reading” CMOS gates



Designing CMOS gates



Complex CMOS gates

- Can a compound gate be arbitrarily complex?
 - NO, propagation delay is a strong function of fan-in:
$$t_p = a_0 \cdot FO + a_1 \cdot FI + a_2 \cdot (FI)^2$$
 - FO $\Rightarrow$ Fan-out, number of loads connected to the gate:
 - 2 gate capacitances per FO + interconnect
 - FI $\Rightarrow$ Fan-in, Number of inputs in the gate:
 - Quadratic dependency on FI due to:
 - Resistance increase
 - Capacitance increase
 - Avoid large FI gates (Typically $FI \leq 4$)