

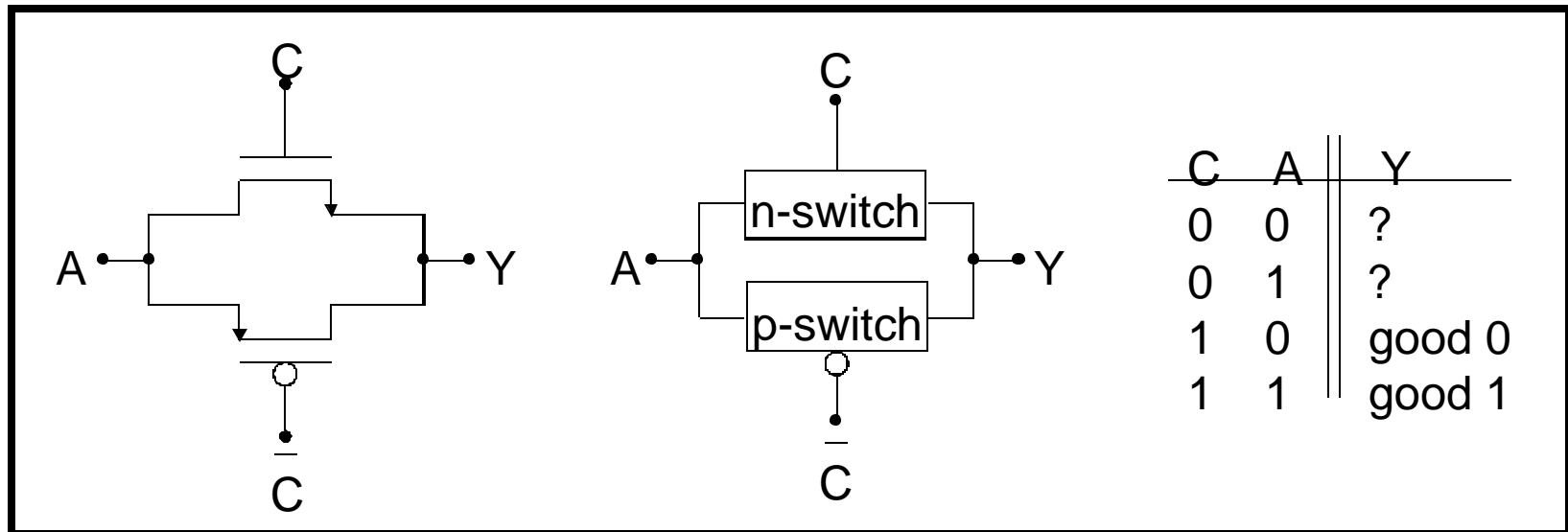
Outline

- Introduction – *“Is there a limit?”*
- Transistors – *“CMOS building blocks”*
- Parasitics I – *“The [un]desirables”*
- Parasitics II – *“Building a full MOS model”*
- The CMOS inverter – *“A masterpiece”*
- Technology scaling – *“Smaller, Faster and Cooler”*
- Technology – *“Building an inverter”*
- Gates I – *“Just like LEGO”*
- **The pass gate – *“An useful complement”***
- Gates II – *“A portfolio”*
- Sequential circuits – *“Time also counts!”*
- DLLs and PLLs – *“A brief introduction”*
- Storage elements – *“A bit in memory”*

“An useful complement”

- The pass gate switch
- Regions of operation
- Pass gate delay

The CMOS pass gate



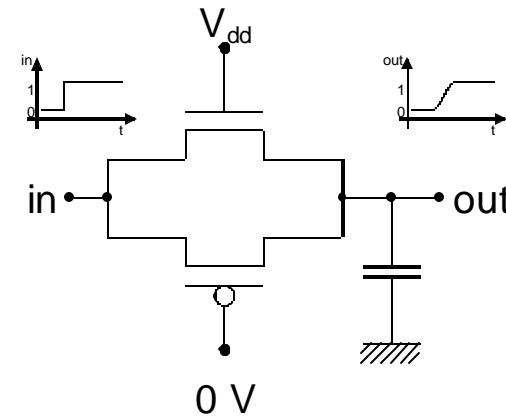
The CMOS pass gate

Regions of operation:

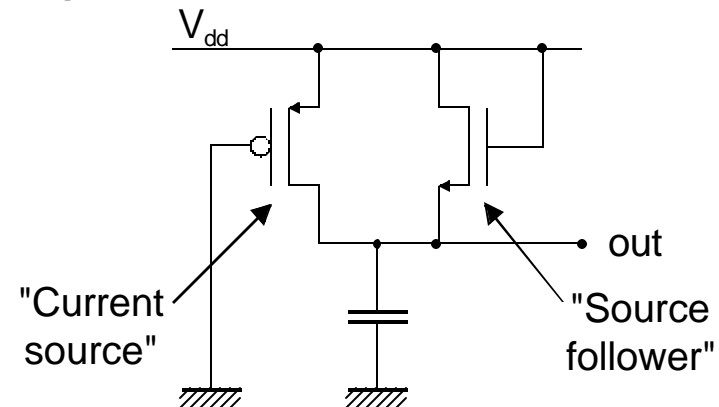
“0” to “1” transition

- NMOS:
 - source follower
 - $V_{gs} = V_{ds}$ always:
 - $V_{out} < V_{dd} - V_{TN} \Rightarrow$ saturation
 - $V_{out} > V_{dd} - V_{TN} \Rightarrow$ cutoff
 - $V_{TN} > V_{TN0}$ (bulk effect)
- PMOS:
 - current source
 - $V_{out} < |V_{TP}| \Rightarrow$ saturation
 - $V_{out} > V_{TP} \Rightarrow$ linear

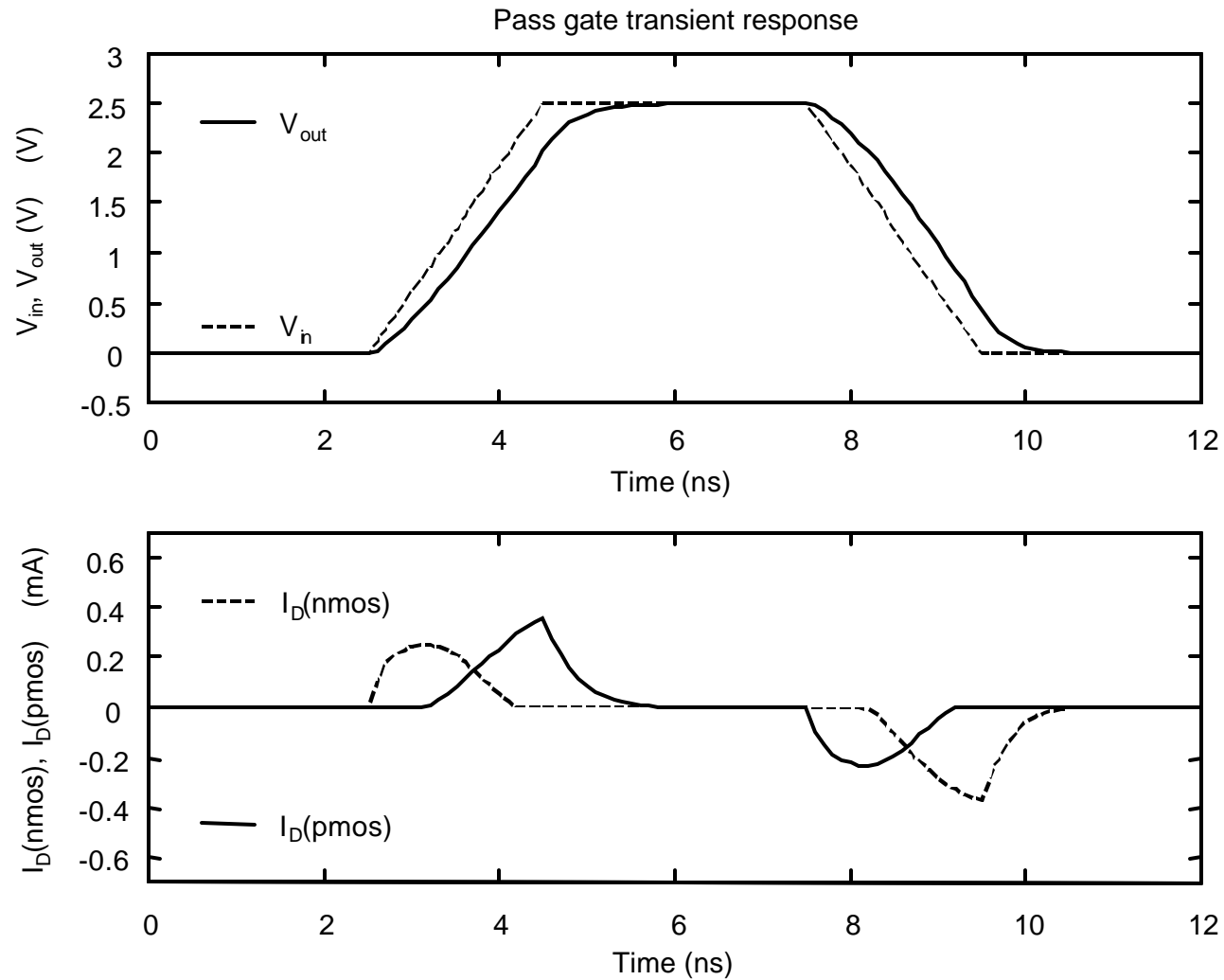
Pass gate: 0 \Rightarrow 1 transition



Equivalent for 0 \Rightarrow 1 transition



The CMOS pass gate



The CMOS pass gate

- Regions of operation: “0” to “1” transition

$V_{\text{out}} < V_{\text{TP}} $	NMOS and PMOS saturated
$ V_{\text{TP}} < V_{\text{out}} < V_{\text{dd}} - V_{\text{TN}}$	NMOS saturated, PMOS linear
$V_{\text{out}} > V_{\text{dd}} - V_{\text{TN}}$	NMOS cutoff, PMOS linear

- Regions of operation: “1” to “0” transition

$V_{\text{out}} > V_{\text{dd}} - V_{\text{TN}}$	NMOS and PMOS saturated
$V_{\text{dd}} - V_{\text{TN}} > V_{\text{out}} > V_{\text{TP}} $	NMOS linear, PMOS saturated
$V_{\text{TP}} > V_{\text{out}}$	NMOS linear, PMOS cutoff

- Both devices combine to form a good switch

The CMOS pass gate

- Delay of a chain of pass gates:

$$t_d \propto C \cdot R_{eq} \cdot \frac{N \cdot (N + 1)}{2}$$

- Delay proportional to N^2
- Avoid N large:
 - Break the chain by inserting buffers
- Warning:
 - A pass gate provides no power gain or buffering
 - All the work is done by the previous gate
 - It really looks like a simple switch

