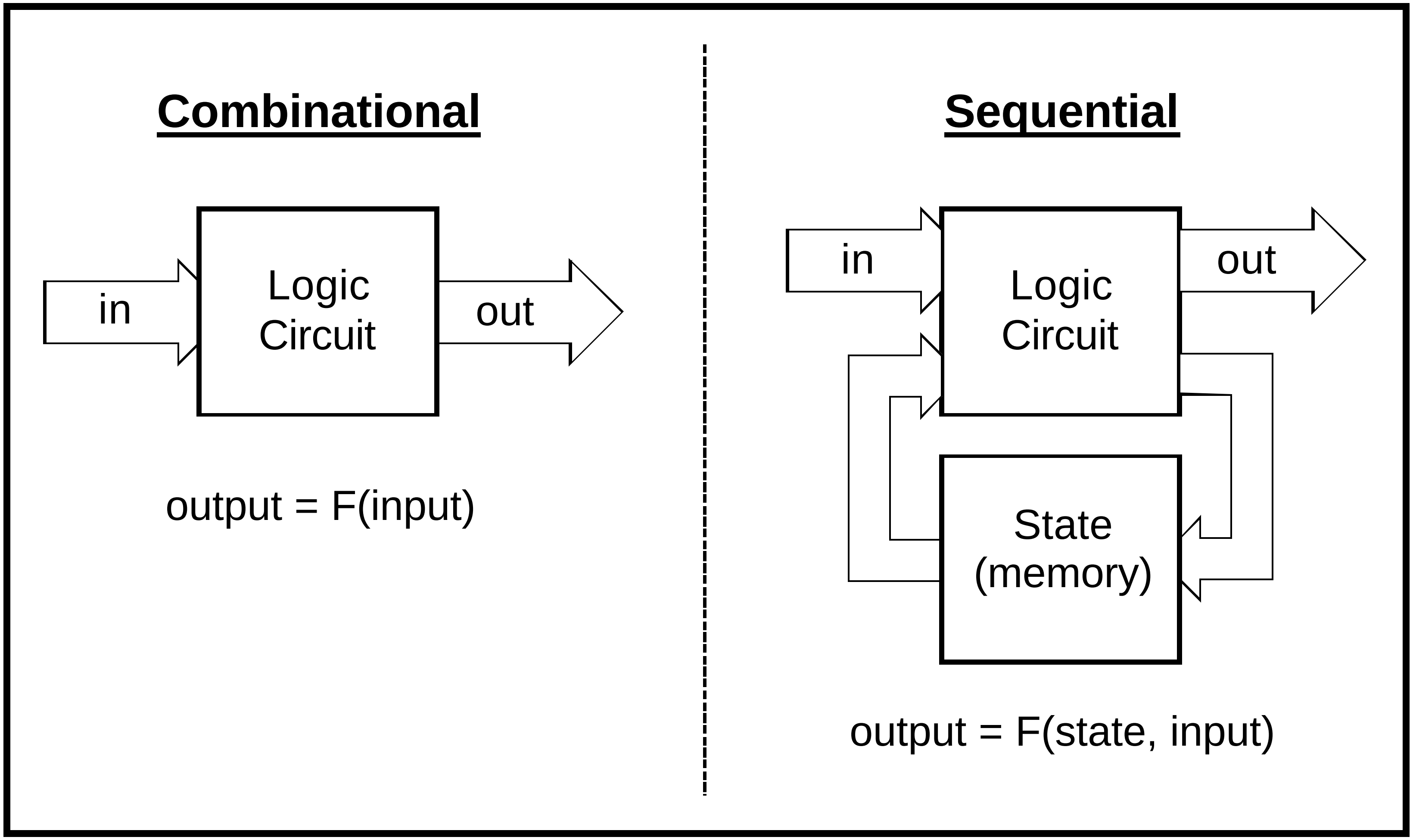
Outline

- Introduction – *"Is there a limit?"*
- Transistors – *"CMOS building blocks"*
- Parasitics I – *"The [un]desirables"*
- Parasitics II – *"Building a full MOS model"*
- The CMOS inverter – *"A masterpiece"*
- Technology scaling – *"Smaller, Faster and Cooler"*
- Technology – *"Building an inverter"*
- Gates I – *"Just like LEGO"*
- The pass gate – *"An useful complement"*
- Gates II – "A portfolio"
- Sequential circuits – *"Time also counts!"*
- DLLs and PLLs – " A brief introduction"
- Storage elements – *"A bit in memory"*

Sequential circuits

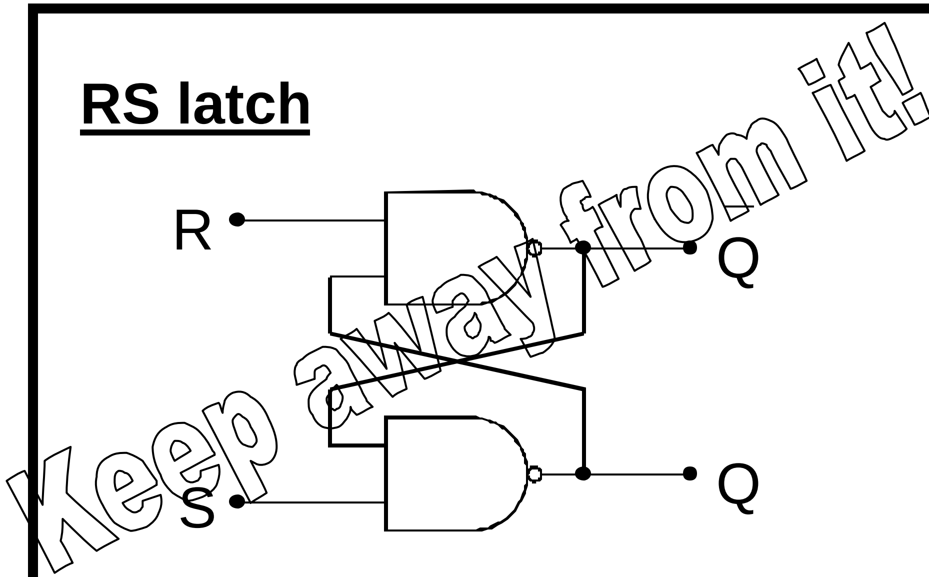
- Time in logic circuits
- “A bad memory”
- Latch 1
- Latch 2
- D flip-flop
- State machine timing
- Interconnects
- Clock distribution

“Time also counts”



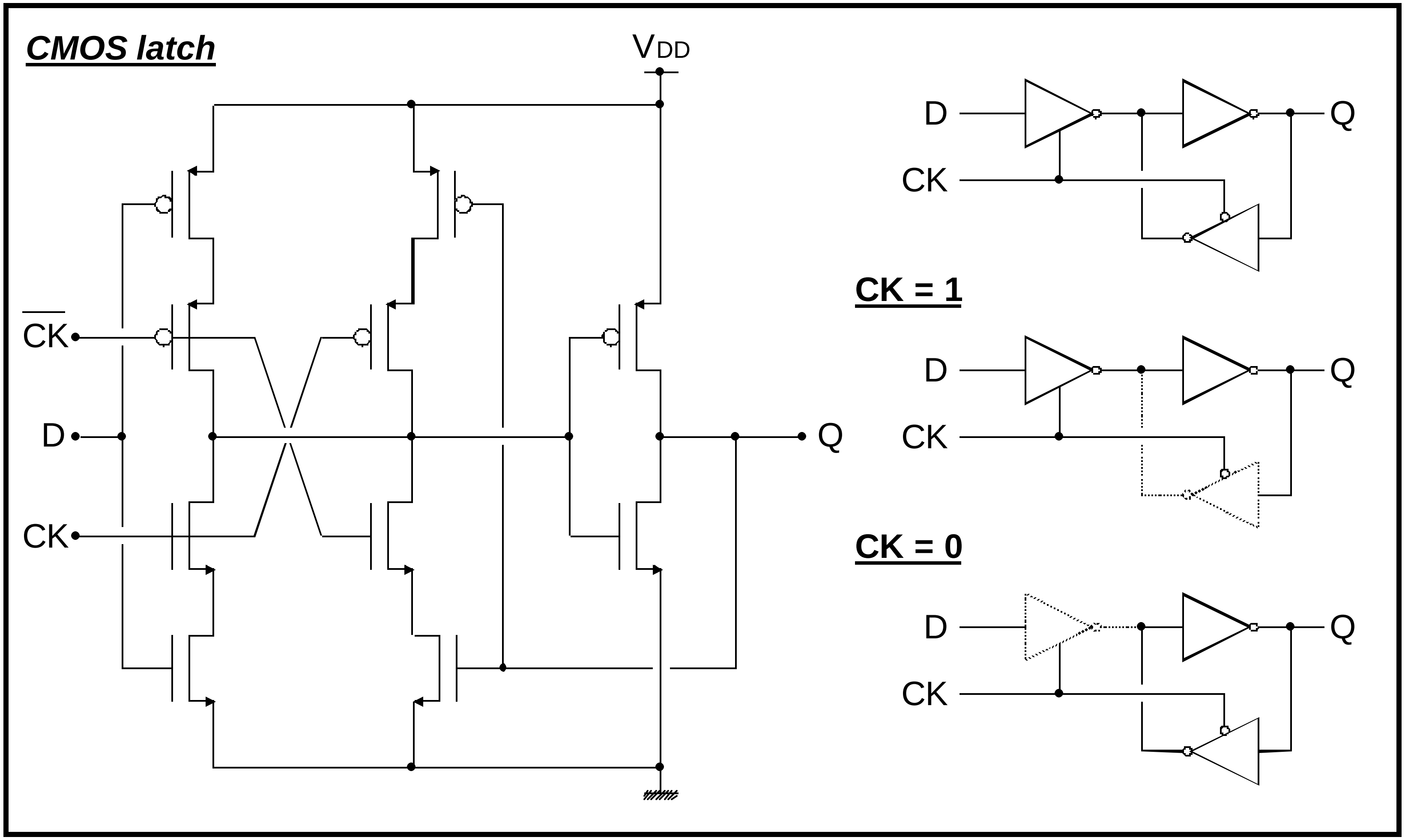
RS Latch – "A bad memory"

RS latch

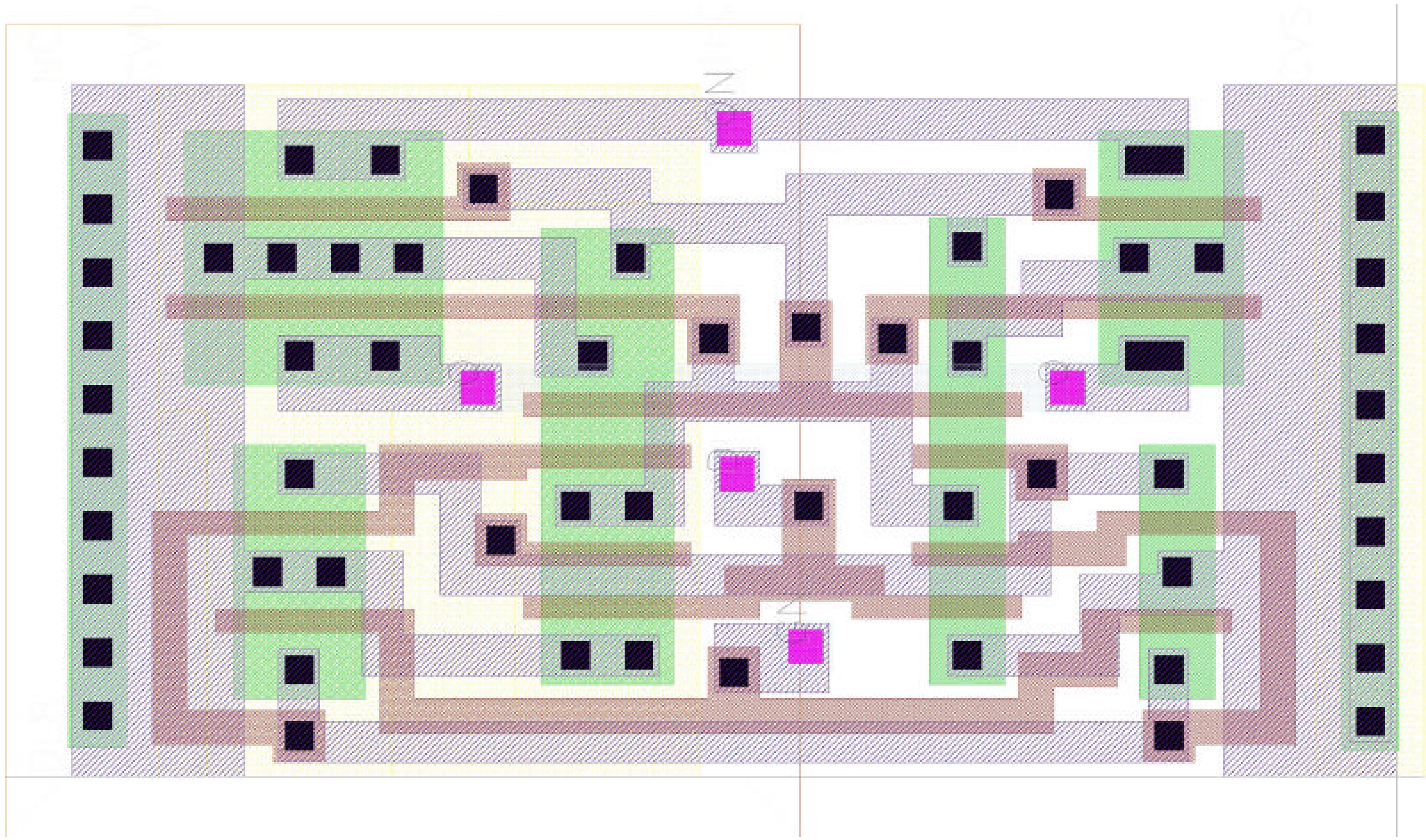


R	S	Q_{n+1}	$\bar{Q}_{n+1}$	
0	0	1	1	(ilegal)
0	1	0	1	
1	0	1	0	
1	1	Q_n	$\bar{Q}_n$	(memory)

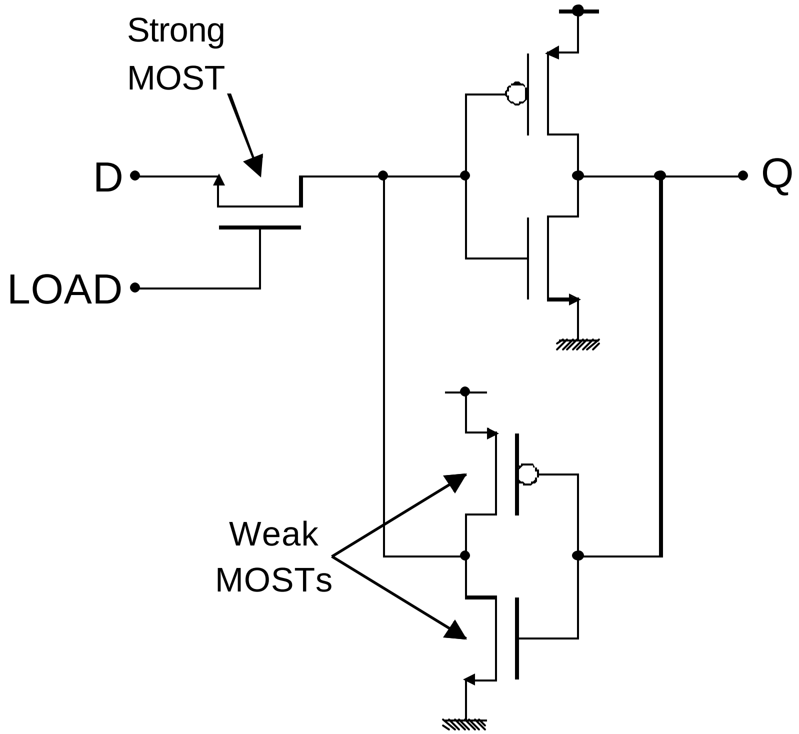
Latch

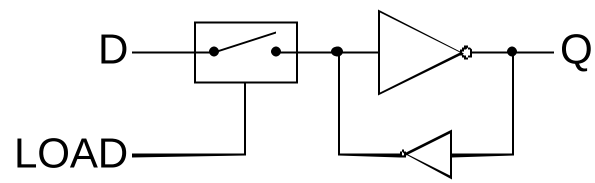


Latch



Latch





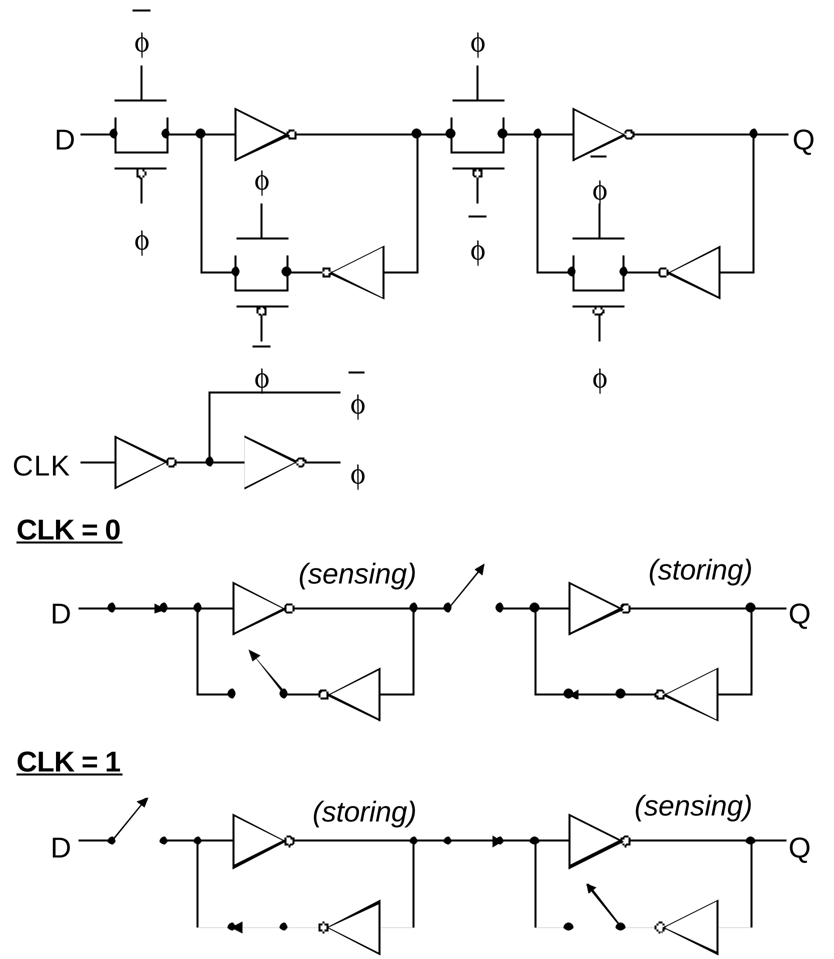
Load = 0 => Hold

Load = 1 => Transparent

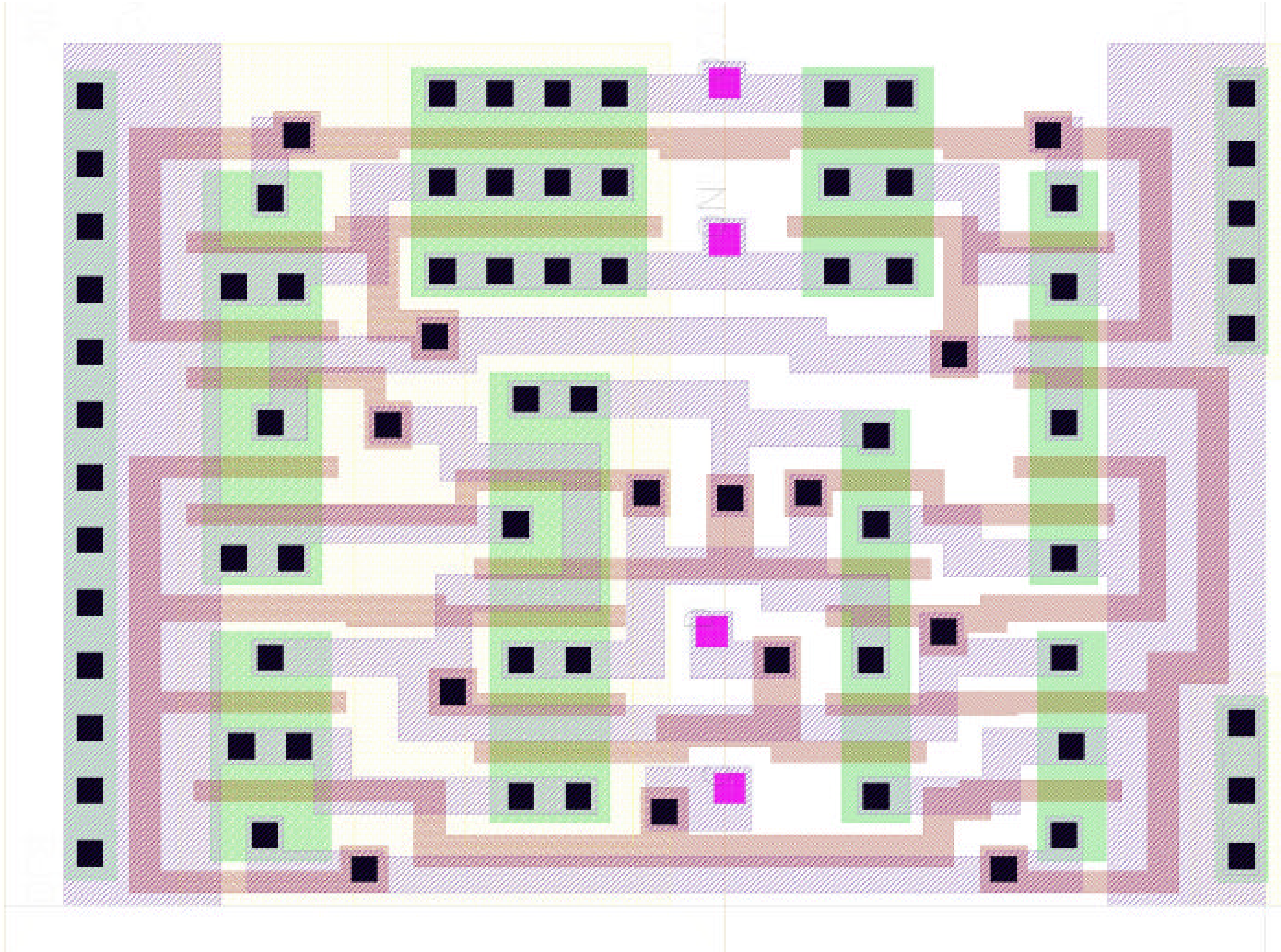
If D = 0, switch = current sink
if D = 1, switch = source follower

D Flip-Flop

Positive edge-triggered flip-flop

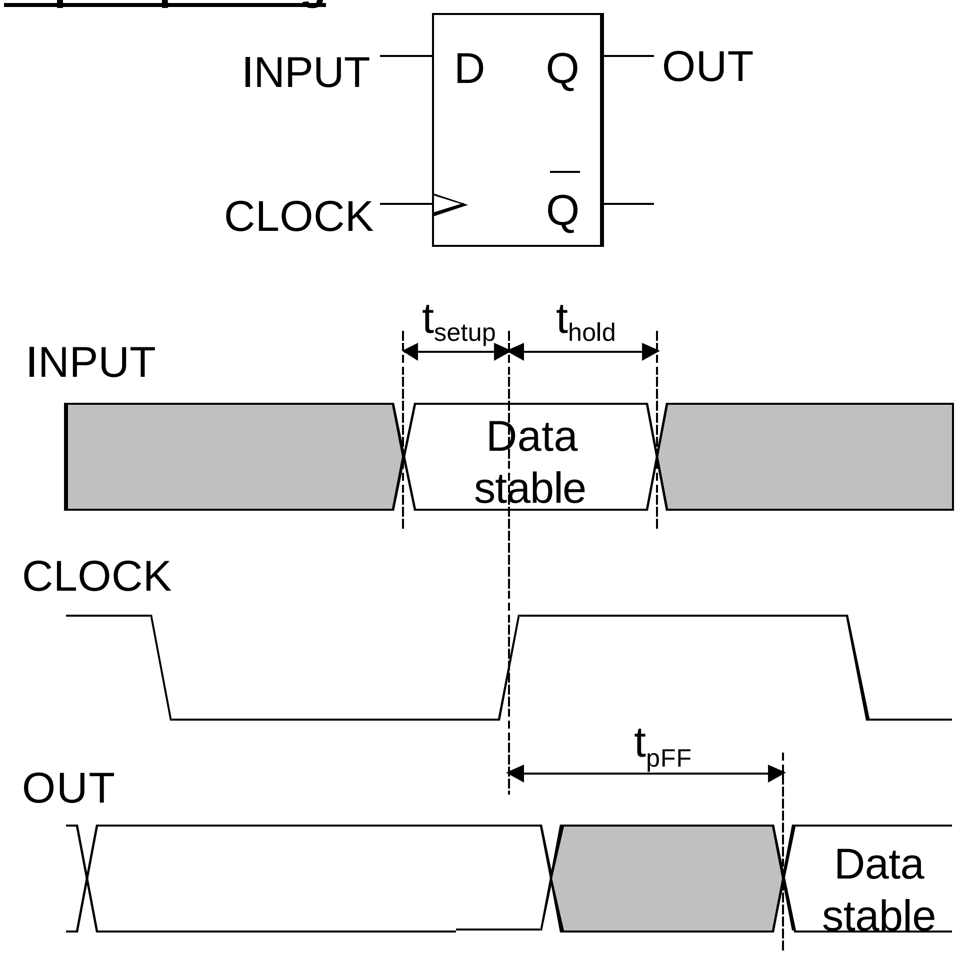


D Flip-Flop



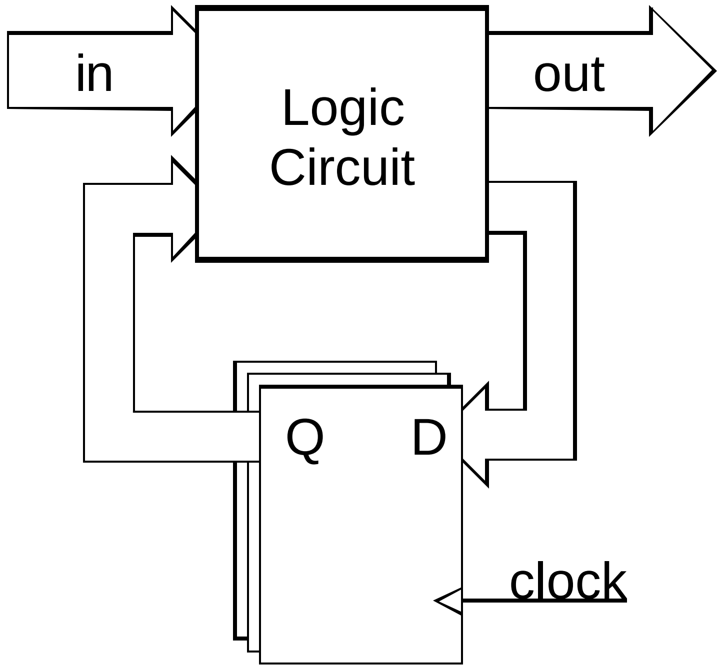
State machine timing

Flip-Flop timing



State machine timing

Maximum clock frequency



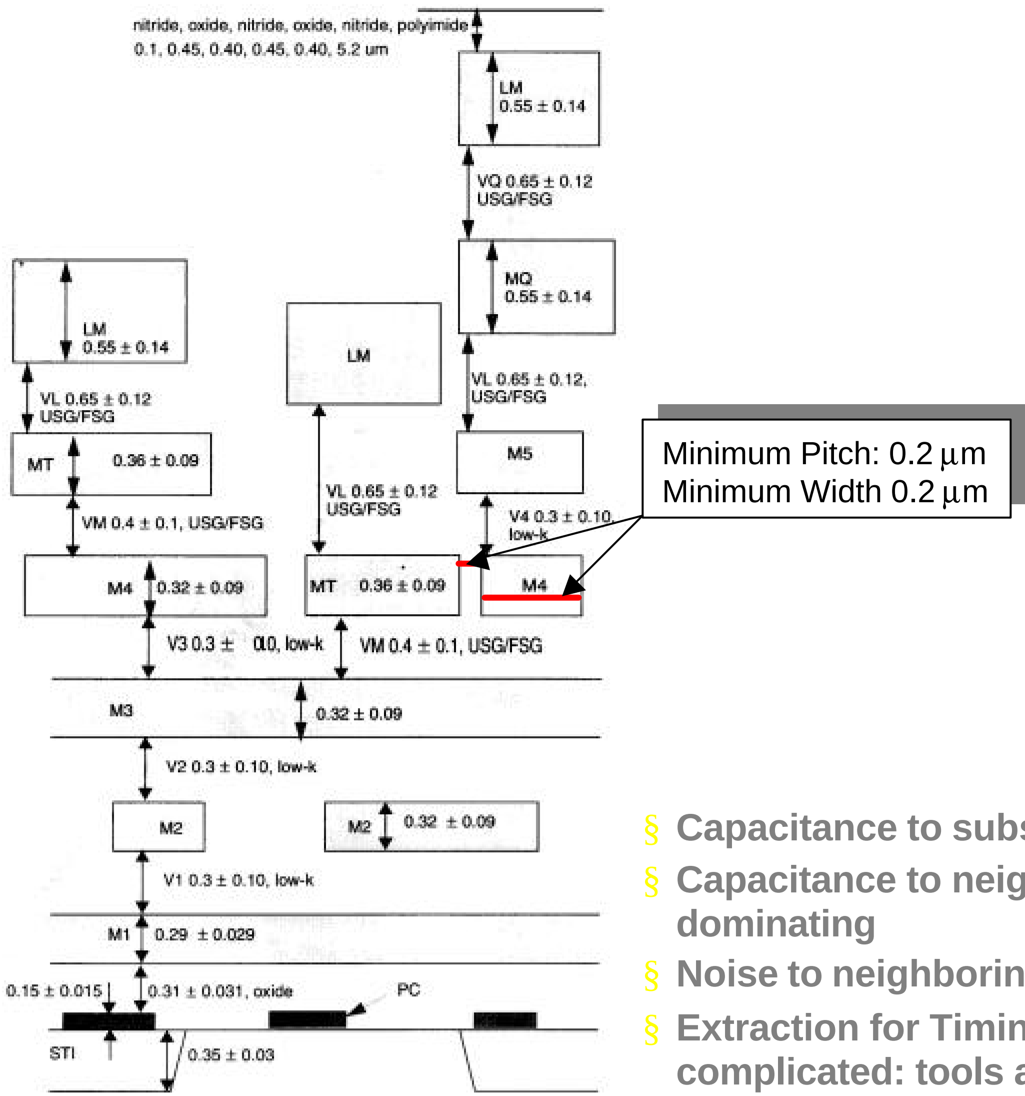
$$T_{min} > t_{pFF} + t_{p,comb} + t_{setup}$$

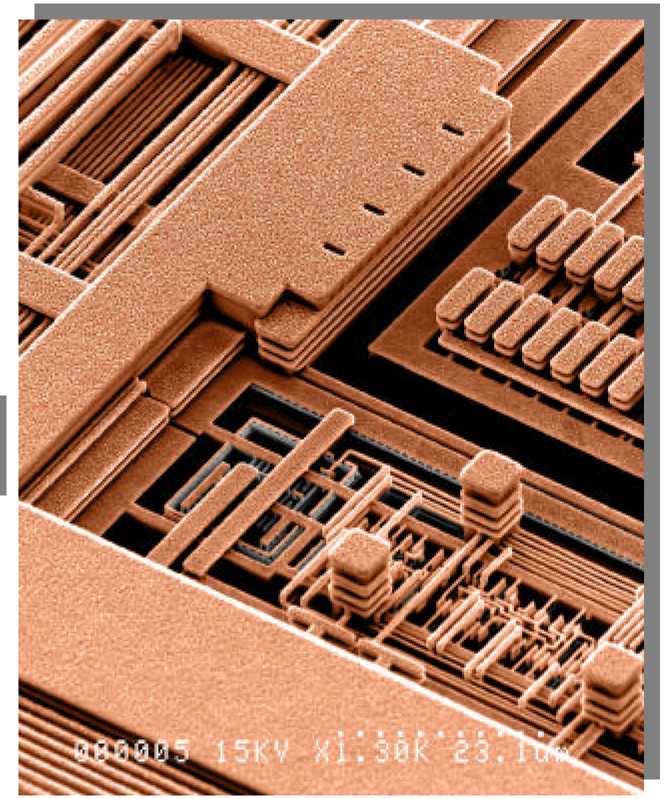
$$f_{max} = 1/T_{min}$$

Interconnects

- The previous result assumes that signals can propagate instantaneously across interconnects
- In reality interconnects are metal or polysilicon structures with associated resistance and capacitance.
- That, introduces signal propagation delay that has to be taken into account for reliable operation of the circuit

Interconnects





- Capacitance to substrate becomes irrelevant
- Capacitance to neighboring signal becomes dominating
- Noise to neighboring signal also not negligible
- Extraction for Timing simulation horribly complicated: tools absolutely mandatory

Interconnects

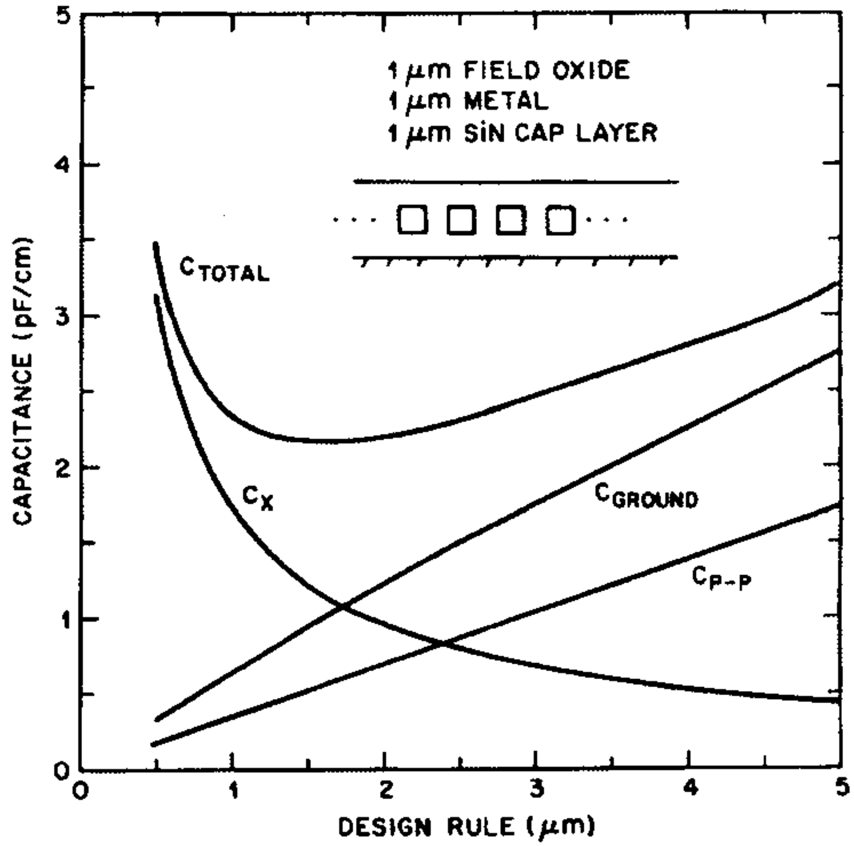
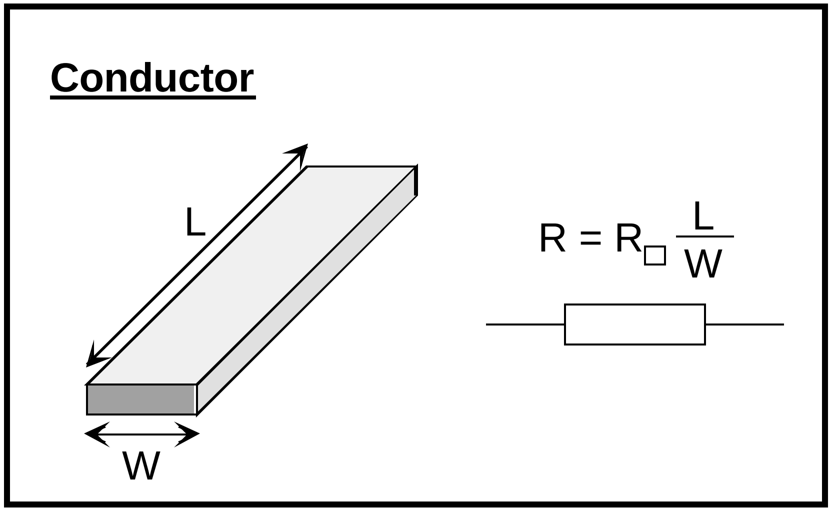


Figure 3.10: Interconnect capacitance including wire-to-wire capacitance [Schaper83]. (© 1983 IEEE)

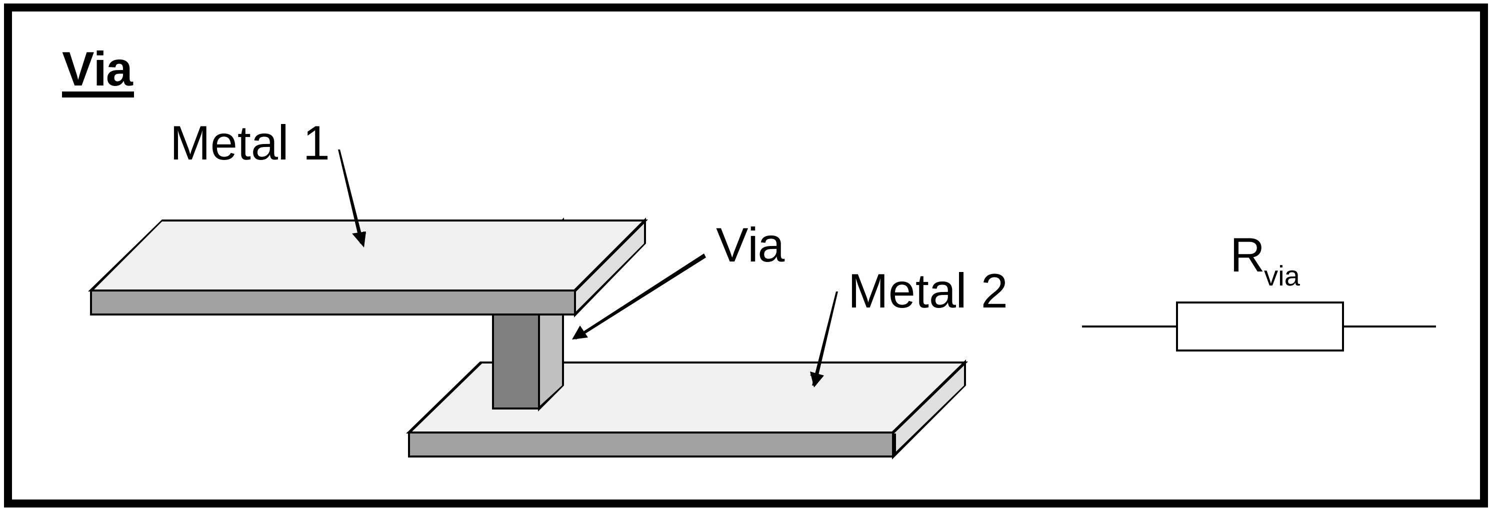
Interconnects



Film	Sheet resistance (Ω/square)
n-well	310
p+, n+ diffusion (salicided)	4
polysilicon (salicided)	4
Metal 1	0.12
Metal 2, 3 and 4	0.09
Metal 5	0.05

(Typical values for an advanced process)

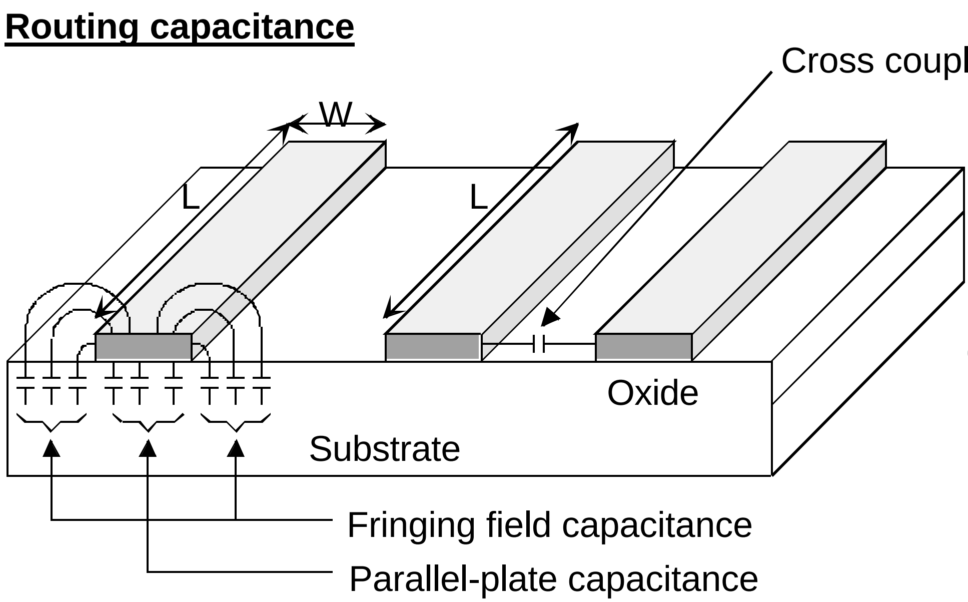
Interconnects



- Via or contact resistance depends on:
  - The contacted materials
  - The contact area

Via/contact	Resistance (Ω)
M1 to n+ or p+	10
M1 to Polysilicon	10
V1, 2, 3 and 4	7

Interconnects

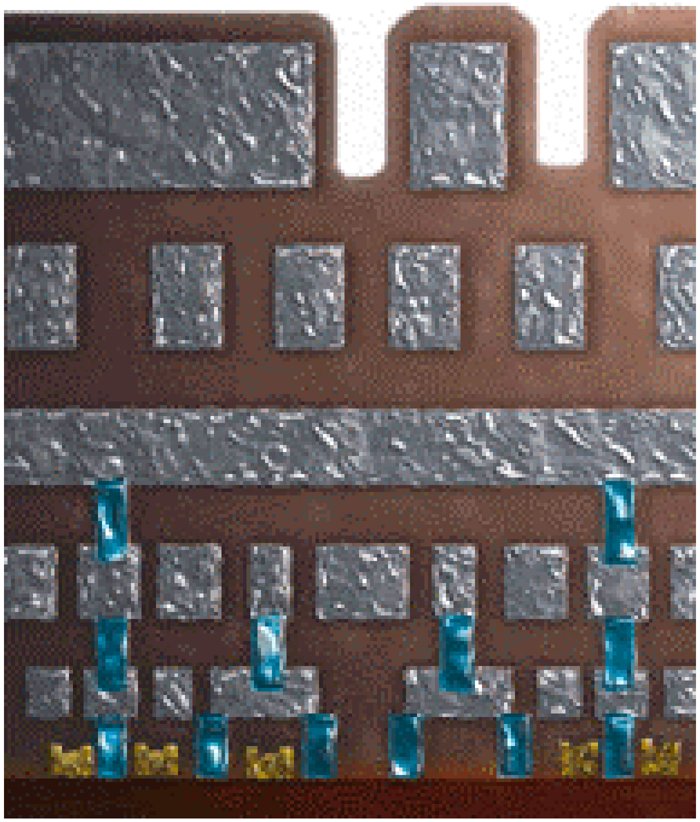


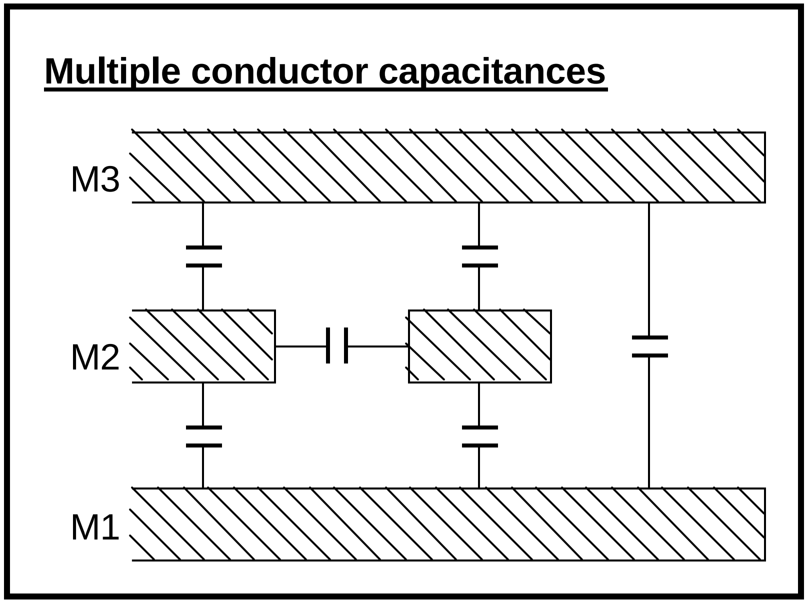
$$C = C_{f0}\,2\,L + C_{p0}\,W\,L$$

$$C_x = C_{x0}\,L$$

Interconnect layer	Parallel-plate (fF/μm²)	Fringing (fF/μm)
Polysilicon to sub.	0.058	0.043
Metal 1 to sub.	0.031	0.044
Metal 2 to sub.	0.015	0.035
Metal 3 to sub.	0.010	0.033

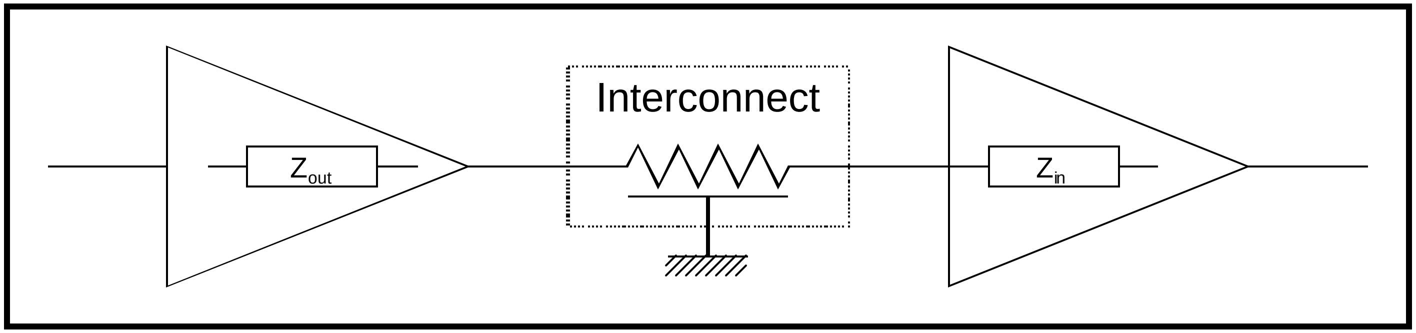
Interconnects





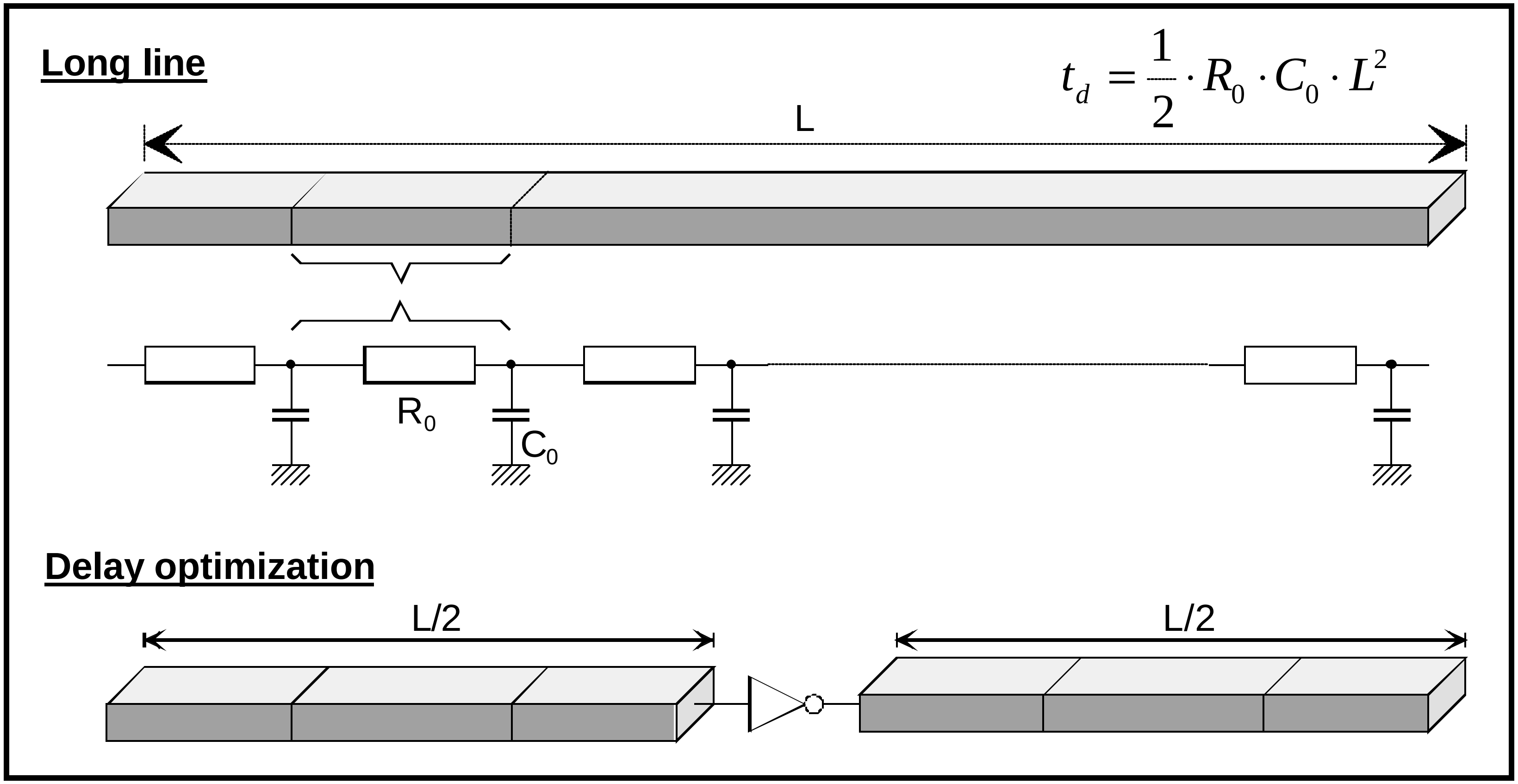
- Three dimensional field simulators are required to accurately compute the capacitance of a multi-wire structure

Interconnects



- Delay depends on:
  - Impedance of the driving source
  - Distributed resistance/capacitance of the wire
  - Load impedance
- Distributed RC delay:
  - Can be dominant in long wires
  - Important in polysilicon wires (relatively high resistance)
  - Important in salicided wires
  - Important in heavily loaded wires

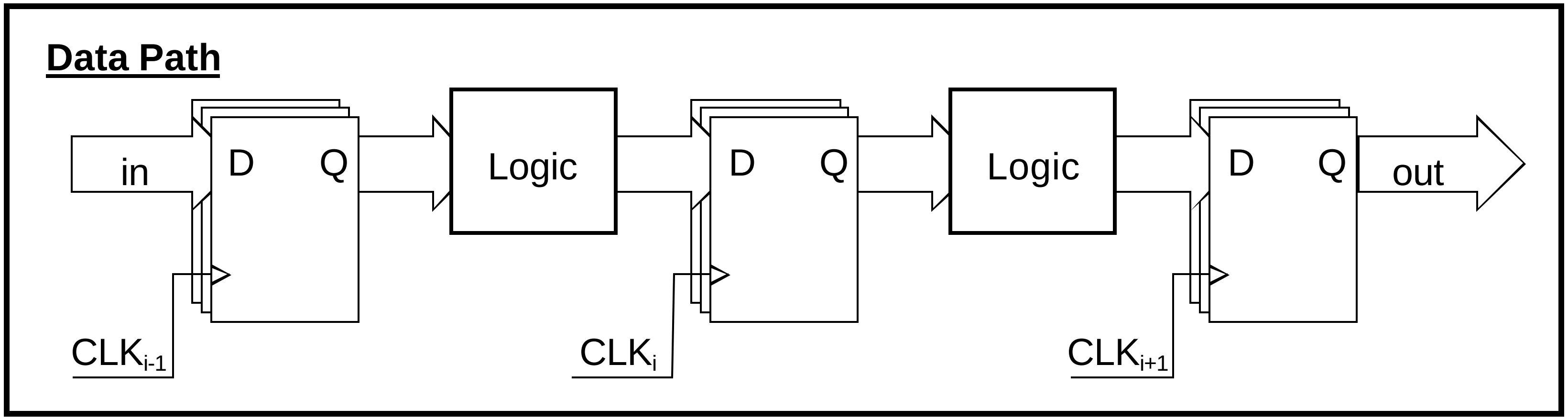
Interconnects



Clock distribution

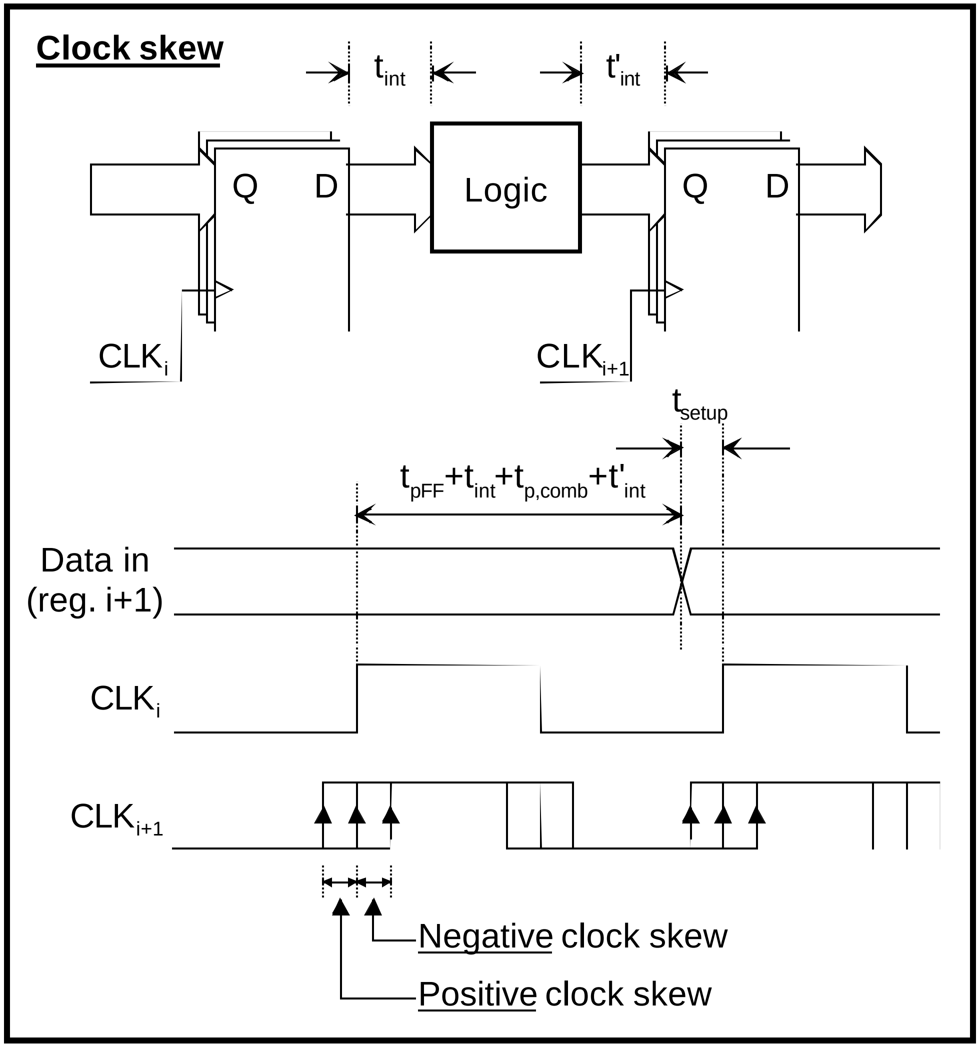
- Clock signals are “special signals”
- Every data movement in a synchronous system is referenced to the clock signal
- Clock signals:
  - Are typically loaded with high fanout
  - Travel over the longest distances in the IC
  - Operate at the highest frequencies

Clock distribution



- "Equipotential" clocking:
  - In a synchronous system all clock signals are derived from a single clock source ("clock reference")
  - Ideally: clocking events should occur at all registers simultaneously … $= t(clk_{i-1}) = t(clk_i) = t(clk_{i+1}) =$ …
  - In practice: clocking events will occur at slightly different instants among the different registers in the data path

Clock distribution



Clock distribution

- Skew: difference between the clocking instants of two "sequential" registers:

  Skew = t(CLK$_i$)- t(CLK$_{i+1}$)

- Maximum operation frequency:

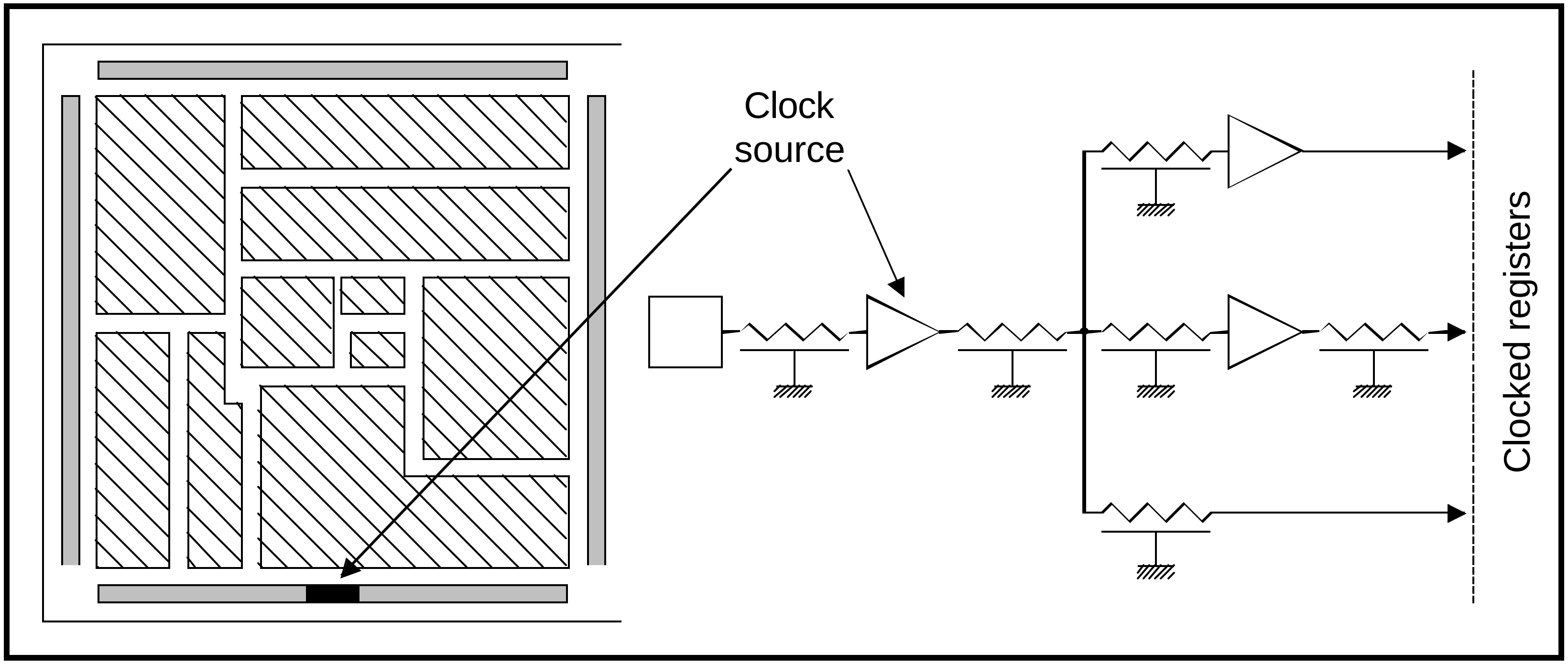
$$T_{\min} = \frac{1}{f_{\max}} = t_{dFF} + t_{\text{int}} + t_{p,comb} + t'_{\text{int}} + t_{setup} + t_{skew}$$

- Skew > 0, decreases the operation frequency
- Skew < 0, can be used to compensate a critical data path <u>BUT</u> this results in more positive skew for the next data path!

Clock distribution

- Different clock paths can have different delays due to:
  - Differences in line lengths from clock source to the clocked registers
  - Differences in delays in the active buffers within the clock distribution network:
    - Differences in passive interconnect parameters (line resistance/capacitance, line dimensions, …)
    - Differences in active device parameters (threshold voltages, channel mobility)
- In a well designed and balanced clock distribution network, the distributed clock buffers are the principal source of clock skew

Clock distribution



- Clock buffers:
  - Amplify the clock signal degraded by the interconnect impedance
  - Isolate the local clock lines from upstream load impedances

Clock distribution