Introduction to VLSI ASIC Design and Technology

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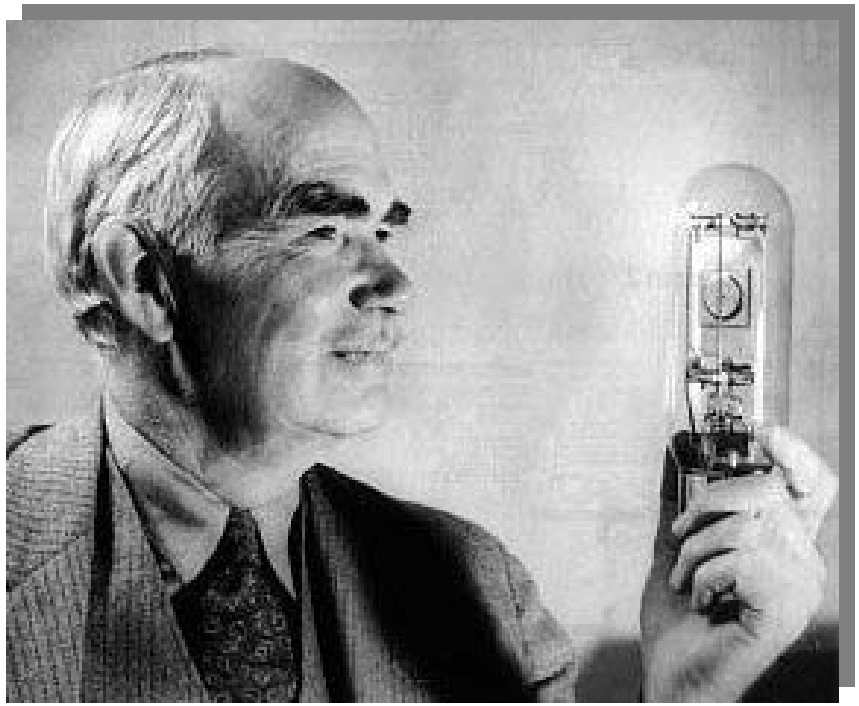
Outline

- Introduction – *"Is there a limit?"*
- Transistors – *"CMOS building blocks"*
- Parasitics I – *"The [un]desirables"*
- Parasitics II – *"Building a full MOS model"*
- The CMOS inverter – *"A masterpiece"*
- Technology scaling – *"Smaller, Faster and Cooler"*
- Technology – *"Building an inverter"*
- Gates I – *"Just like LEGO"*
- The pass gate – *"An useful complement"*
- Gates II – "A portfolio"
- Sequential circuits – *"Time also counts!"*
- DLLs and PLLs – " A brief introduction"
- Storage elements – *"A bit in memory"*

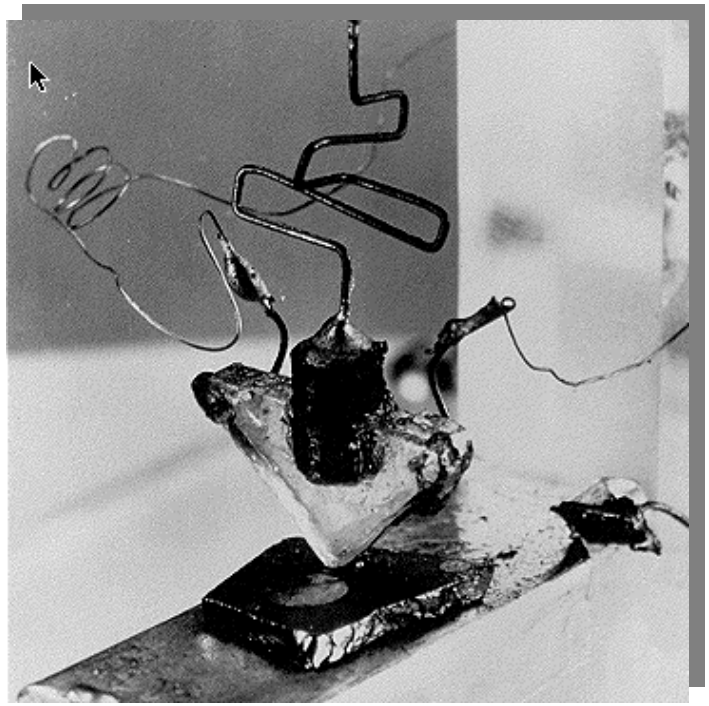
Introduction

1906



Audion (Triode), 1906
Lee De Forest

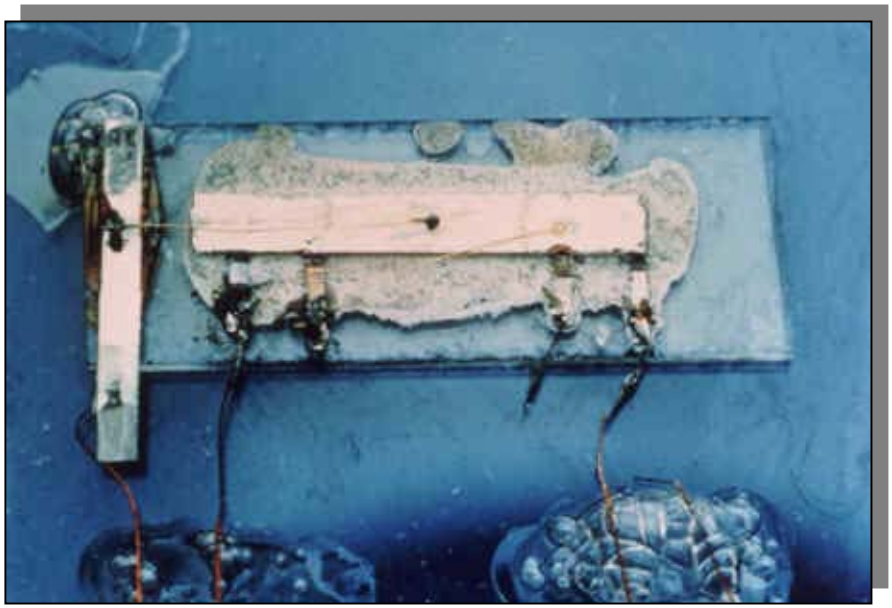
1947



First point contact transistor (germanium), 1947
John Bardeen and Walter Brattain
Bell Laboratories

Introduction

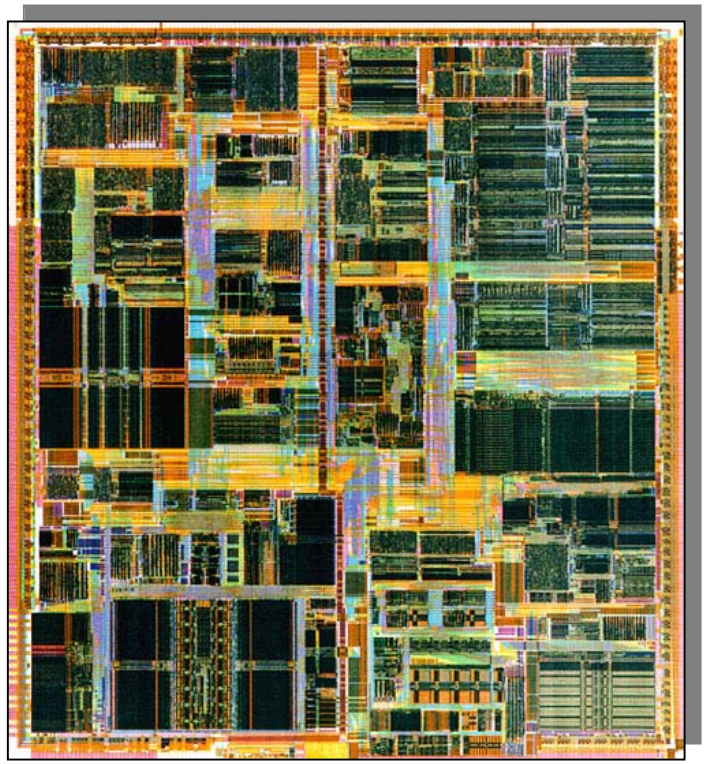
1958



First integrated circuit (germanium), 1958
Jack S. Kilby, Texas Instruments

Contained five components, three types:
transistors resistors and capacitors

1997



Intel Pentium II, 1997
Clock: 233MHz
Number of transistors: 7.5 M
Gate Length: 0.35

“The world is digital…”

- Analogue looses terrain:
  - Computing
  - Instrumentation
  - Control systems
  - Telecommunications
  - Consumer electronics

"…analogue, alive and kicking"

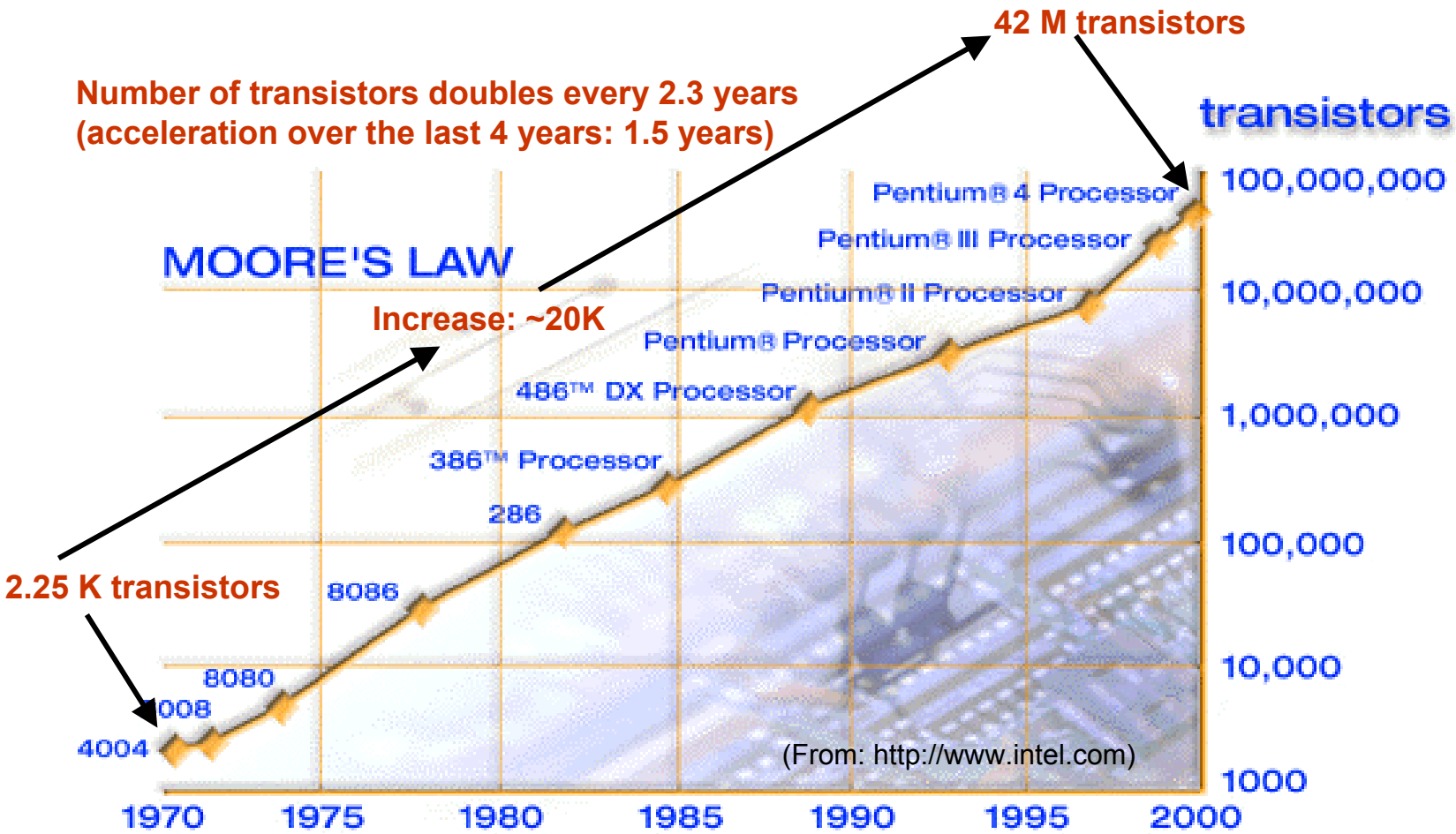
- Amplification of very week signals
- A/D and D/A conversion
- RF communications
- Very high frequency amplification and signal processing
- As digital systems become faster and faster and circuit densities increase:
  - "Analogue" phenomena are becoming important in digital systems

“Moore’s Law”

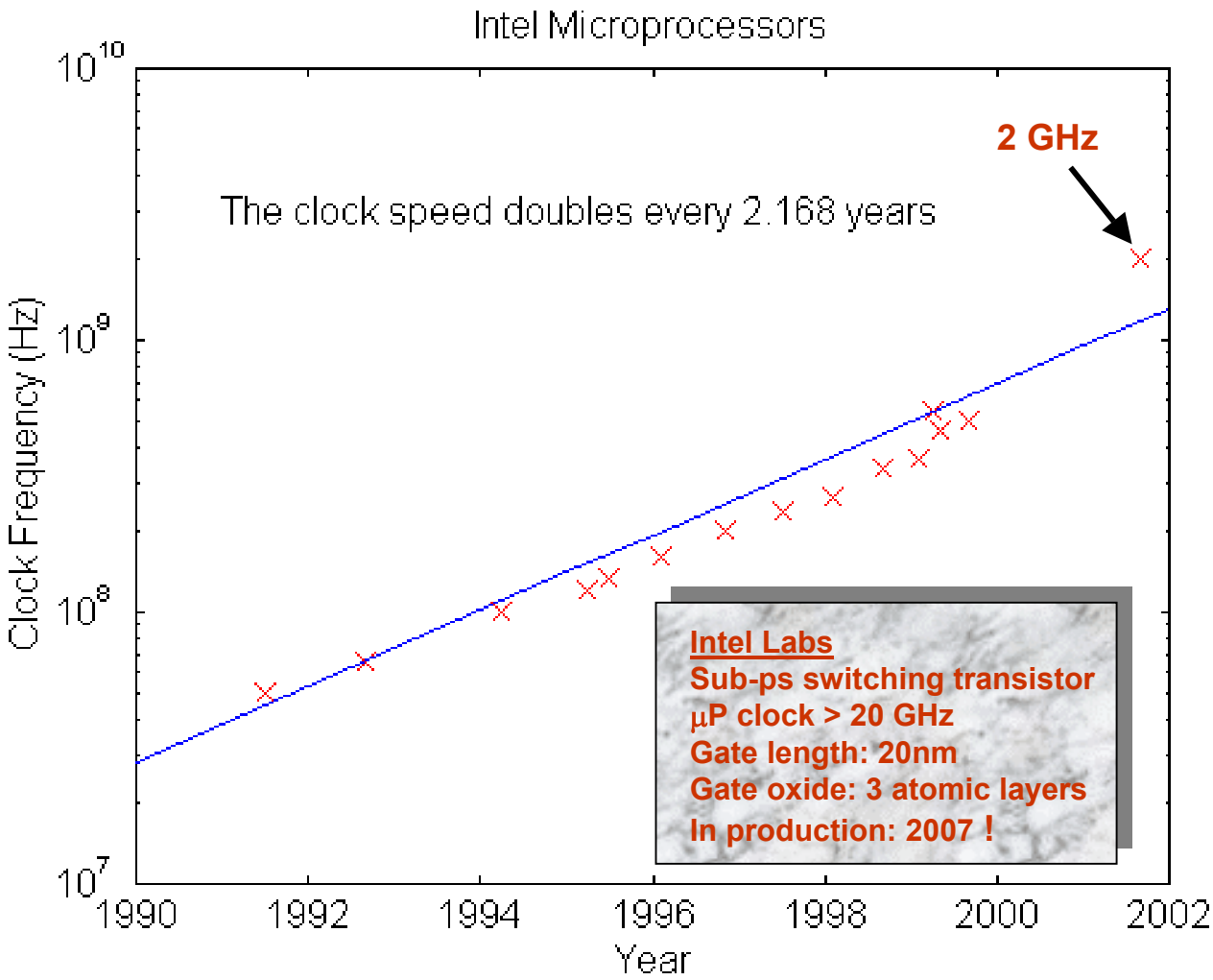
The number of transistors that can be integrated on a single IC grows exponentially with time.

“Integration complexity doubles every three years”
Gordon Moore
Fairchild Corporation - 1965

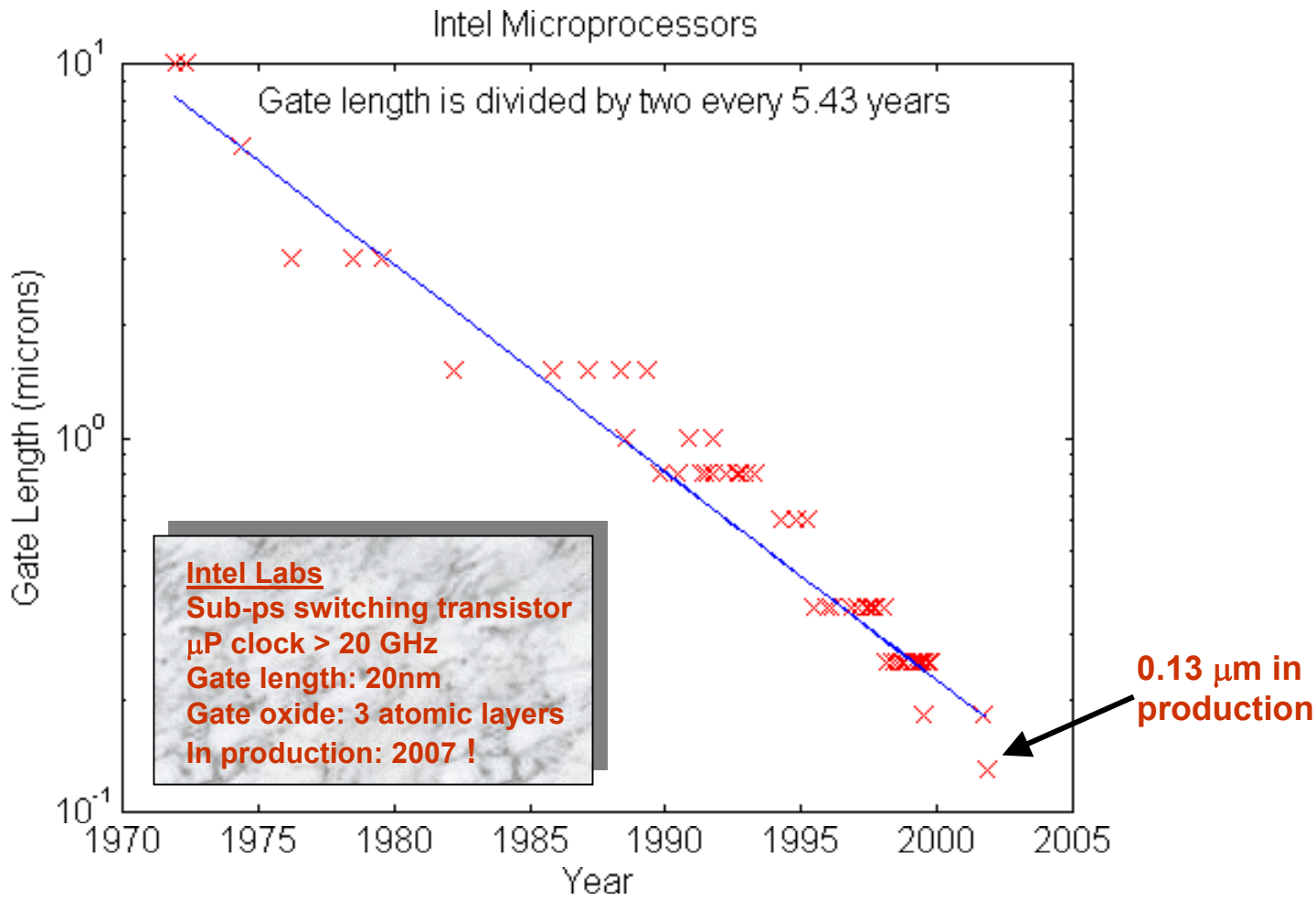
Trends in transistor count



Trends in clock frequency



Trends in feature size



Driving force: Economics (1)

- Traditionally, the cost/function in an IC is reduced by 25% to 30% a year.
- To achieve this, the number of functions/IC has to be increased. This demands for:
  - Increase of the transistor count
  - Decrease of the feature size (*contains the area increase and improves performance*)
  - Increase of the clock speed

Driving force: Economics (2)

- Increase productivity:
  - Increase equipment throughput
  - Increase manufacturing yields
  - Increase the number of chips on a wafer:
    - reduce the area of the chip: smaller feature size & redesign
  - Use the largest wafer size available

Example of a cost effective product (typically DRAM): the initial IC area is reduced to 50% after 3 years and to 35% after 6 years.

2002 and beyond ?

Semiconductor Industry Association (SIA) Road Map, 1998 Update

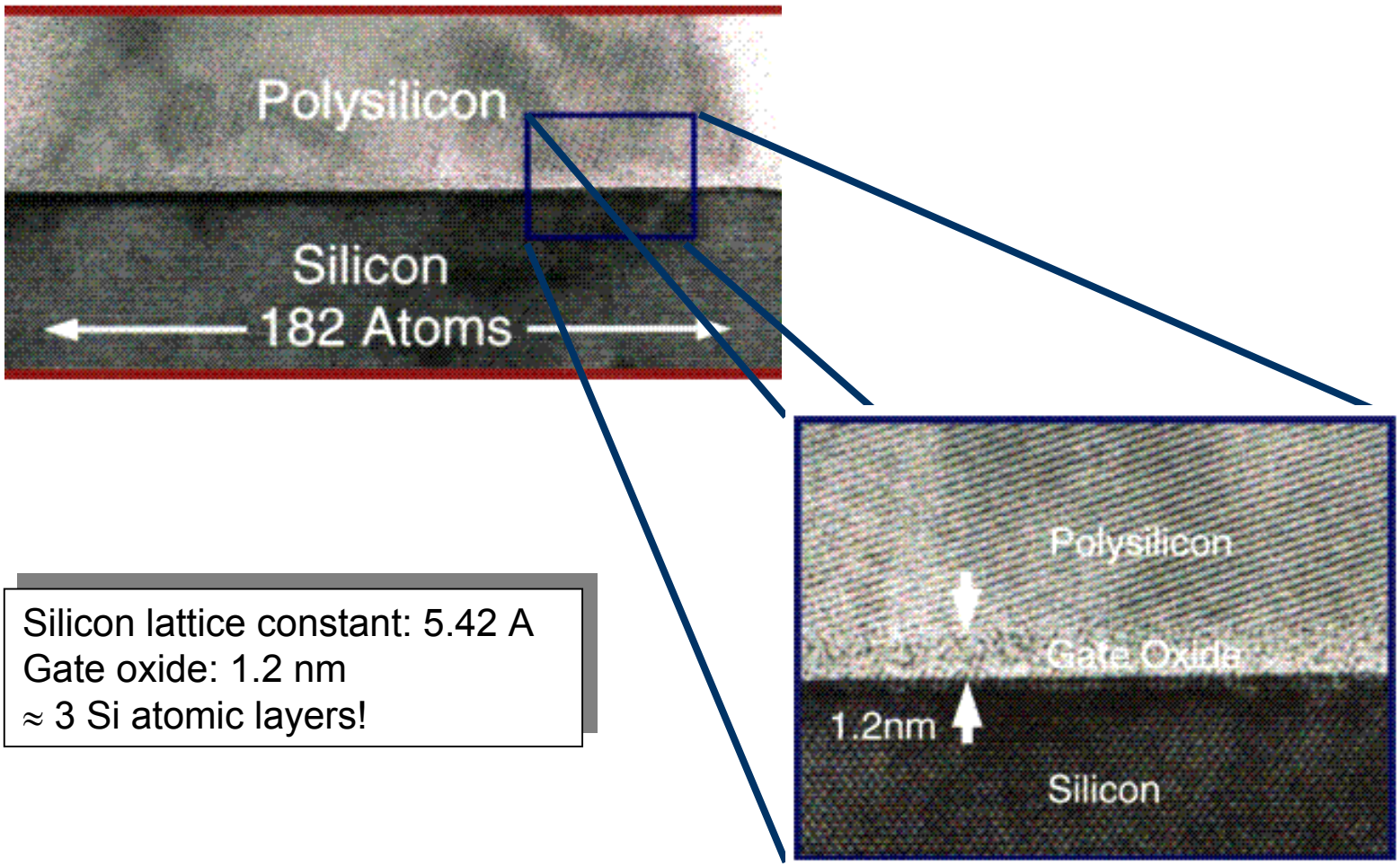
	1999	***2002***	***2014***
Technology (nm)	180	130	35
Minimum mask count	22/24	24	29/30
Wafer diameter (mm)	300	300	450
Memory-samples (bits)	1G	4G	1T
Transistors/cm^2 (μP)	6.2M	18M	390M
Wiring levels (maximum)	*6-7*	*7*	*10*
Clock, local (MHz)	1250	2100	10000
Chip size: DRAM (mm^2)	400	560	2240
Chip size: μP (mm^2)	340	430	901
Power supply (V)	1.5-1.8	1.2-1.5	0.37-0.42
Maximum Power (W)	*90*	*130*	*183*
Number of pins (μP)	700	957	3350

IEEE Spectrum, July 1999

Special report: "The 100-million transistor IC"

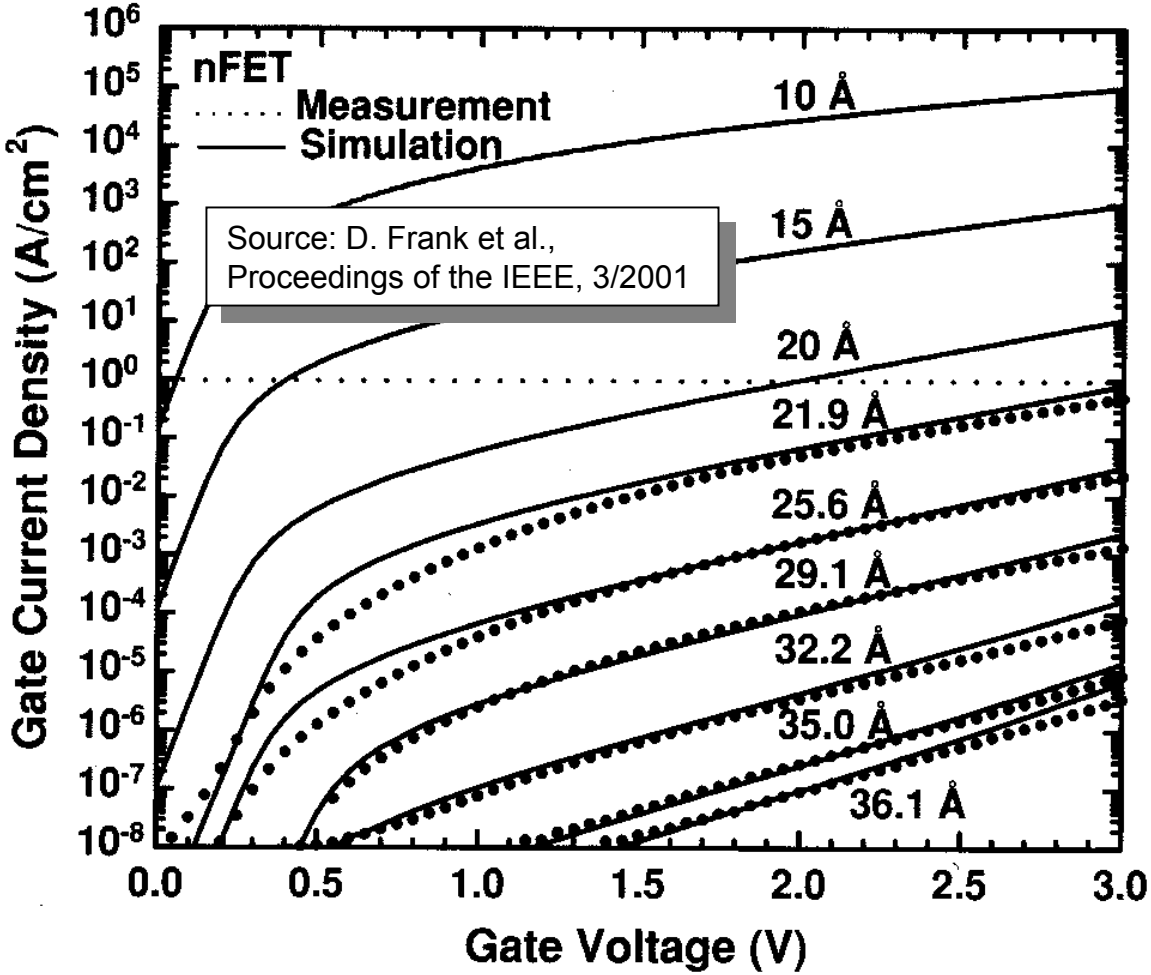
These scaling trends will allow the electronics market to growth at 15% / year

"Is there a limit?"



Silicon lattice constant: 5.42 A
Gate oxide: 1.2 nm
≈ 3 Si atomic layers!

"Is there a limit?"

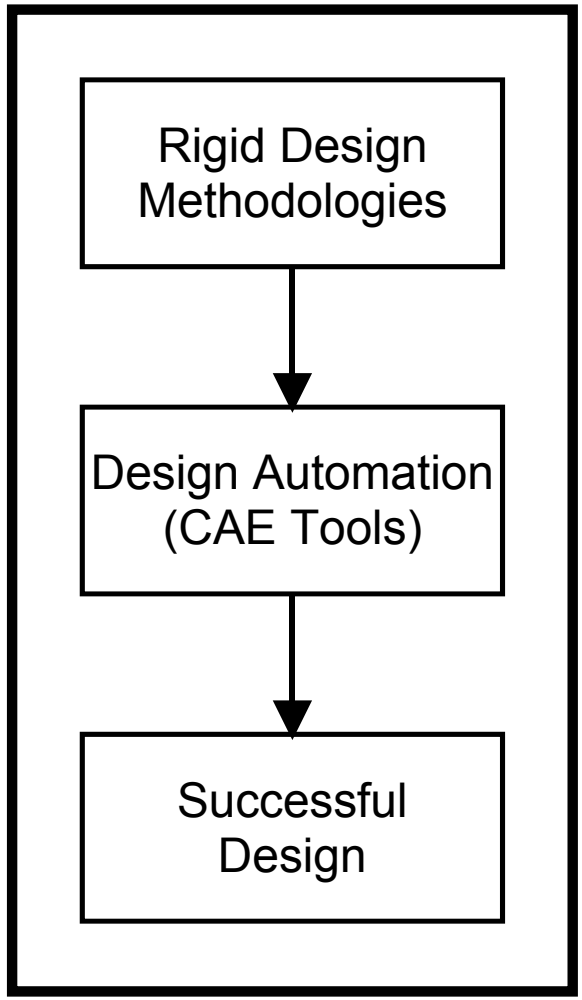


"Is there a limit?"

- High volume factory:
  - Total capacity: 40K Wafer Starts Per Month (WSPM) (180 nm)
  - Total capital cost: $2.7B
    - Production equipment: 80%
    - Facilities: 15%
    - Material handling systems: 3%
    - Factory information & control: 2%
- Worldwide semiconductor market revenues in 2000: ~$180B
  - Semiconductor market growth rate: ~15% / year
  - Equipment market growth rate: ~19.4% / year
  - By 2010 equipment spending will exceed 30% of the semiconductor market revenues!

How to cope with complexity?

- By applying:
  - Rigid design methodologies
  - Design automation



Design abstraction levels