

Outline

- Introduction – *“Is there a limit?”*
- Transistors – *“CMOS building blocks”*
- Parasitics I – *“The [un]desirables”*
- Parasitics II – *“Building a full MOS model”*
- The CMOS inverter – *“A masterpiece”*
- Technology scaling – *“Smaller, Faster and Cooler”*
- Technology – *“Building an inverter”*
- Gates I – *“Just like LEGO”*
- The pass gate – *“An useful complement”*
- Gates II – *“A portfolio”*
- Sequential circuits – *“Time also counts!”*
- DLLs and PLLs – *“A brief introduction”*
- Storage elements – *“A bit in memory”*

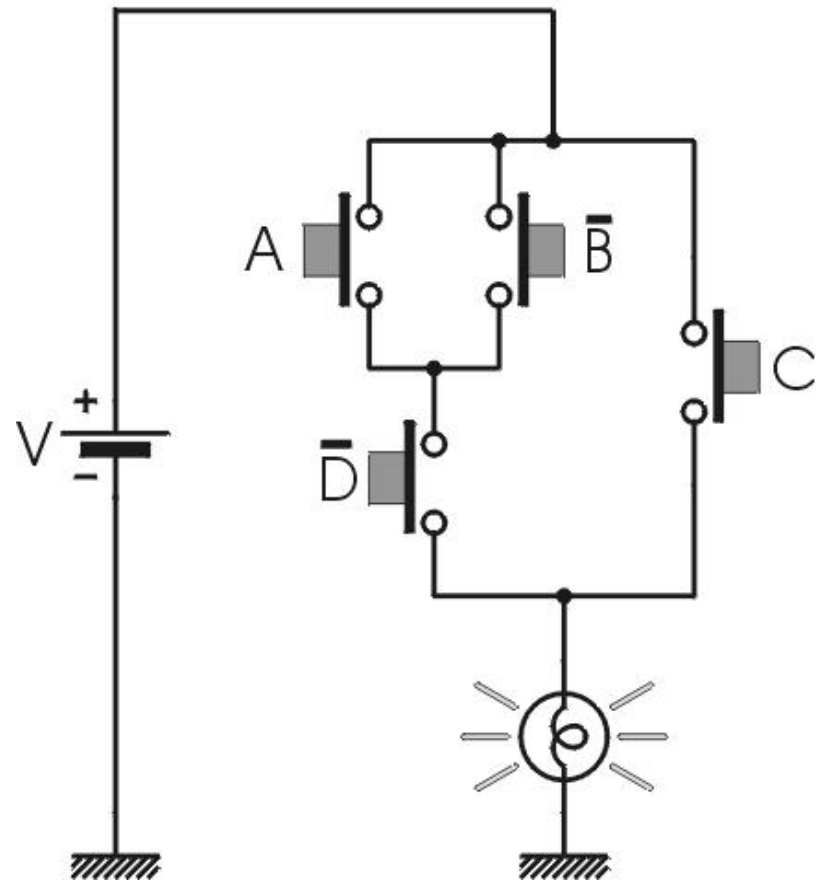
“CMOS building blocks”

- “Making Logic”
- Silicon switches:
 - The NMOS
 - Its mirror image, the PMOS
- Electrical behavior:
 - Strong inversion
 - Model
 - How good is the approximation?
 - Weak inversion
 - Gain and inversion

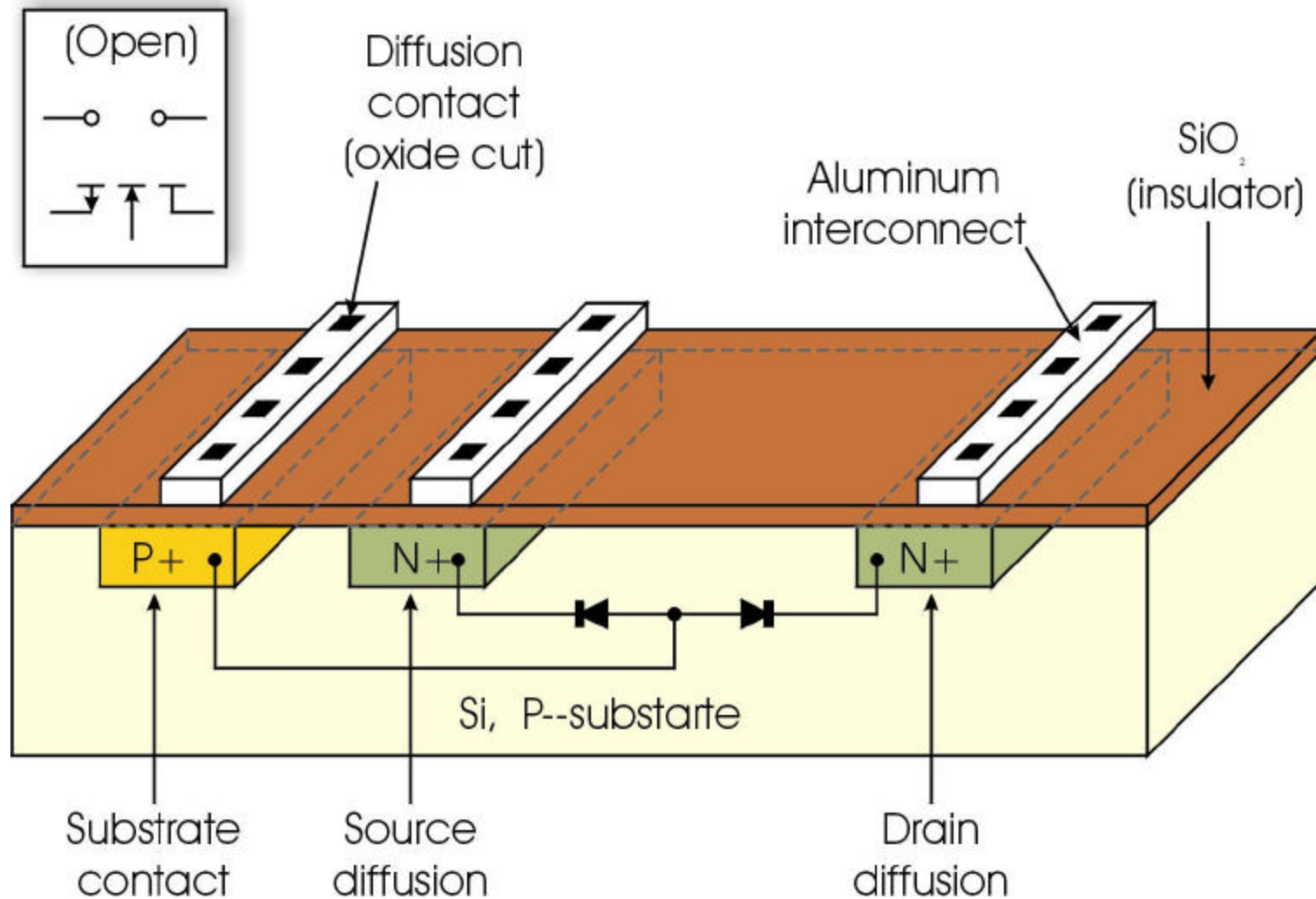
“Making Logic”

- Logic circuit “ingredients”:
 - Power source
 - Switches
 - Power gain
 - Inversion
- Power always comes from some form of external EMF generator.
- NMOS and PMOS transistors:
 - Can perform the last three functions
 - They are the building blocks of CMOS technologies!

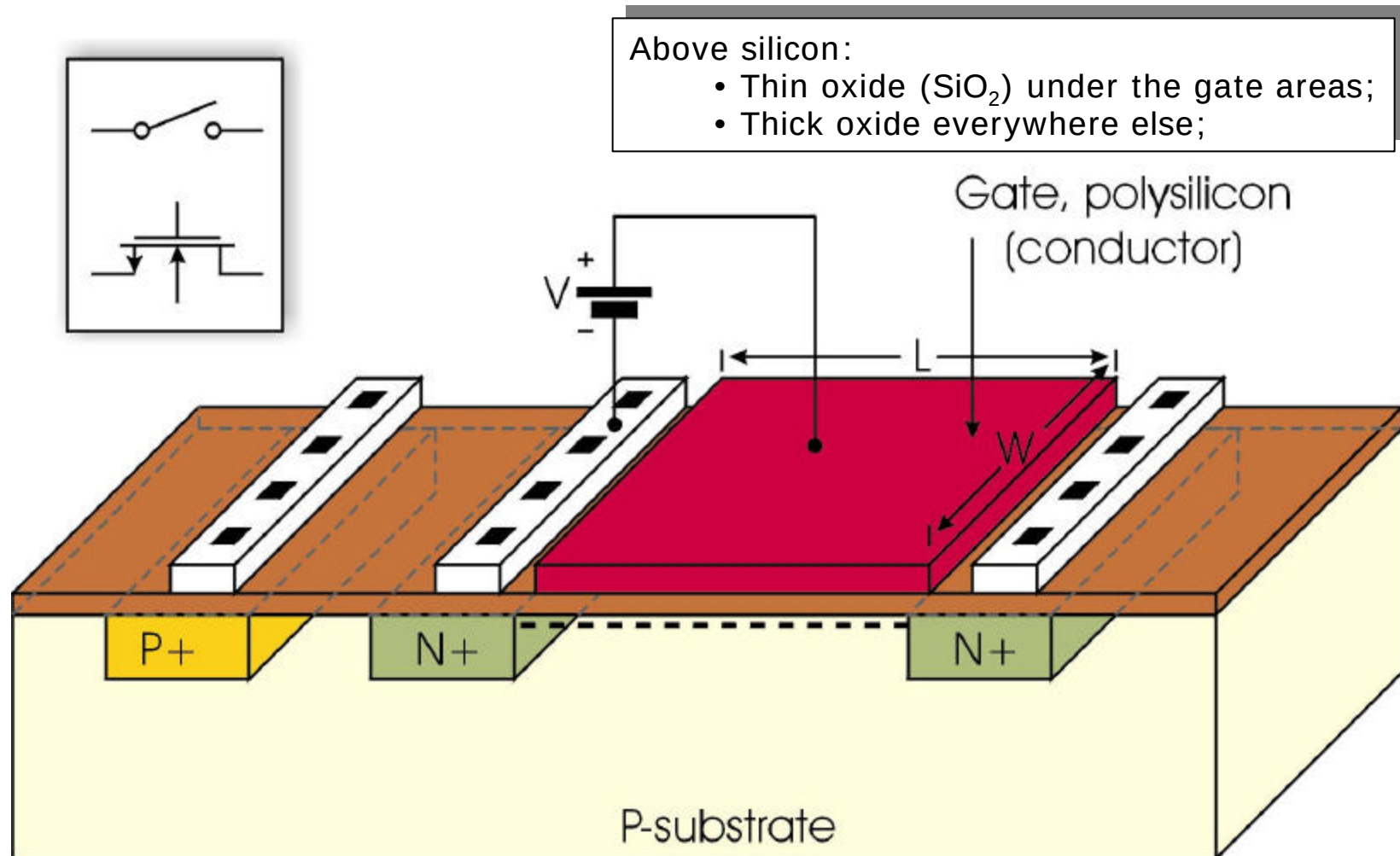
$$\text{Light ON} = (A + \bar{B}) \bar{D} + C$$



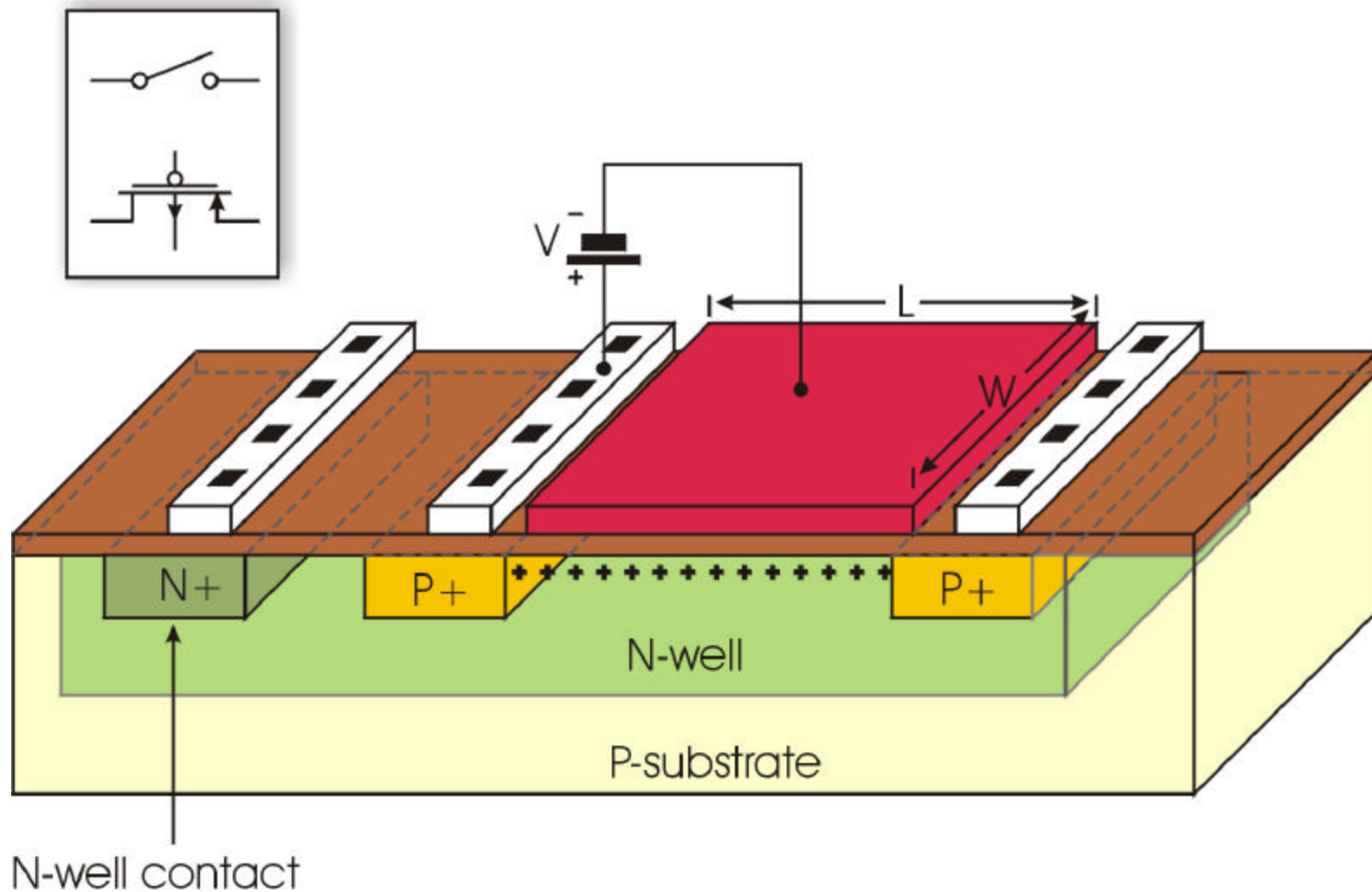
Silicon switches: the NMOS



Silicon switches: the NMOS



Silicon switches: the PMOS



MOSFET equations

- Cut-off region

$$I_{ds} = 0 \quad \text{for} \quad V_{gs} - V_T < 0$$

- Linear region

$$I_{ds} = m \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{gs} - V_T) \cdot V_{ds} - \frac{V_{ds}^2}{2} \right] \cdot (1 + l \cdot V_{ds}) \quad \text{for} \quad 0 < V_{ds} < V_{gs} - V_T$$

- Saturation

$$I_{ds} = \frac{m \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_T)^2 \cdot (1 + l \cdot V_{ds}) \quad \text{for} \quad V_{ds} > V_{gs} - V_T$$

- Oxide capacitance

$$C_{ox} = \frac{e_{ox}}{t_{ox}} \quad (\text{F} / \text{m}^2)$$

- Process “transconductance”

$$m \cdot C_{ox} = \frac{m \cdot e_{ox}}{t_{ox}} \quad (\text{A} / \text{V}^2)$$

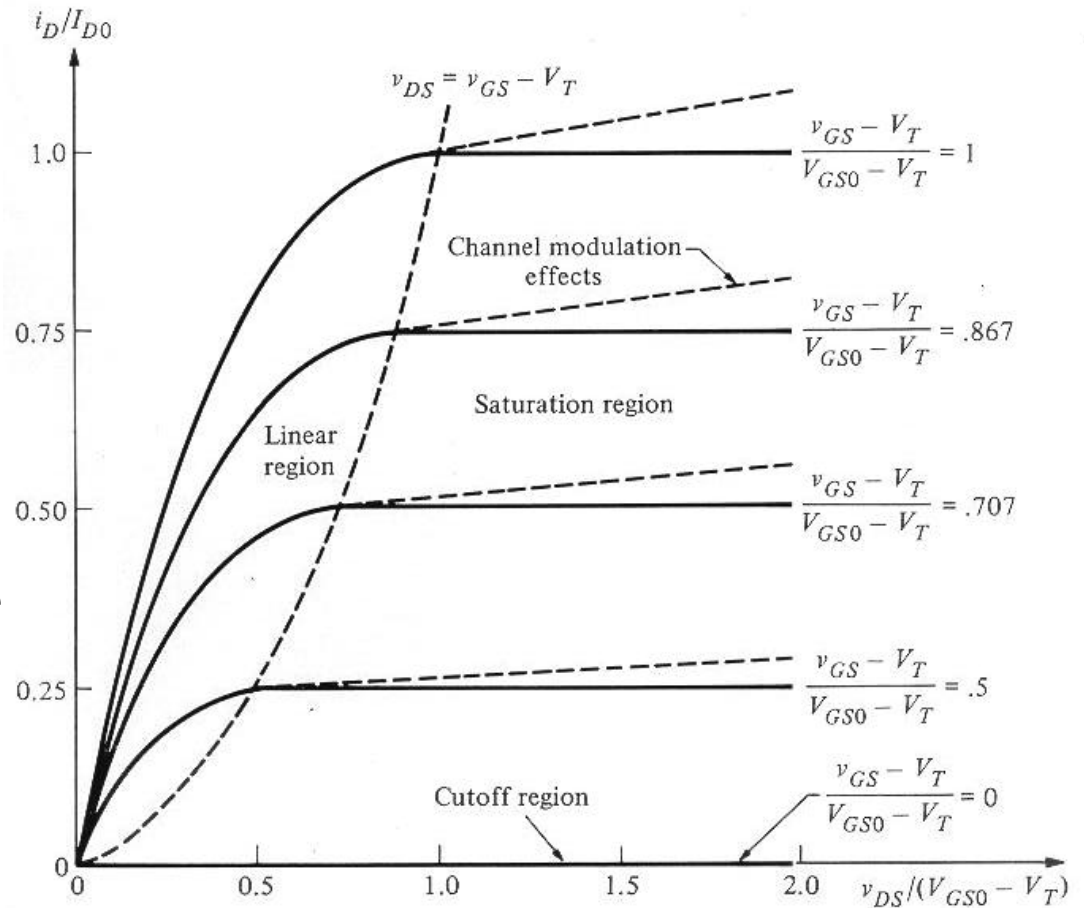
0.24μm process

$t_{ox} = 5\text{nm}$ (~10 atomic layers)

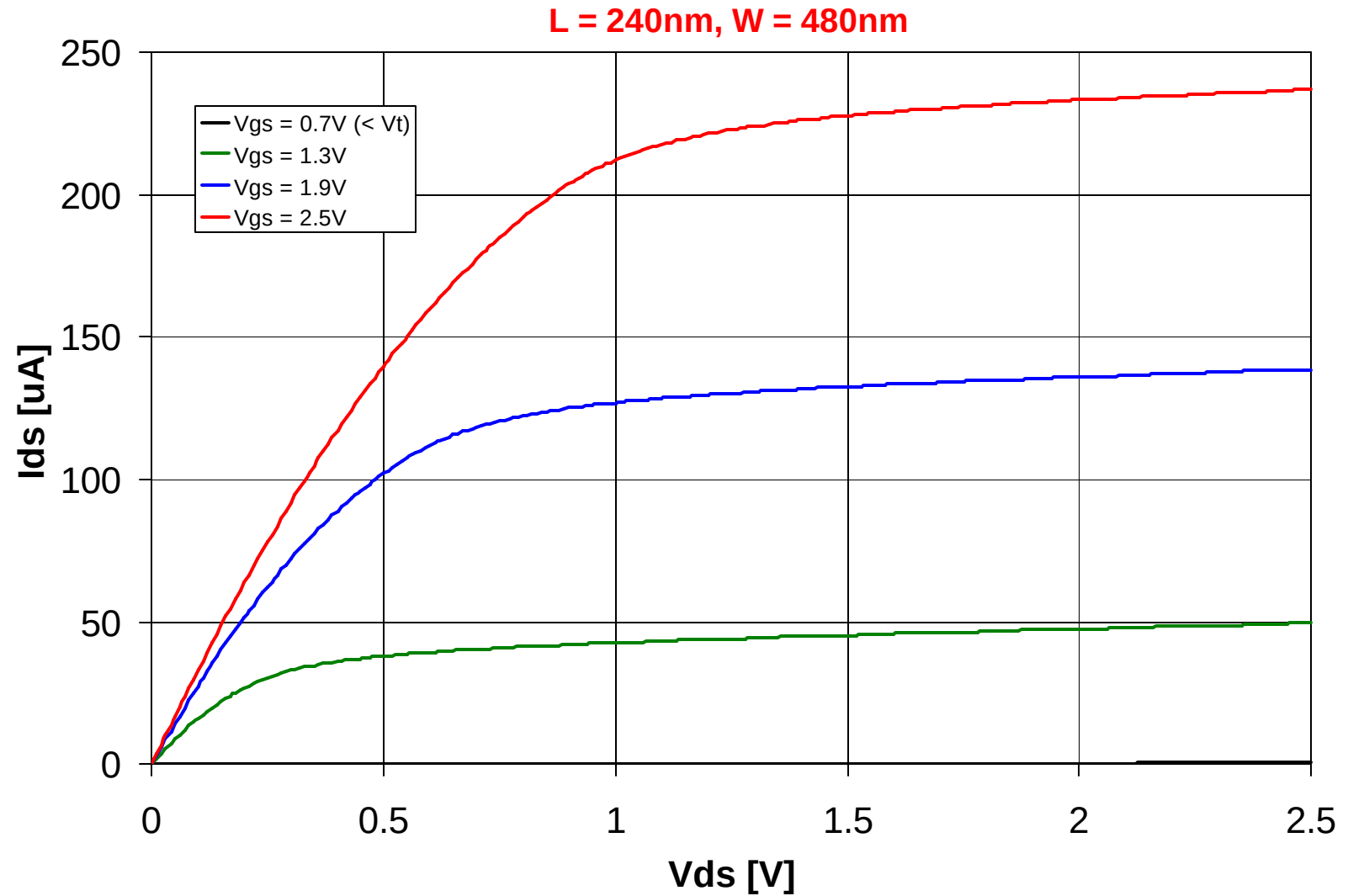
$C_{ox} = 5.6\text{fF}/\mu\text{m}^2$

MOS output characteristics

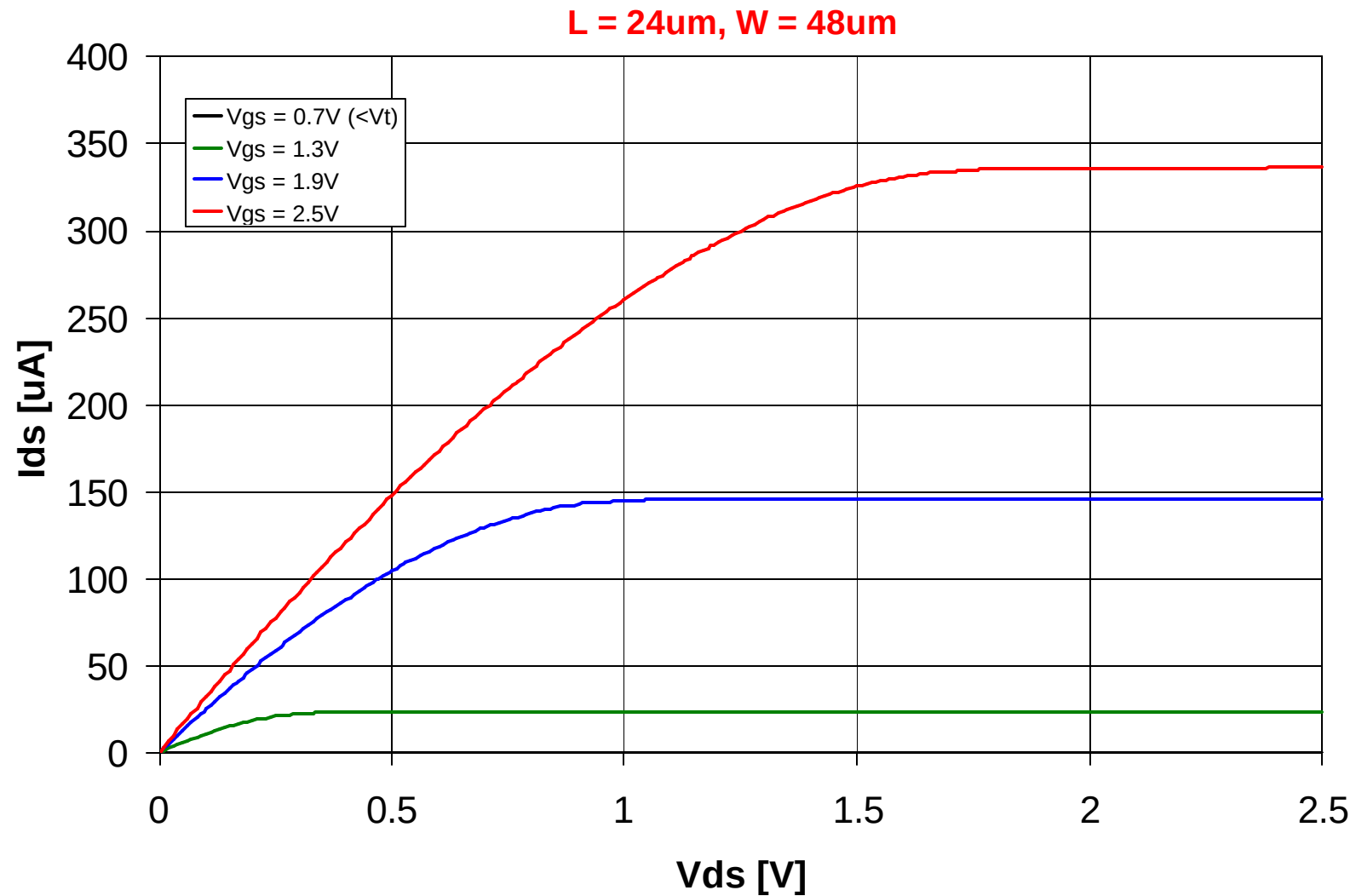
- **Linear region:**
 $V_{ds} < V_{gs} - V_T$
 - Voltage controlled resistor
- **Saturation region:**
 $V_{ds} > V_{gs} - V_T$
 - Voltage controlled current source
- Curves deviate from the ideal current source behavior due to:
 - Channel modulation effects



MOS output characteristics

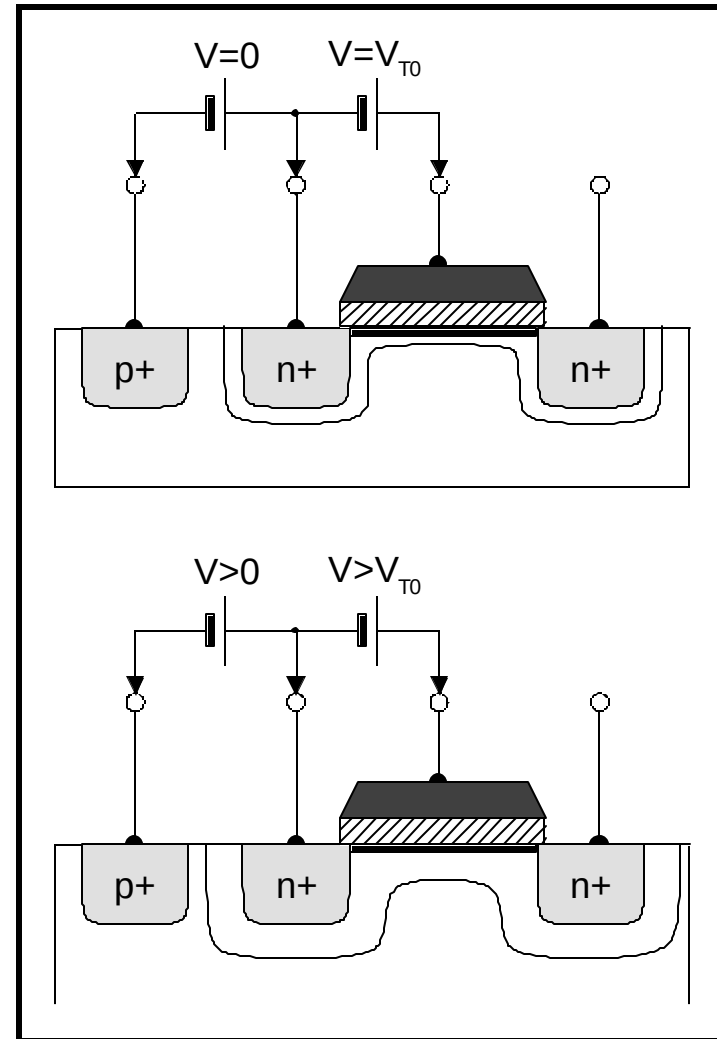


MOS output characteristics

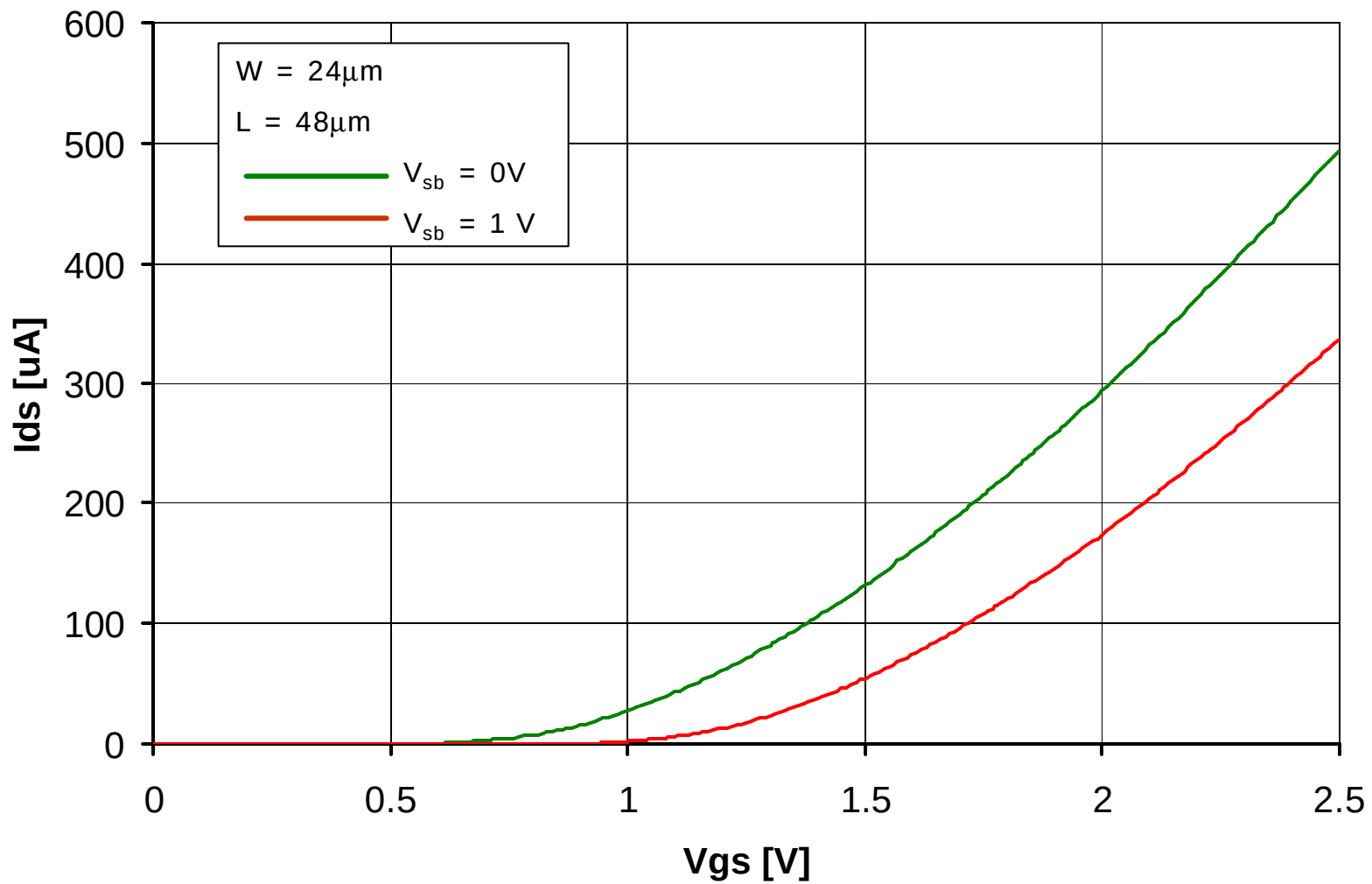


Bulk effect

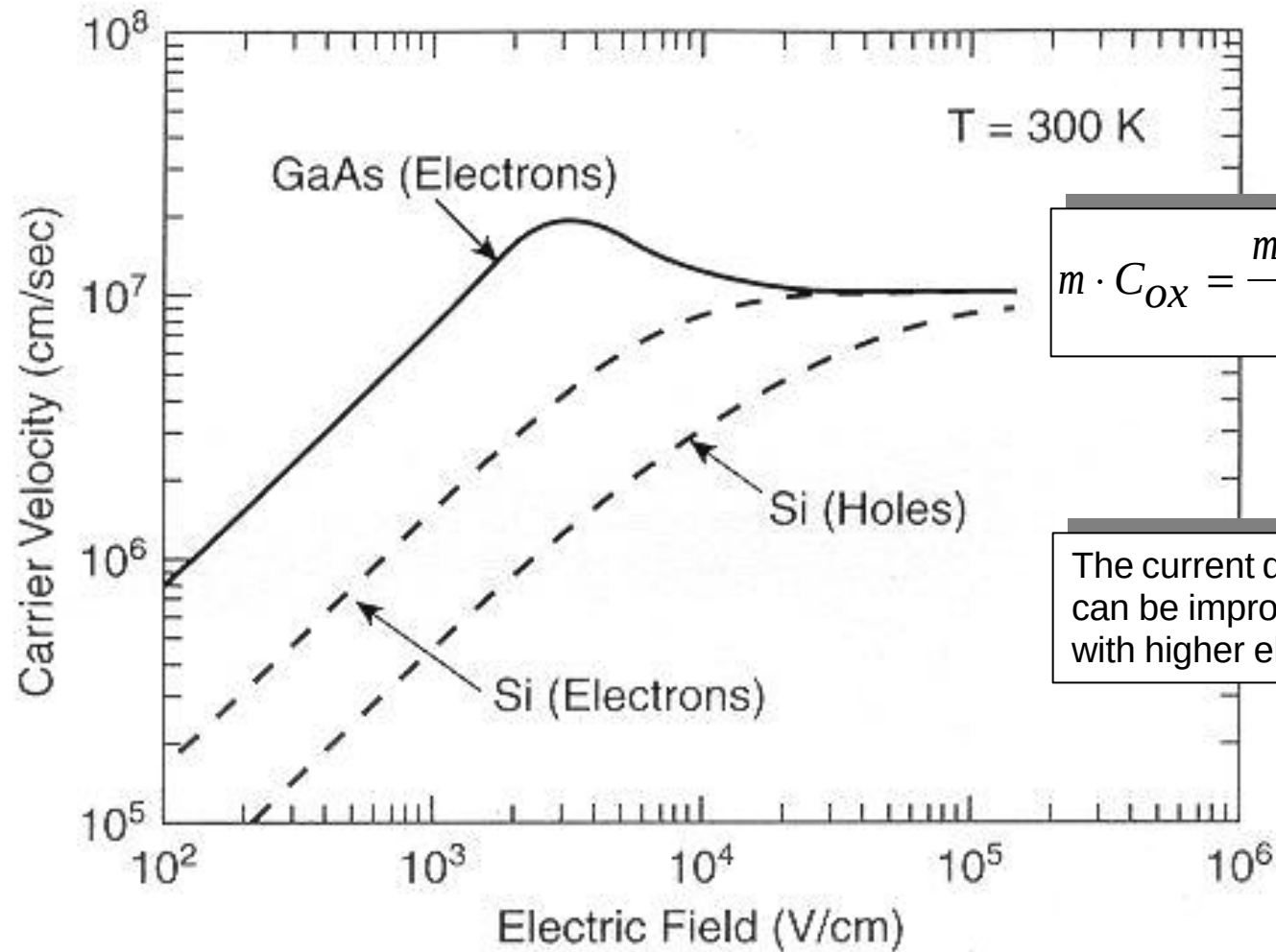
- The threshold depends on:
 - Gate oxide thickness
 - Doping levels
 - Source-to-bulk voltage
- When the semiconductor surface inverts to n-type the channel is in “strong inversion”
- $V_{sb} = 0 \Rightarrow$ strong inversion for:
 - surface potential $> -2\phi_F$
- $V_{sb} > 0 \Rightarrow$ strong inversion for:
 - surface potential $> -2\phi_F + V_{sb}$



Bulk effect



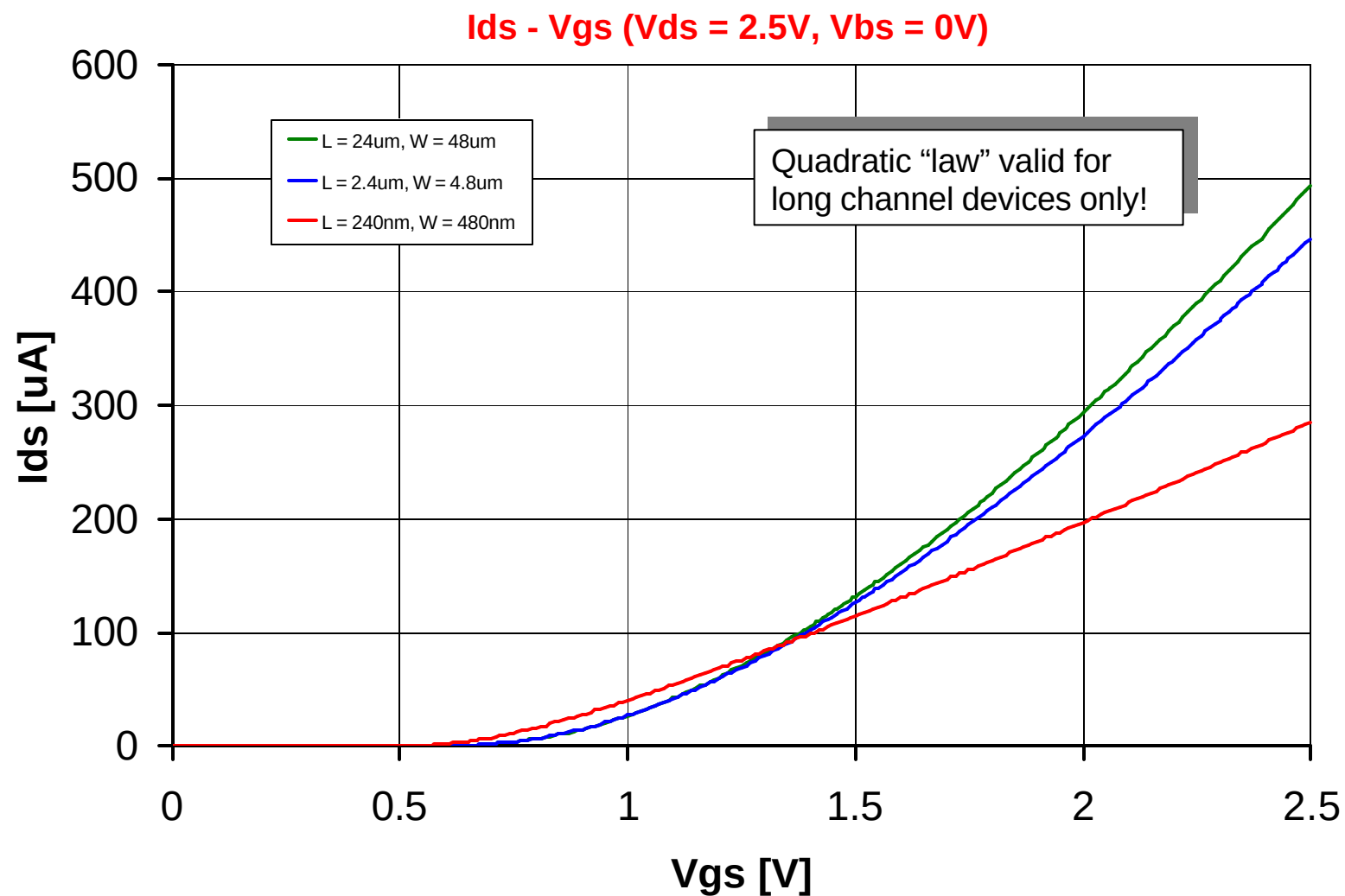
Mobility



$$m \cdot C_{ox} = \frac{m \cdot e_{ox}}{t_{ox}} \quad \left(A / V^2 \right)$$

The current driving capability can be improved by using materials with higher electron mobility

Is the quadratic law valid?



Weak inversion

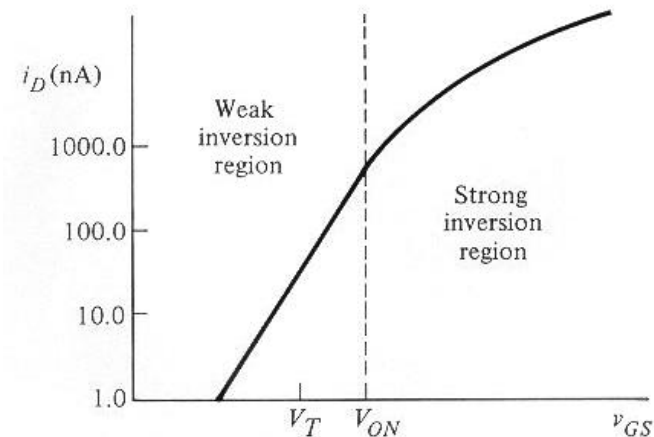
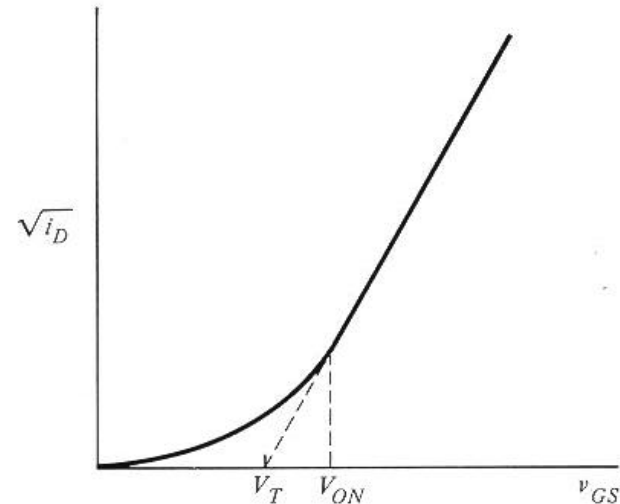
- Is $I_d=0$ when $V_{gs} < V_T$?
- For $V_{gs} < V_T$ the drain current depends exponentially on V_{gs}
- In weak inversion and saturation ($V_{ds} > \sim 150\text{mV}$):

$$I_d \cong \frac{W}{L} \cdot I_{do} \cdot e^{\frac{q \cdot V_{gs}}{n \cdot k \cdot T}}$$

where

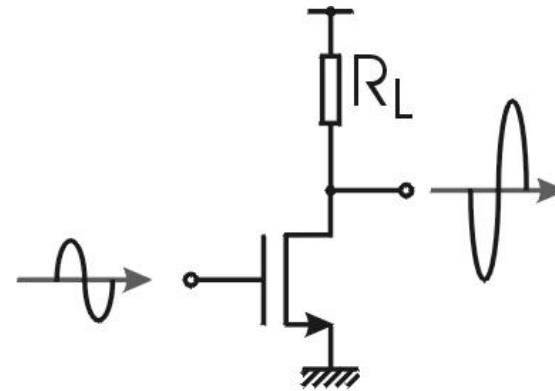
$$I_{do} = e^{-\frac{q \cdot V_T}{n \cdot k \cdot T}}$$

- Used in very low power designs
- Slow operation



Gain & Inversion

- Gain:
 - Signal regeneration at every logic operation
 - “Static” flip-flops
 - “Static” RW memory cells
- Inversion:
 - Intrinsic to the common-source configuration
- The gain cell load can be:
 - Resistor
 - Current source
 - Another gain device (PMOS)



$$V_{\text{out}} = -g_m \times (R_{\text{ds}} \parallel R_L) \times V_{\text{in}}$$

