ICTP Microprocessor Laboratory
African Regional Course on Advanced VLSI Design Techniques
Kwame Nkrumah University of Science and Technology, Kumasi, Ghana
24 November – 12 December 2003

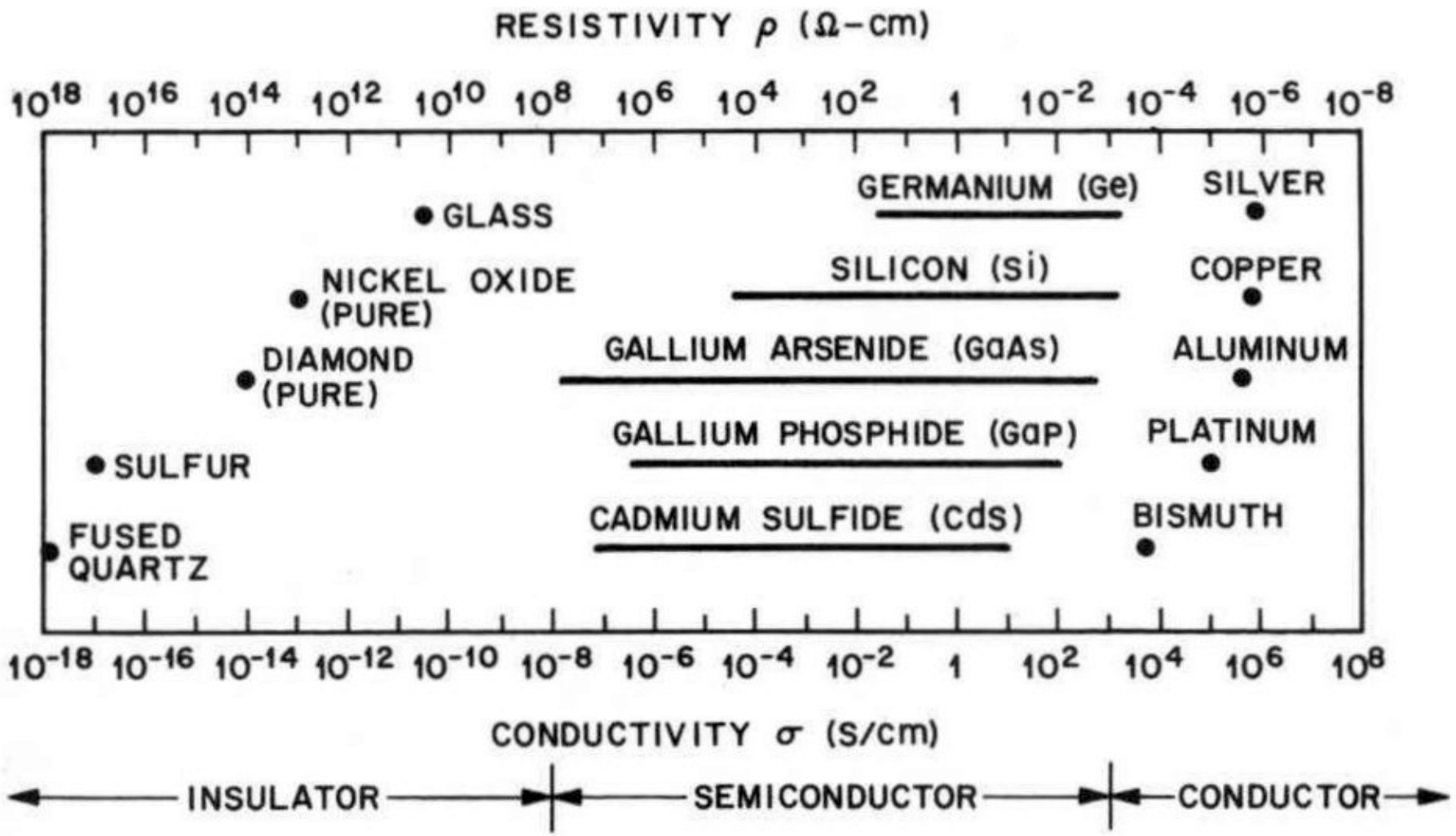
# Introduction to Analog Design in Submicron CMOS Technologies

**Giovanni Anelli**
CERN - European Organization for Nuclear Research
Experimental Physics Division
Microelectronics Group
CH-1211 Geneva 23 – Switzerland
Giovanni.Anelli@cern.ch

# Outline

- Semiconductor physics
  - Silicon and silicon dioxide properties
  - Band diagram concept
  - Intrinsic and doped semiconductors
  - Carrier mobility in silicon
- CMOS technology: an analog designer perspective
  - The MOS transistor
  - DC characteristics
  - Important formulas
  - Small signal equivalent circuit
  - Some cross sections of real integrated circuits

# Insulators and (semi)conductors




**S. M. Sze, *Semiconductor Devices, Physics and Technology*, John Wiley and Sons, 1985, p. 1**

# Physical Properties of Si and $SiO_2$

**at room temperature (300 K)**

| Property | Si | $SiO_2$ |
|---|---|---|
| Atomic/molecular weight | 28.09 | 60.08 |
| Atoms or molecules/$cm^3$ | $5.0 \times 10^{22}$ | $2.3 \times 10^{22}$ |
| Density ($g/cm^3$) | 2.33 | 2.27 |
| Crystal structure | Diamond | Amorphous |
| Lattice constant (Å) | 5.43 | — |
| Energy gap (eV) | 1.12 | 8–9 |
| Dielectric constant | 11.7 | 3.9 |
| Intrinsic carrier concentration ($cm^{-3}$) | $1.4 \times 10^{10}$ | — |
| Carrier mobility ($cm^2$/V-s) | Electron: 1430 | — |
| | Hole: 470 | — |
| Effective density of states ($cm^{-3}$) | Conduction band, $N_c$: $3.2 \times 10^{19}$ | — |
| | Valence band, $N_v$: $1.8 \times 10^{19}$ | — |
| Breakdown field (V/cm) | $3 \times 10^5$ | $>10^7$ |
| Melting point (°C) | 1415 | 1600–1700 |
| Thermal conductivity (W/cm-°C) | 1.5 | 0.014 |
| Specific heat (J/g-°C) | 0.7 | 1.0 |
| Thermal diffusivity ($cm^2/s$) | 0.9 | 0.006 |
| Thermal expansion coefficient ($°C^{-1}$) | $2.5 \times 10^{-6}$ | $0.5 \times 10^{-6}$ |

**Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998, p. 11.**

# Silicon crystalline structure

**Orbitals filling**

$3p^2$

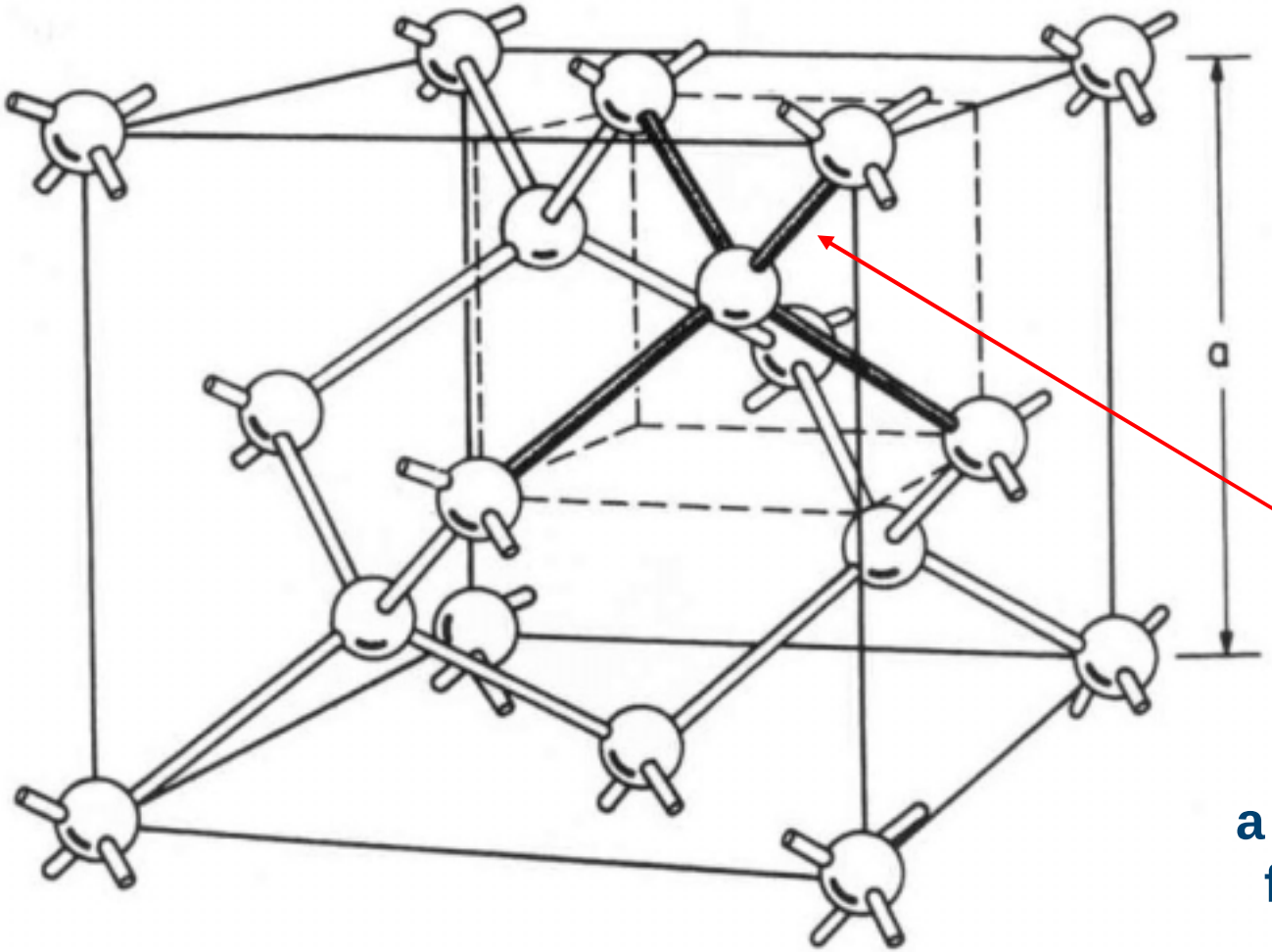
$3s^2$

$2p^6$

$2s^2$

$1s^2$

**Nucleus**




**Diamond lattice structure**

**Covalent bonding**

**a = 0.513 nm for Silicon**

**S. M. Sze, *Semiconductor Devices, Physics and Technology*, John Wiley and Sons, 1985, p. 5.**
**Linus Pauling, *General Chemistry*, Dover, 1988, p. 128.**

# From energy levels to bands

**Allowed energy levels**

$$E_n = \frac{-Z^2 m_0 q^4}{8\varepsilon_0^2 h^2 n^2}$$

**Z: atomic number**

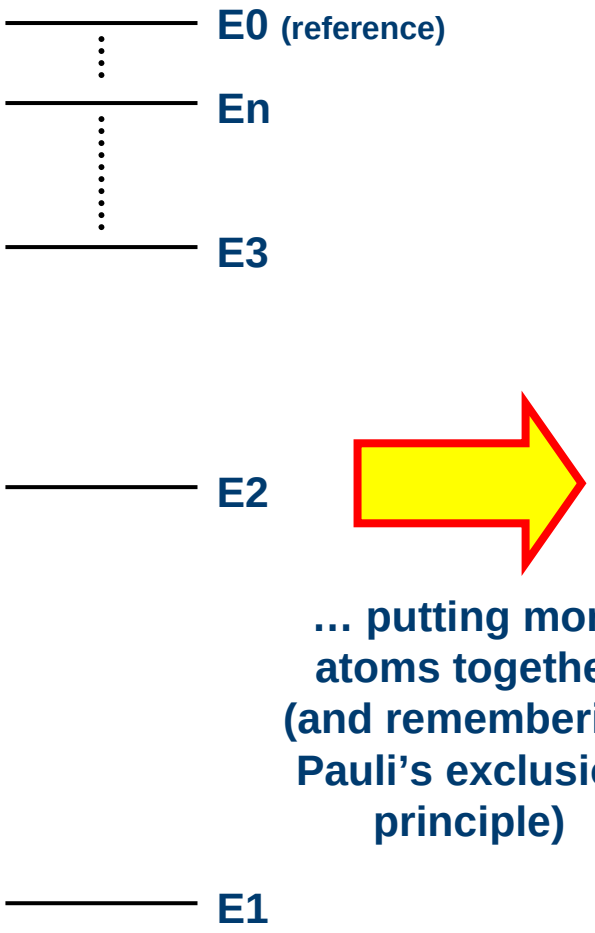
**$m_0$: free electron mass**

**q: electron charge**

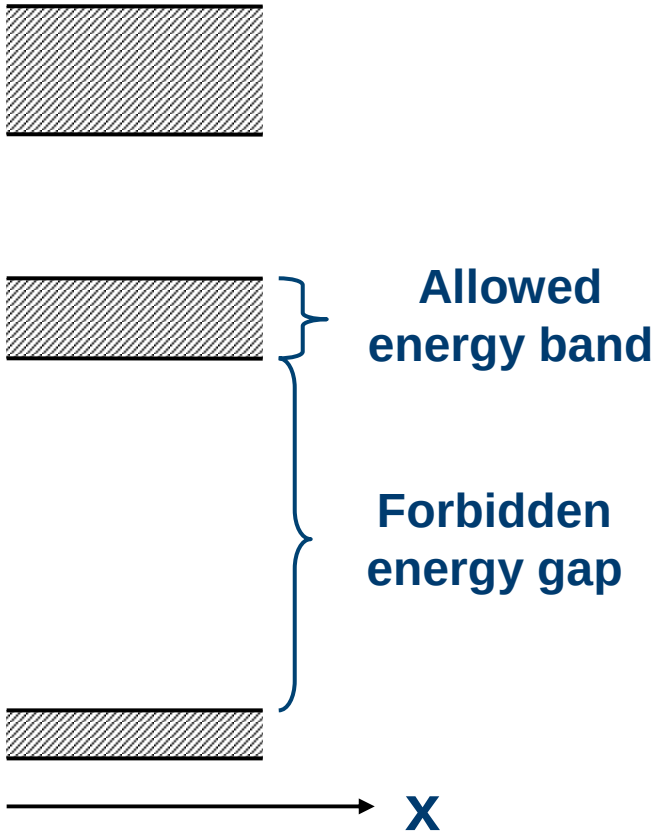
**$\varepsilon_0$: permittivity free space**

**h: Planck's constant**

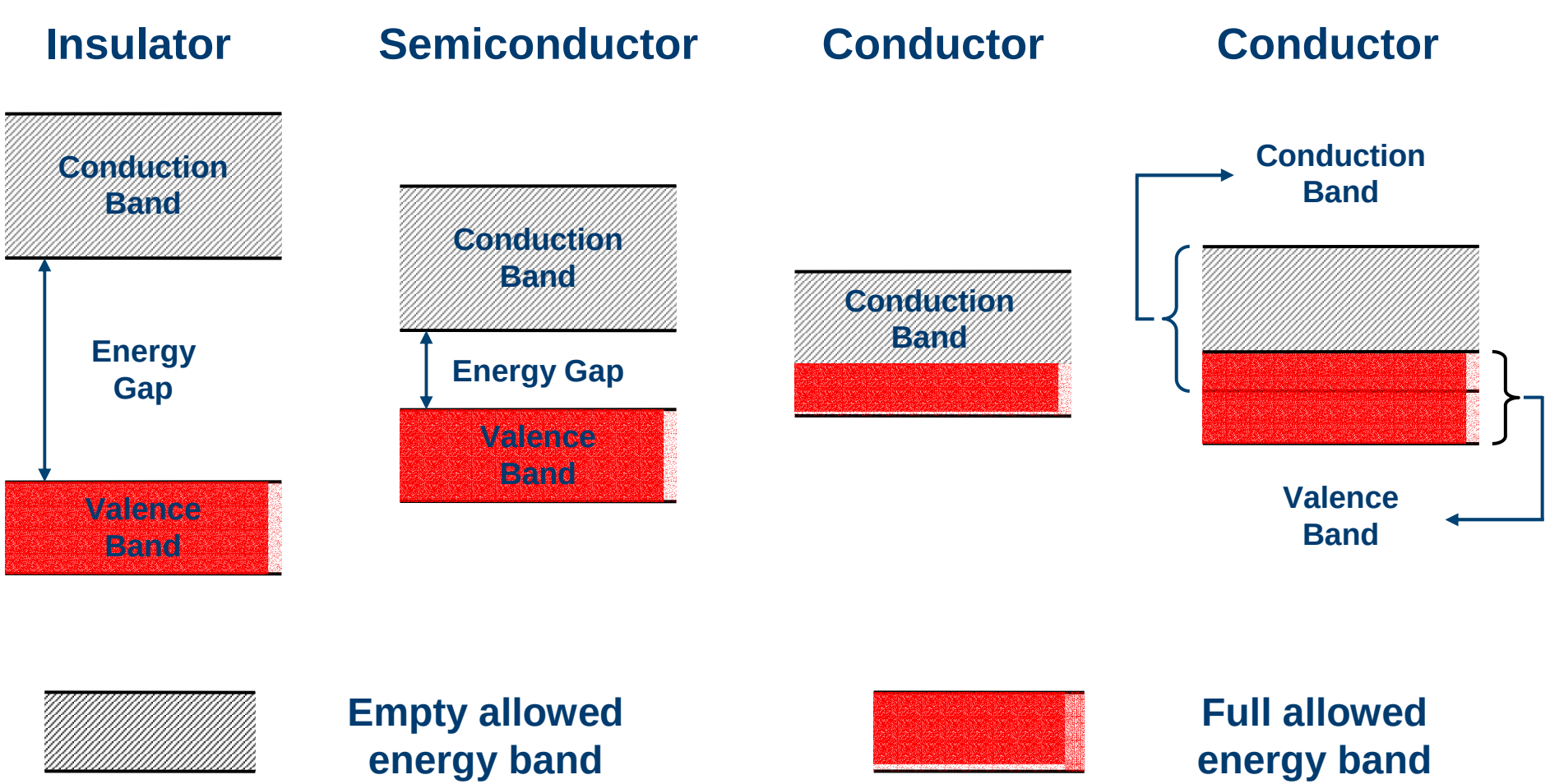
**n: positive integers (level number)**



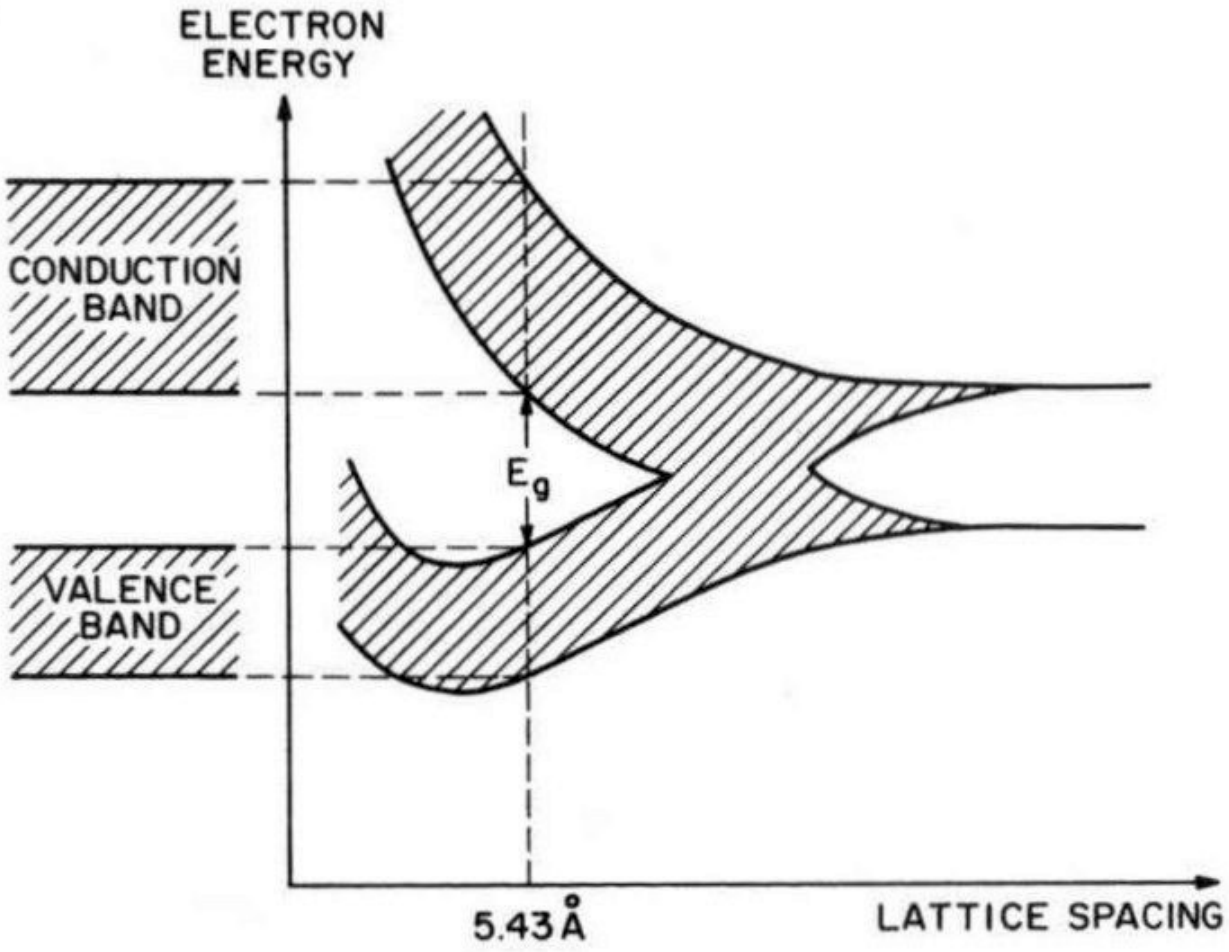

**… putting more atoms together (and remembering Pauli's exclusion principle)**



# Energy-band diagrams



# Formation of Energy Bands



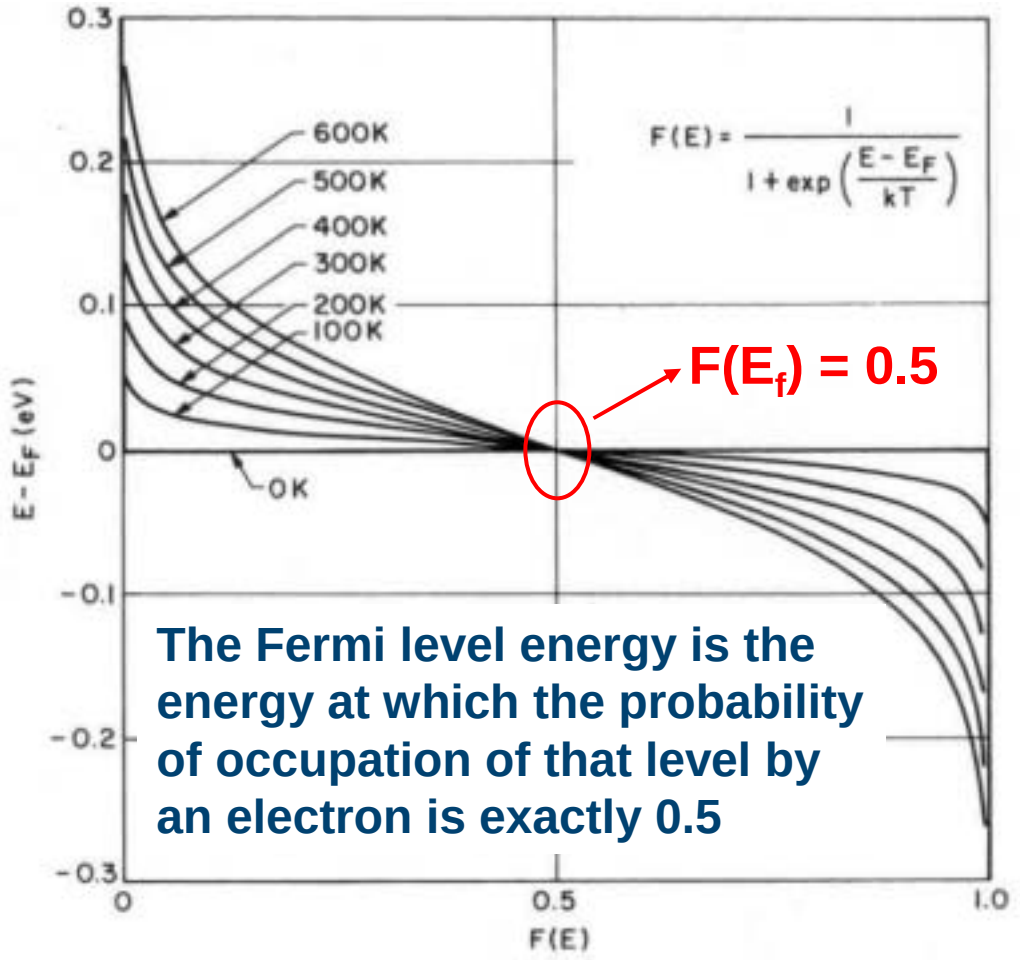

**Curves obtained with quantum mechanical calculations made for diamond lattice crystals.**

**Increasing T increases the lattice spacing and therefore gives a lower energy gap**

**S. M. Sze, *Semiconductor Devices, Physics and Technology*, John Wiley and Sons, 1985, p. 10.**

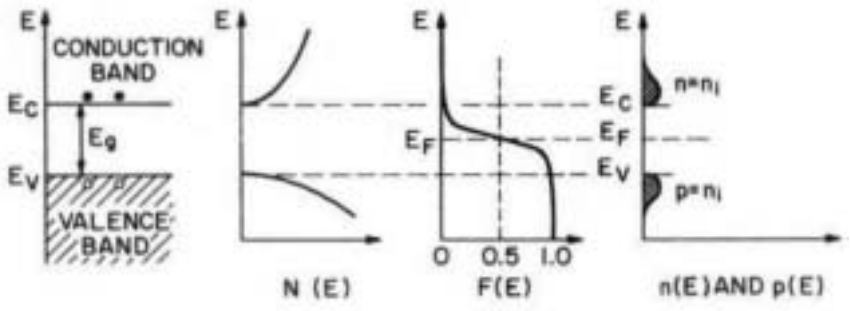
# Intrinsic carrier concentration

## F(E): Fermi-Dirac distribution




**The Fermi level energy is the energy at which the probability of occupation of that level by an electron is exactly 0.5**

## N(E): Density of allowed states




$n = p = n_i$

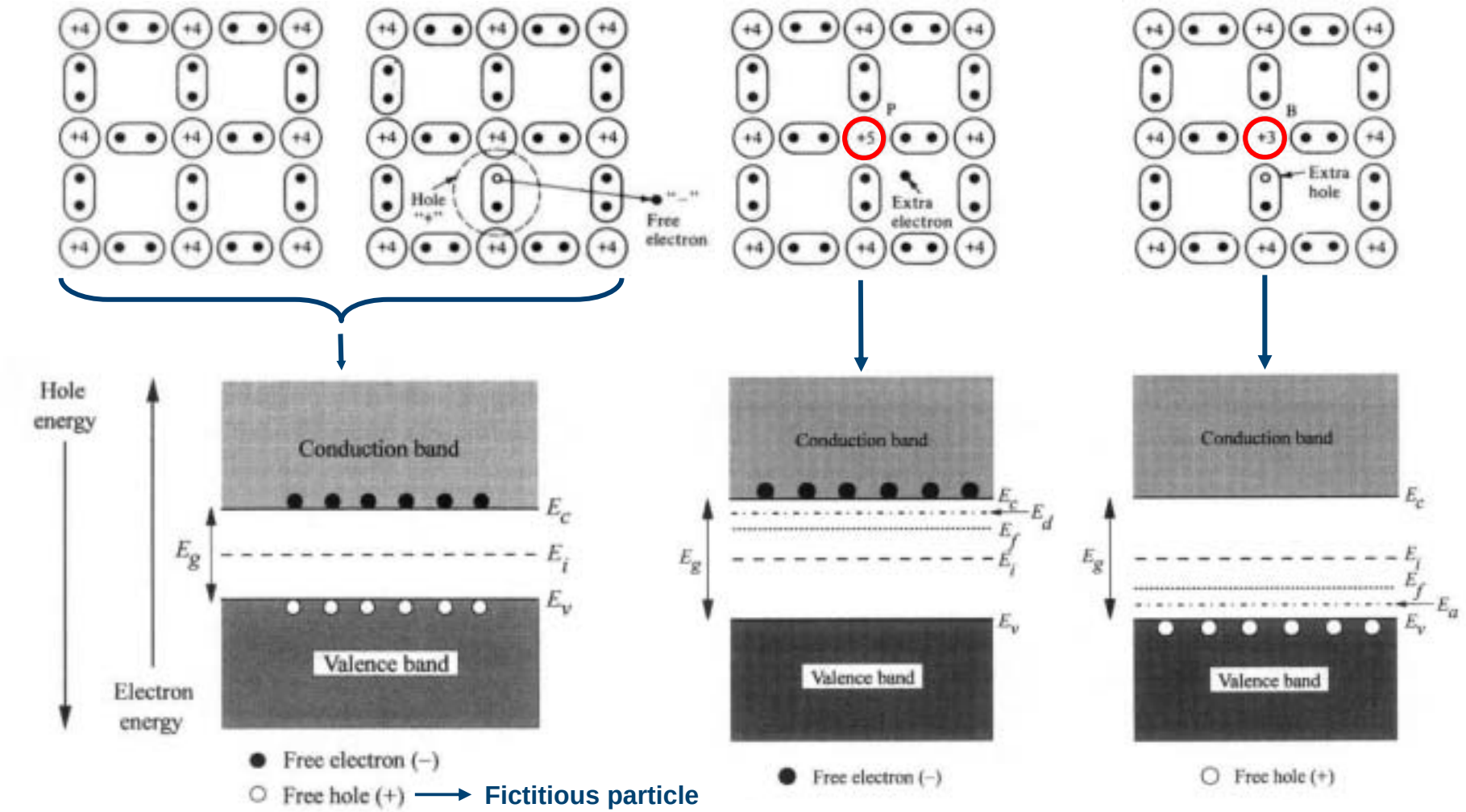
$n_i$ = intrinsic carrier density

$n_i = 1.45*10^{10}\ cm^{-3}$

**The intrinsic carrier concentration is given by the integral as a function of the energy of the product between the functions N(E) and F(E)**

S. M. Sze, *Semiconductor Devices, Physics and Technology*, John Wiley and Sons, 1985, pp. 17, 18.

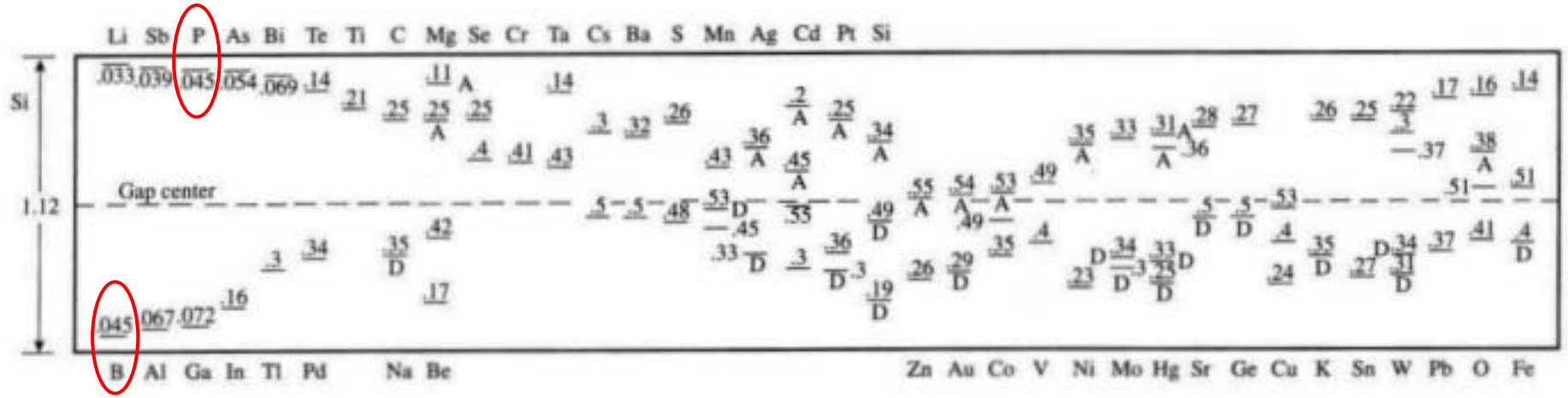
# Intrinsic and doped silicon





**Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998, pp. 10, 13, 14.**
**E. S. Yang, *Microelectronic Devices*, McGraw-Hill International Editions, 1988, pp. 9, 15.**

# Donors and acceptors



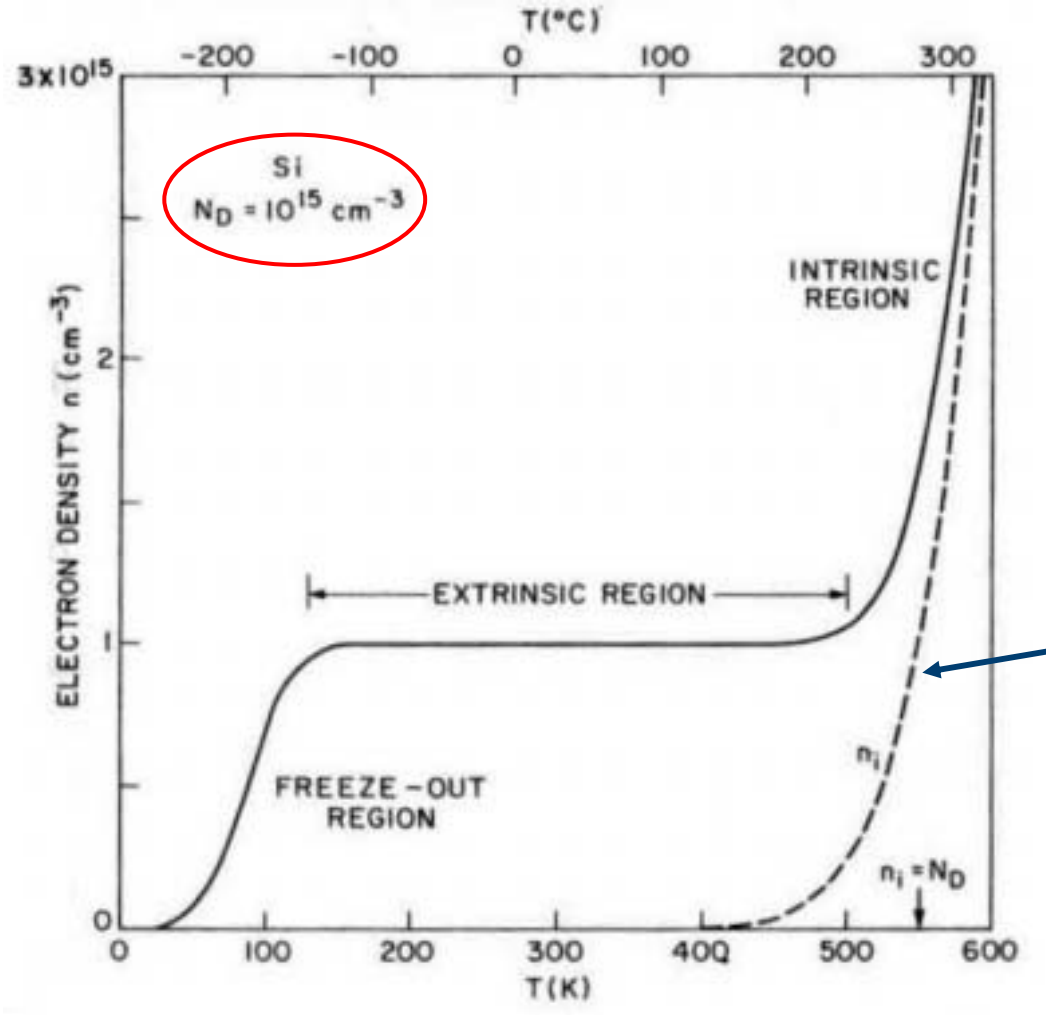

**Intrinsic Semiconductor:** small amount of impurities compared to the thermally generated electrons and holes

**Donor level:** the allowed energy level provided by a donor is neutral when occupied by an electron and positively charged when empty

**Acceptor level:** the allowed energy level provided by an acceptor is neutral when empty (= occupied by a hole) and negatively charged when occupied by an electron (= empty)

Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998, p. 15.

# Carrier density vs Temperature




**N-type semiconductor**

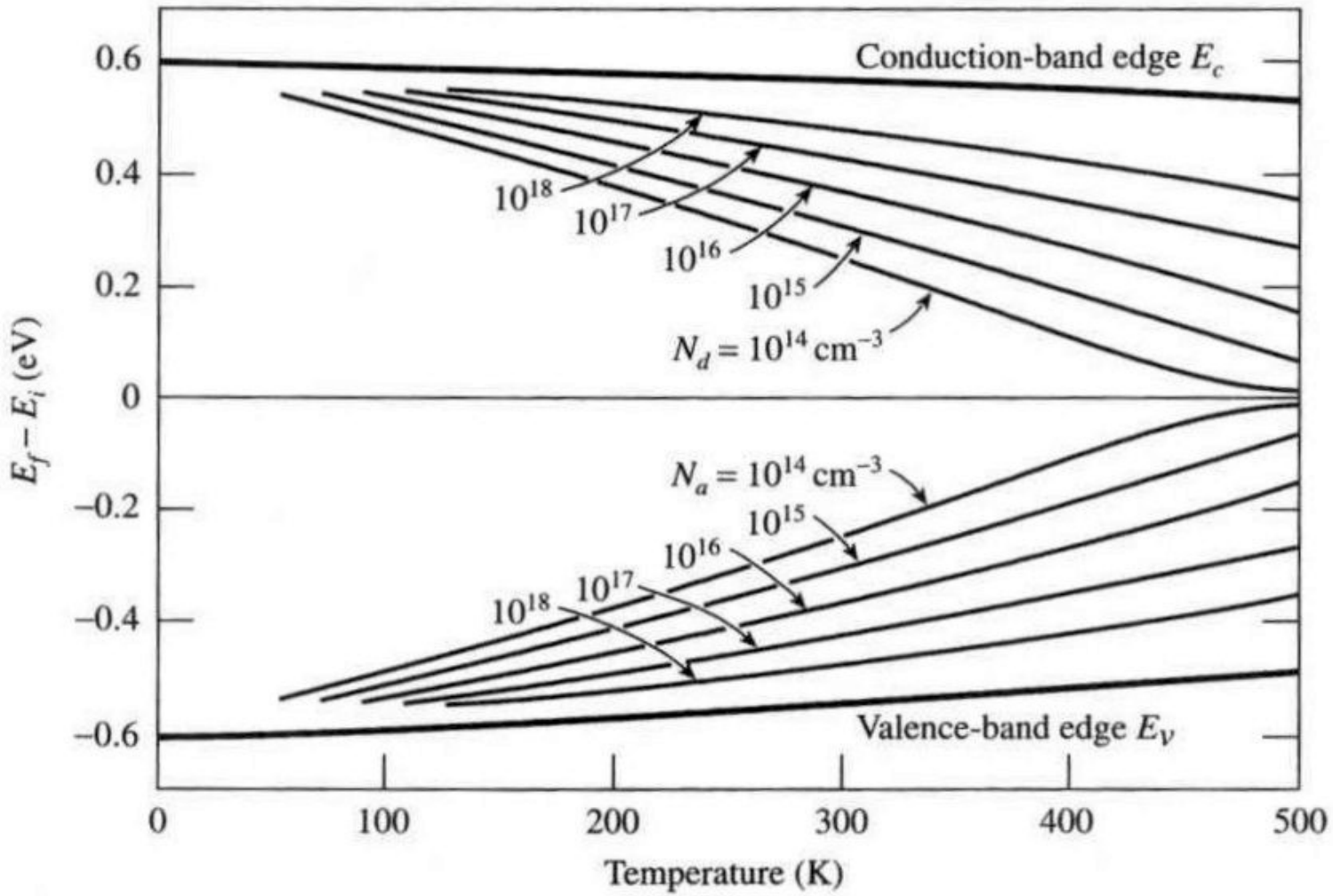
**Electrons are the majority carriers**

**Intrinsic carrier density (= hole density)**

$$n_i^2 = N_c \cdot N_v \cdot e^{-\frac{E_g}{kT}}$$

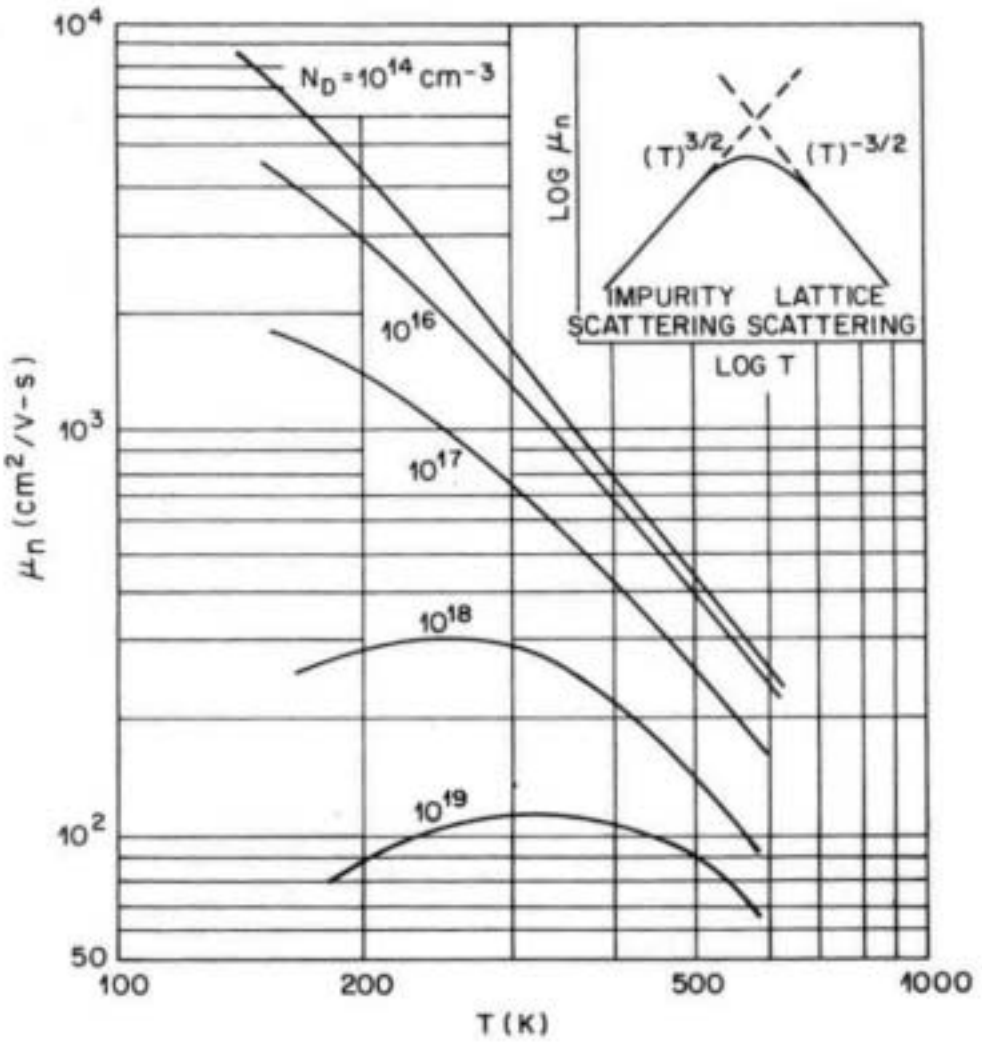
S. M. Sze, *Semiconductor Devices, Physics and Technology*, John Wiley and Sons, 1985, p. 27

# Fermi levels vs Doping and T




**Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998, p. 18.**

# Mobility vs T and $N_D$




**$N_D$: doping concentration**

$$v_d = -\frac{q\tau_m}{m_e}E = -\mu_n E$$

**$v_d$ = drift velocity**

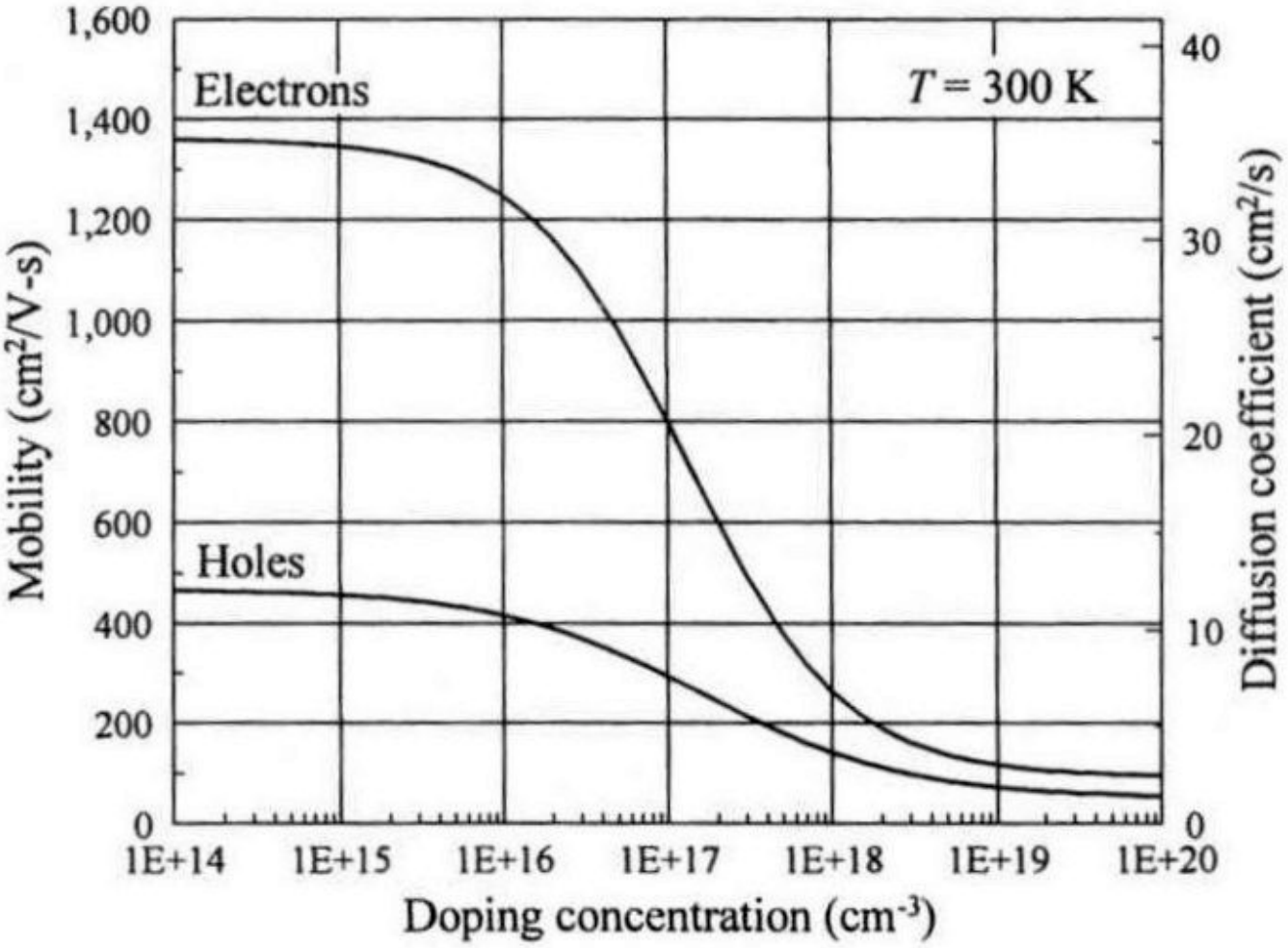
**$\tau_m$ = mean free time between collisions**

**$m_e$ = conductivity effective mass**

**E = electric field**

**S. M. Sze, *Semiconductor Devices, Physics and Technology*, John Wiley and Sons, 1985, p. 33.**

# Mobility vs doping

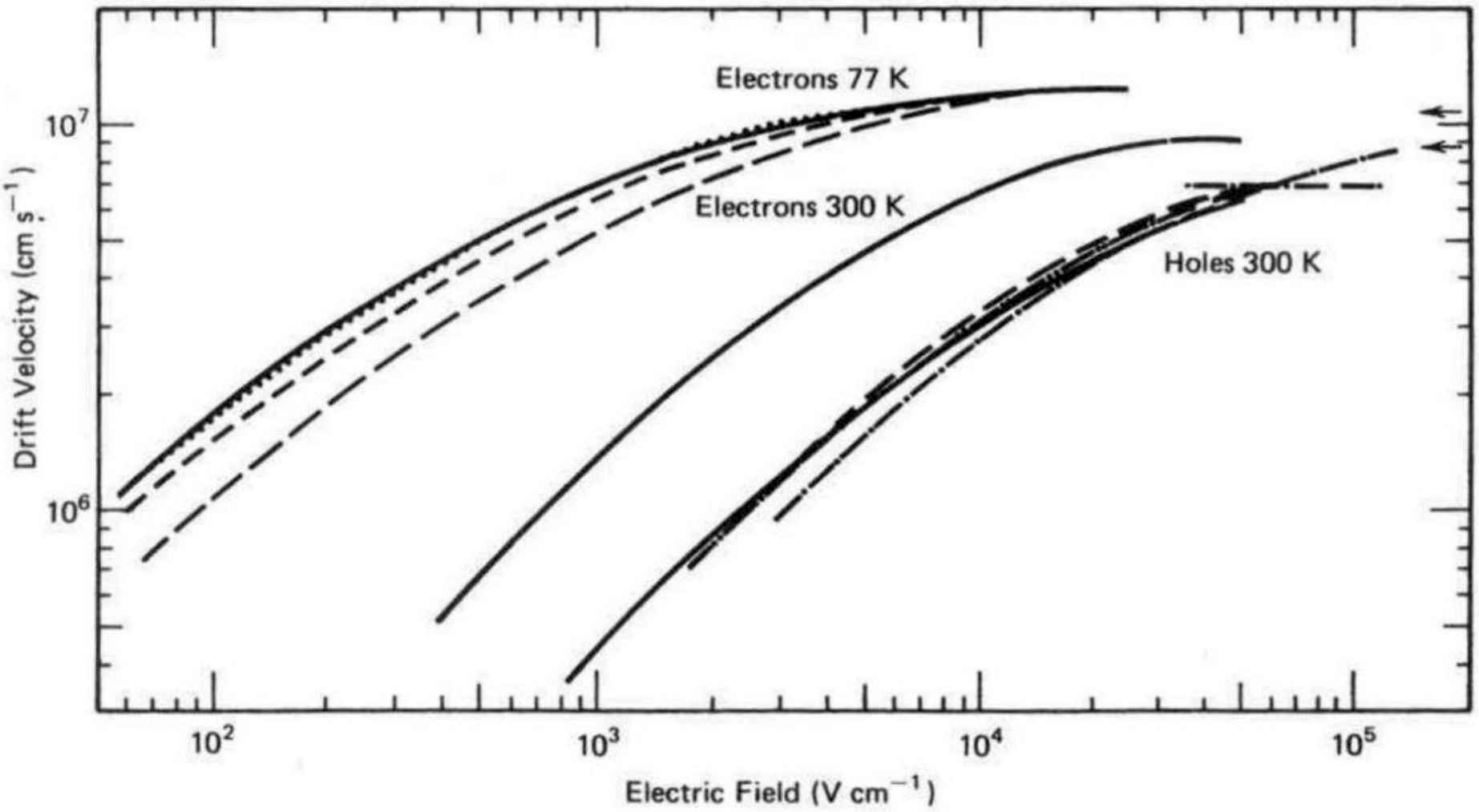



$$\frac{1}{\mu} = \frac{1}{\mu_L} + \frac{1}{\mu_I} + \frac{1}{\mu_S}$$

- $\mu$ = total mobility
- $\mu_L$ = mobility due to lattice scattering
- $\mu_I$ = mobility due to impurity scattering
- $\mu_S$ = mobility due to surface scattering (the dominating factor in MOS transistors)
- It is like for resistors in parallel: the smaller dominates!

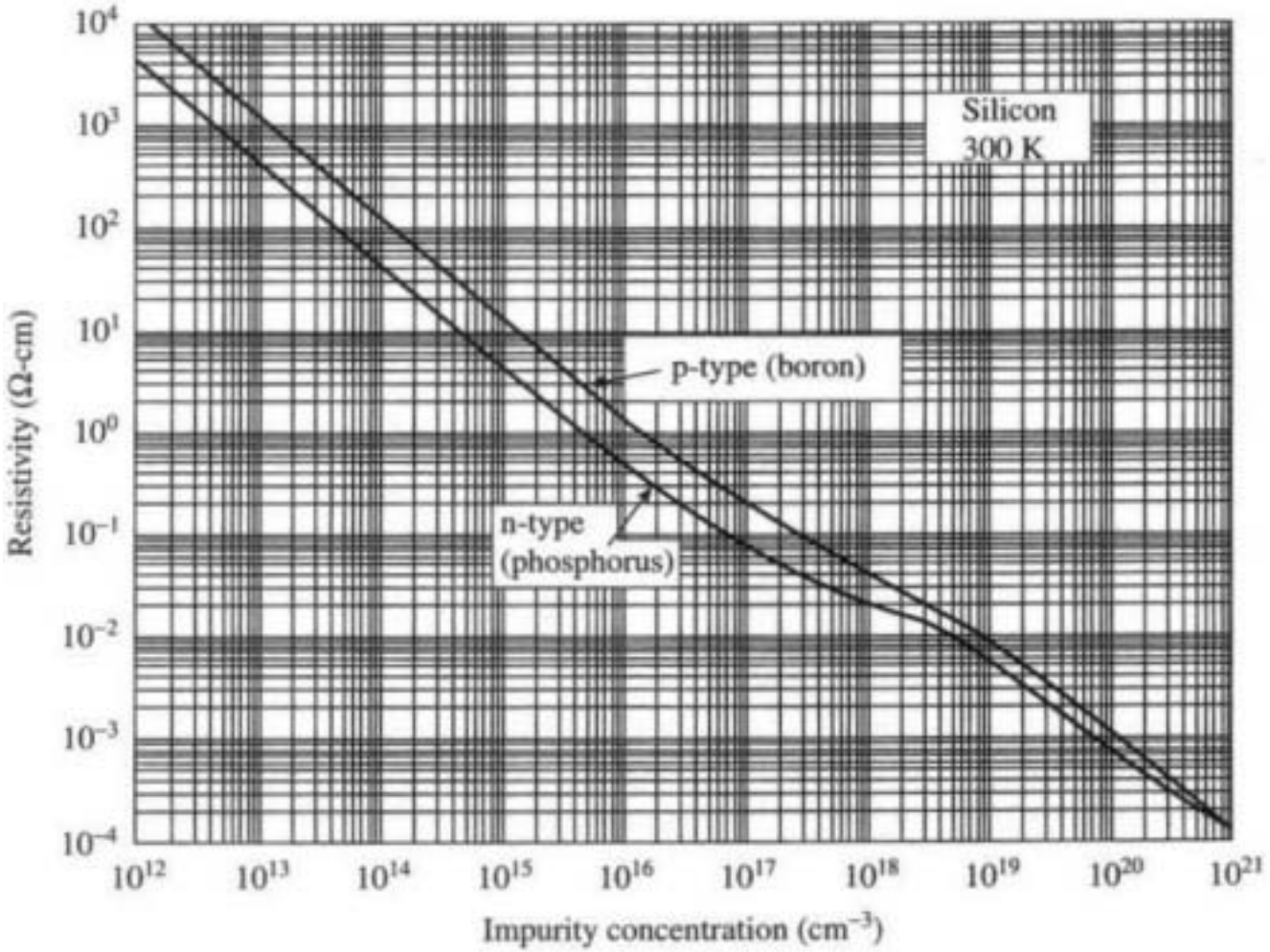
Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998, p. 20.

# Carrier velocity vs Electric Field




R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, 2nd Edition, John Wiley and Sons, 1986, p. 36.

# Resistivity vs doping




$$\rho = \frac{1}{q(n\mu_n + p\mu_p)}$$

**q = electronic charge**

**ρ = resistivity**

**n, p = carrier concentration**

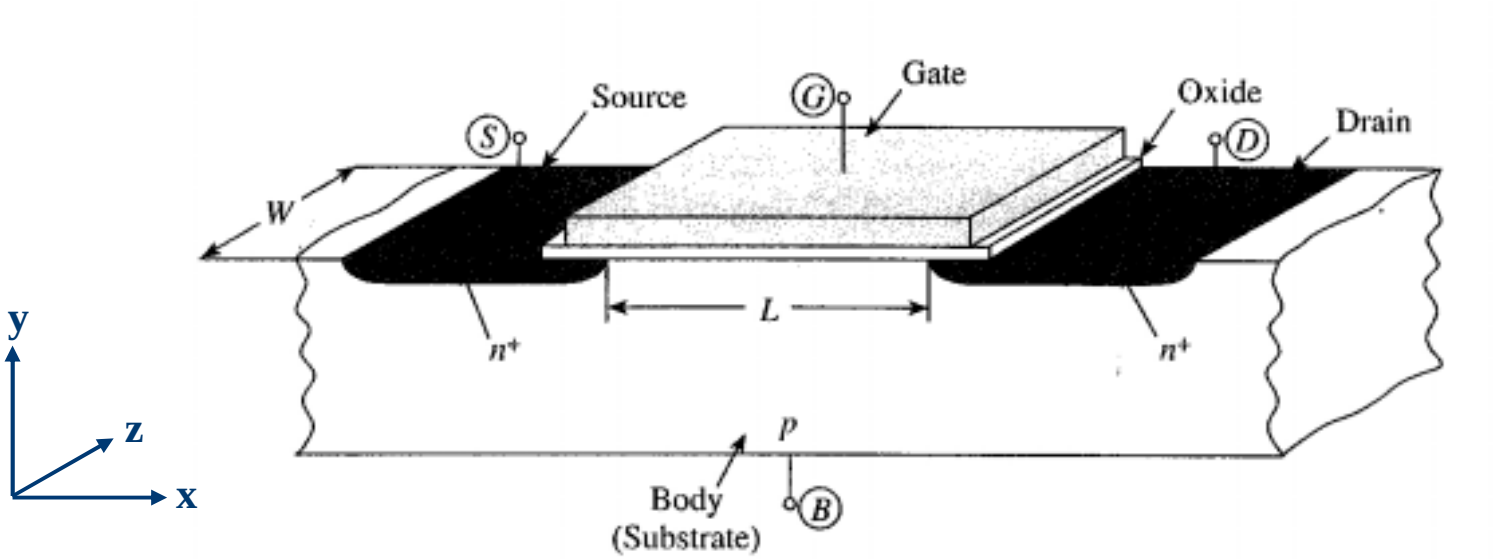
**$\mu_n$, $\mu_p$ = carrier mobility**

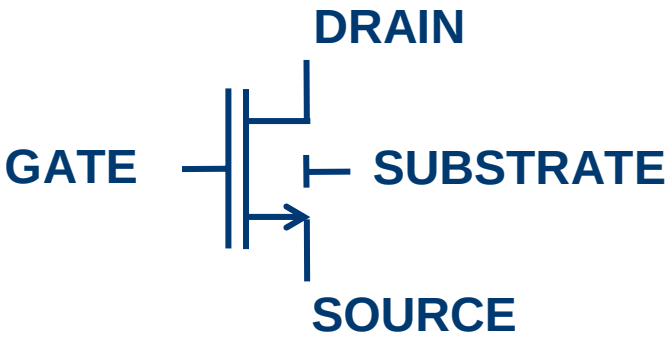
**Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998, p. 21.**

# Outline

- Semiconductor physics
  - Silicon and silicon dioxide properties
  - Band diagram concept
  - Intrinsic and doped semiconductors
  - Carrier mobility in silicon
- CMOS technology: an analog designer perspective
  - The MOS transistor
  - DC characteristics
  - Important formulas
  - Small signal equivalent circuit
  - Some cross sections of real integrated circuits

# The MOS transistor



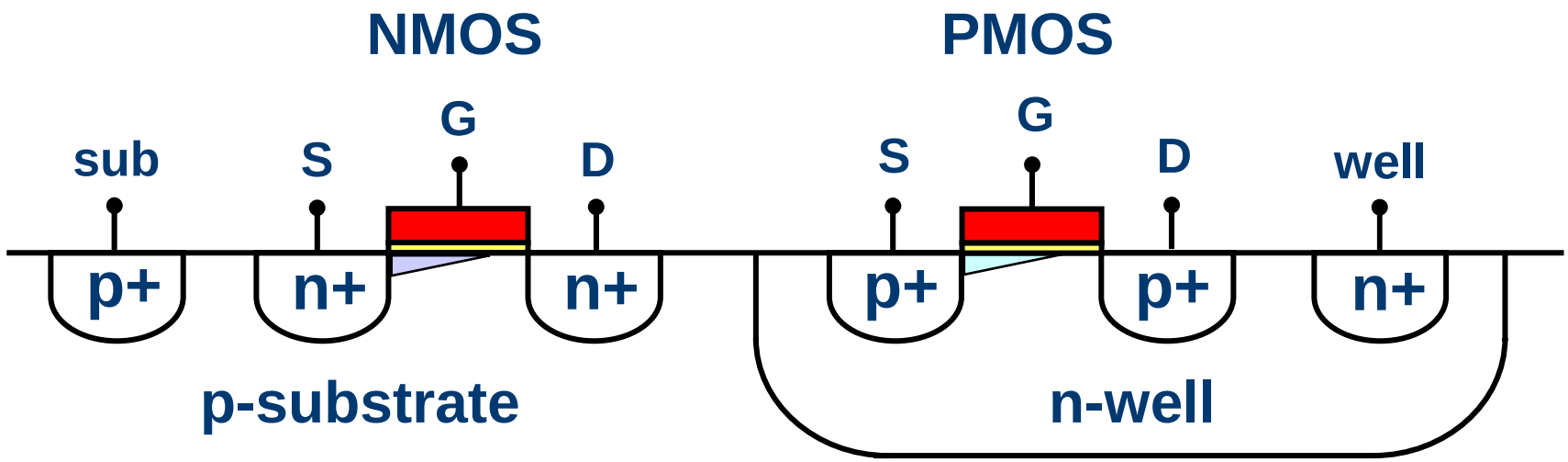

$$i_{DS} = g_m \cdot v_{GS}$$

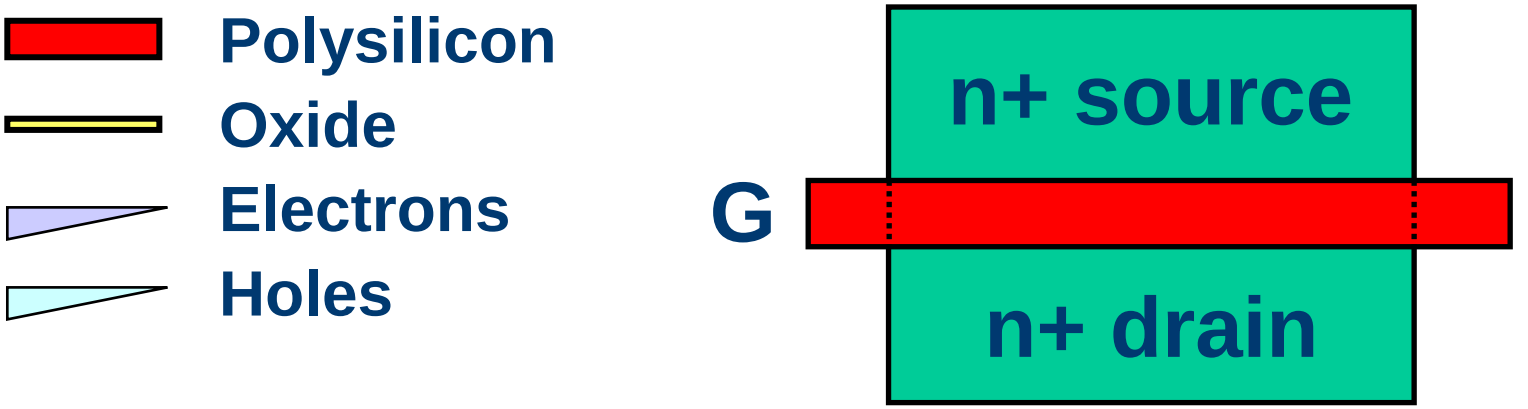
↓

**Transconductance**

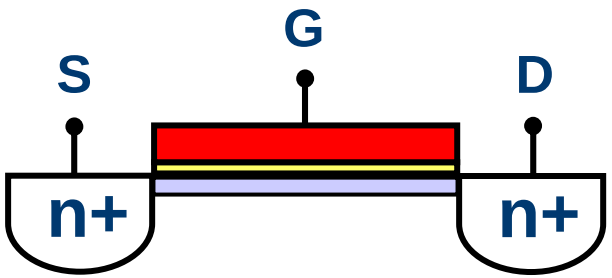
Y. Tsividis, *Operation and Modeling of The MOS Transistor*, 2nd edition, McGraw-Hill, 1999, p. 35

# CMOS technology

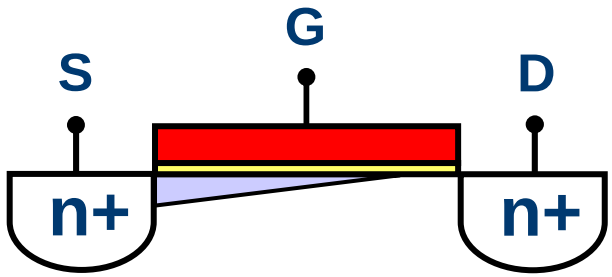


# Linear and Saturation regions

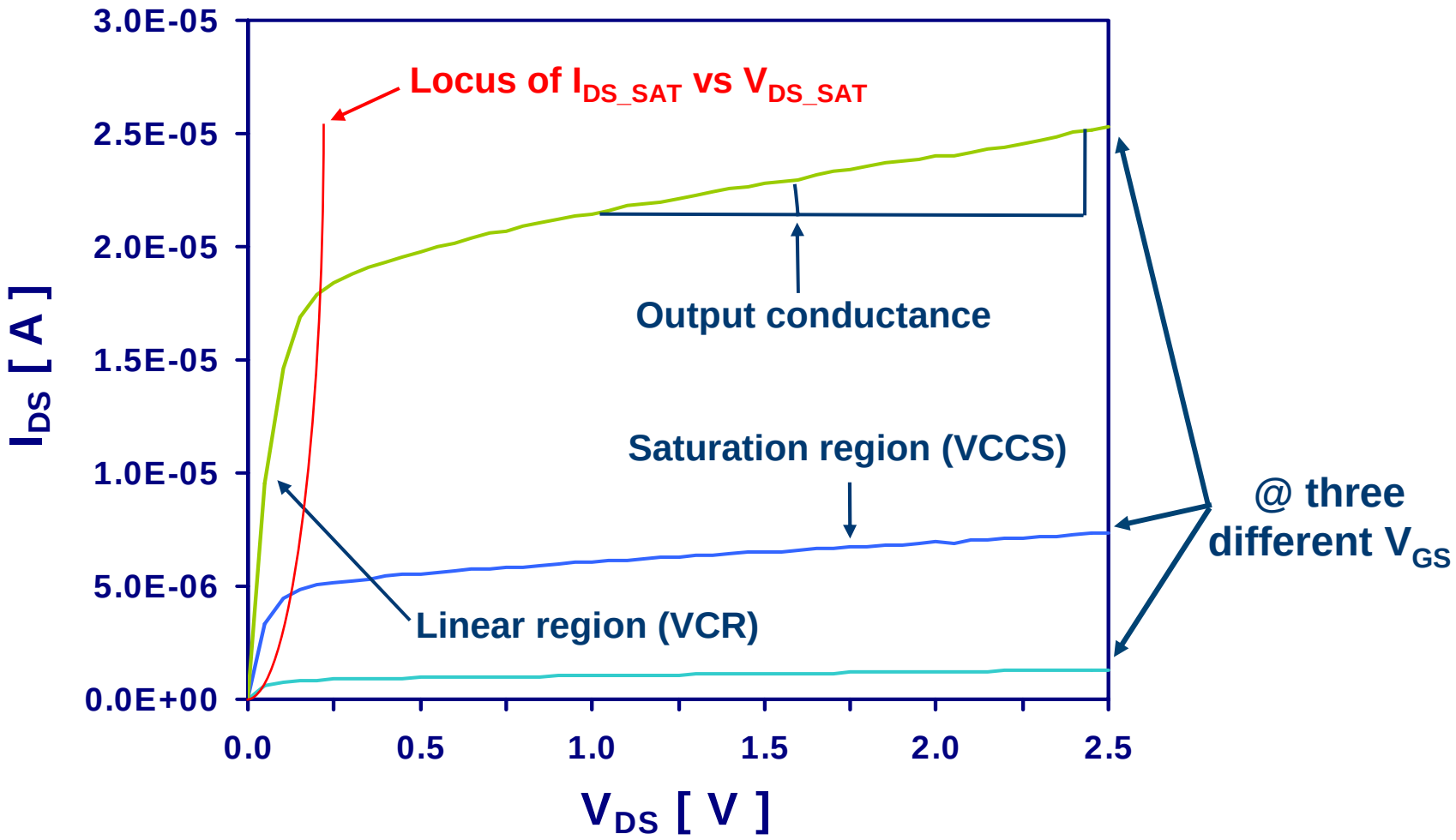



**LINEAR REGION (Low $V_{DS}$):**
**Electrons (in light blue) are attracted to the $SiO_2$ – Si Interface. A conductive channel is created between source and drain. We have a Voltage Controlled Resistor (VCR).**




**SATURATION REGION (High $V_{DS}$):**
**When the drain voltage is high enough the electrons near the drain are insufficiently attracted by the gate, and the channel is pinched off. We have a Voltage Controlled Current Source (VCCS).**

# Drain current vs Drain voltage



# Equations: strong inversion

**LINEAR REGION:**

$$V_{DS} < \frac{V_{GS} - V_T}{n} = V_{DS\_SAT}$$

$$I_{DS} = \beta \left(V_{GS} - V_T - \frac{nV_{DS}}{2}\right)V_{DS}$$

**Transconductance:** $g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \beta V_{DS}$

**SATURATION REGION:**

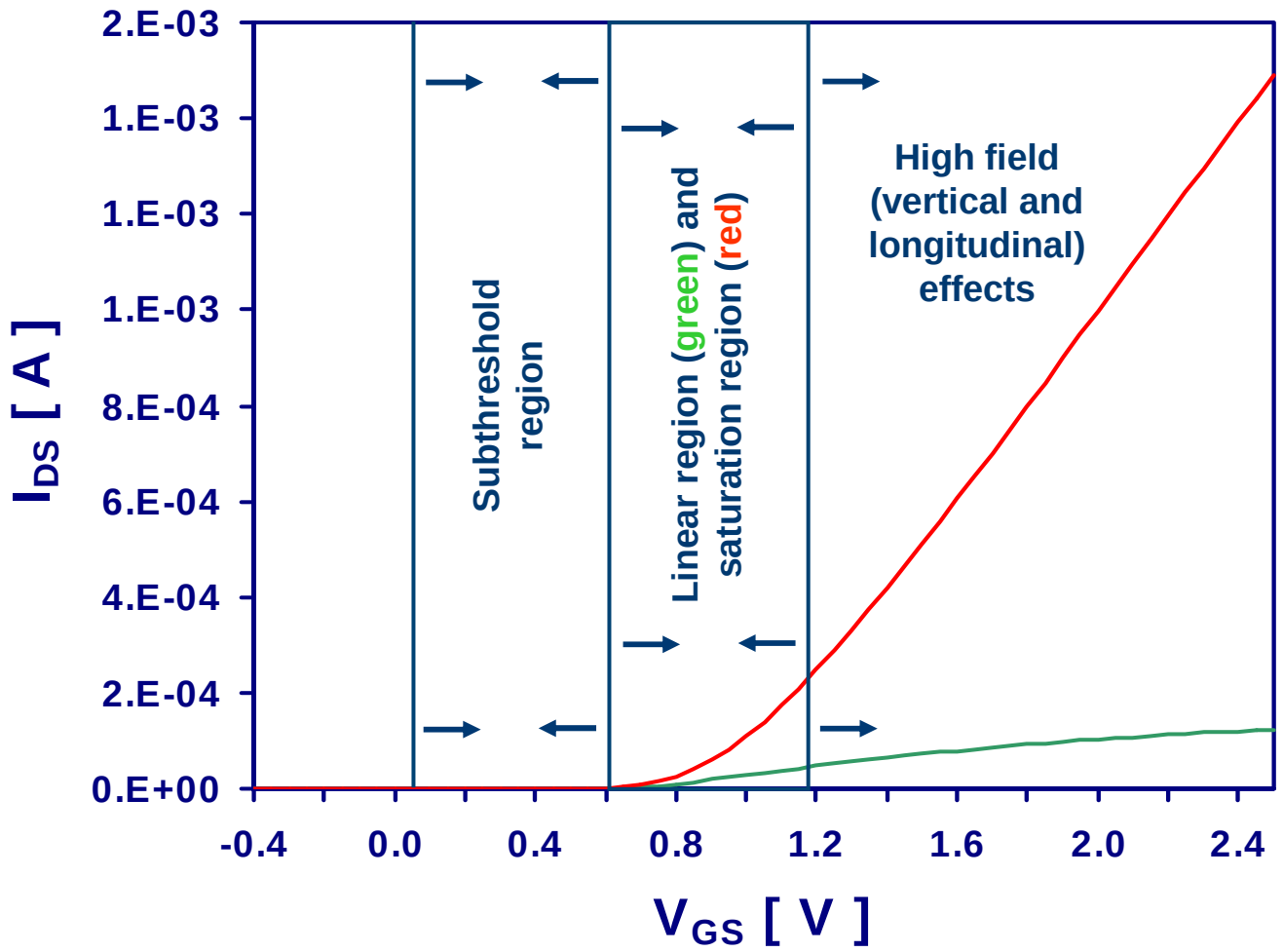
$$V_{DS} > \frac{V_{GS} - V_T}{n} = V_{DS\_SAT}$$

$$I_{DS} = \frac{\beta}{2n}(V_{GS} - V_T)^2$$

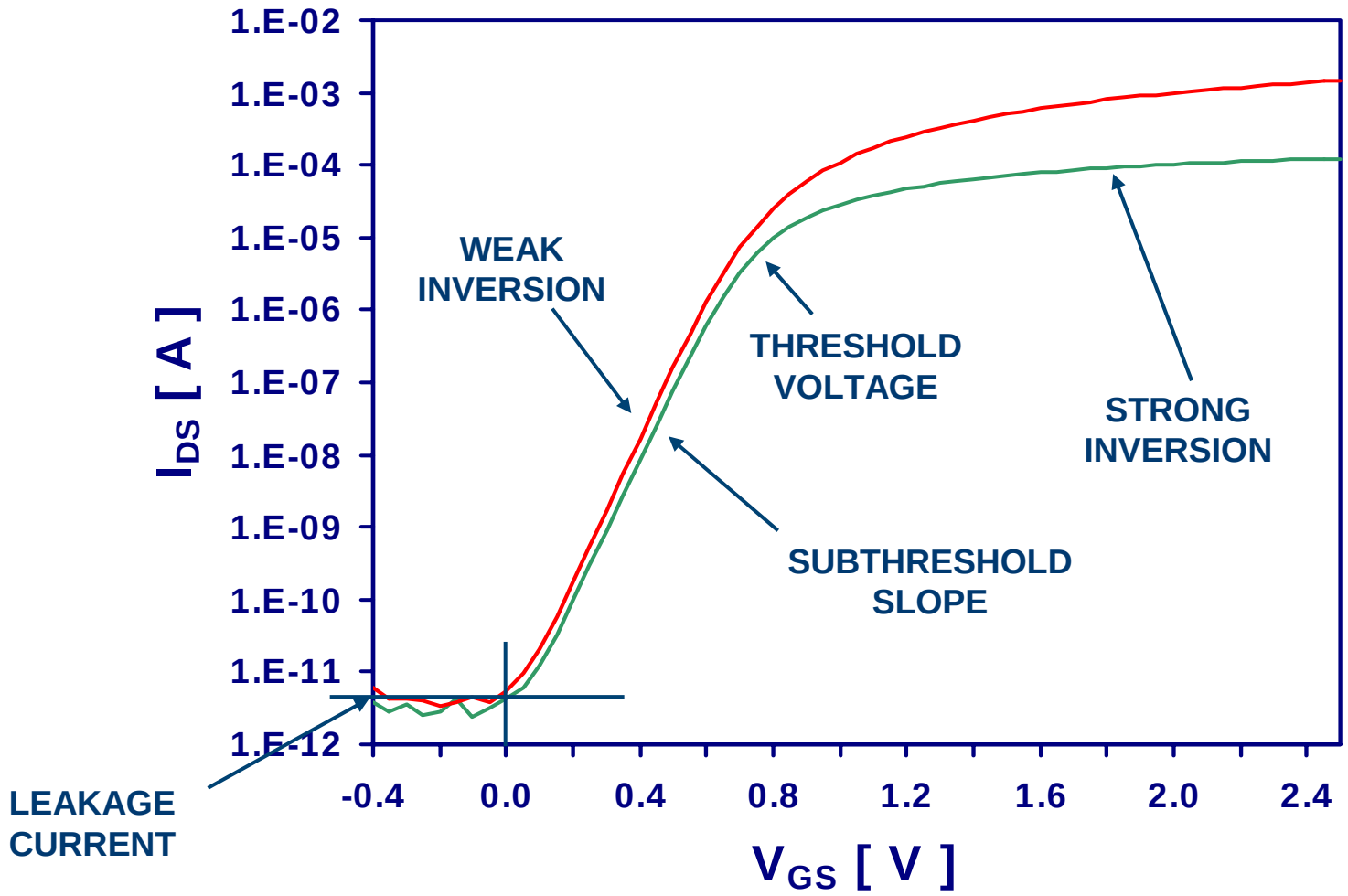
**Transconductance:** $g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\beta}{n}(V_{GS} - V_T) = \sqrt{2\frac{\beta}{n} I_{DS}}$

$$n = \frac{g_m + g_{mb}}{g_m} \approx 1.x \qquad g_{mb} = \frac{\partial I_{DS}}{\partial V_{BS}} \qquad \beta = \mu C_{ox} \frac{W}{L} \qquad C_{ox} = \frac{\varepsilon_{SiO_2}}{t_{ox}}$$

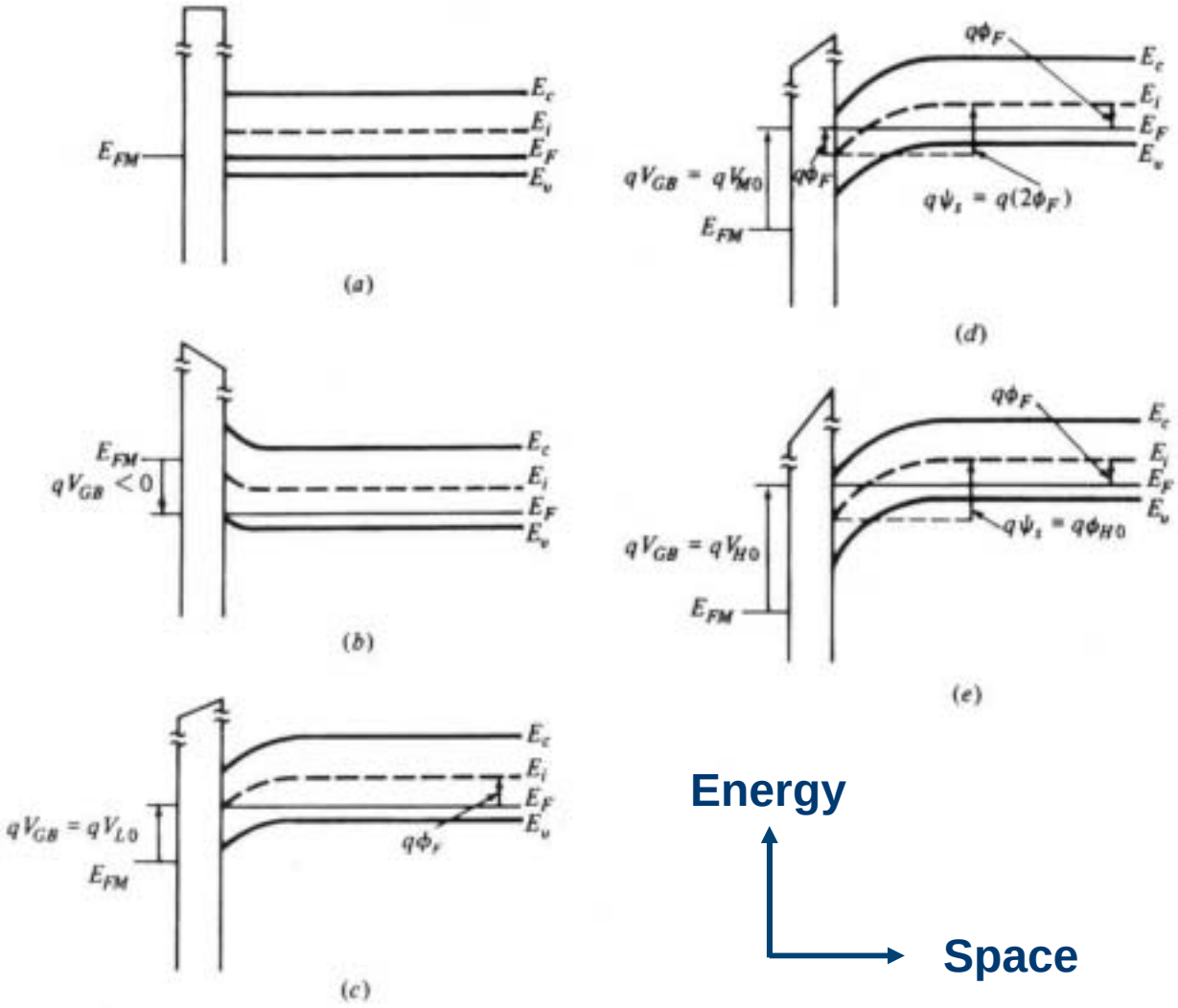
# Drain current vs Gate voltage



# Log($I_{DS}$) vs $V_{GS}$



# Band diagrams of a MOS structure




**Diagrams assuming $V_{FB} = 0$**

**(a) Flat-band condition**

**(b) Accumulation**

**(c) Onset of weak inversion**

**(d) Onset of moderate inversion**

**(e) Onset of strong inversion**

$$n = n_i \cdot e^{\frac{E_F - E_i}{kT}}$$

$$p = n_i \cdot e^{\frac{E_i - E_F}{kT}}$$

**Tip: think at electrons as if they were little balls and holes little bubbles…**

Y. Tsividis, *Operation and Modeling of The MOS Transistor*, 2nd edition, McGraw-Hill, 1999, p. 576

# Equations: weak inversion

$$I_{DS} = I_{D0} \frac{W}{L} e^{\frac{V_{GS}}{n\phi_t}} \left(1 - e^{-\frac{V_{DS}}{n\phi_t}}\right)$$

If $V_{DS} > 4n\phi_t$ then the drain current does not depend on $V_{DS}$ any longer (saturation)

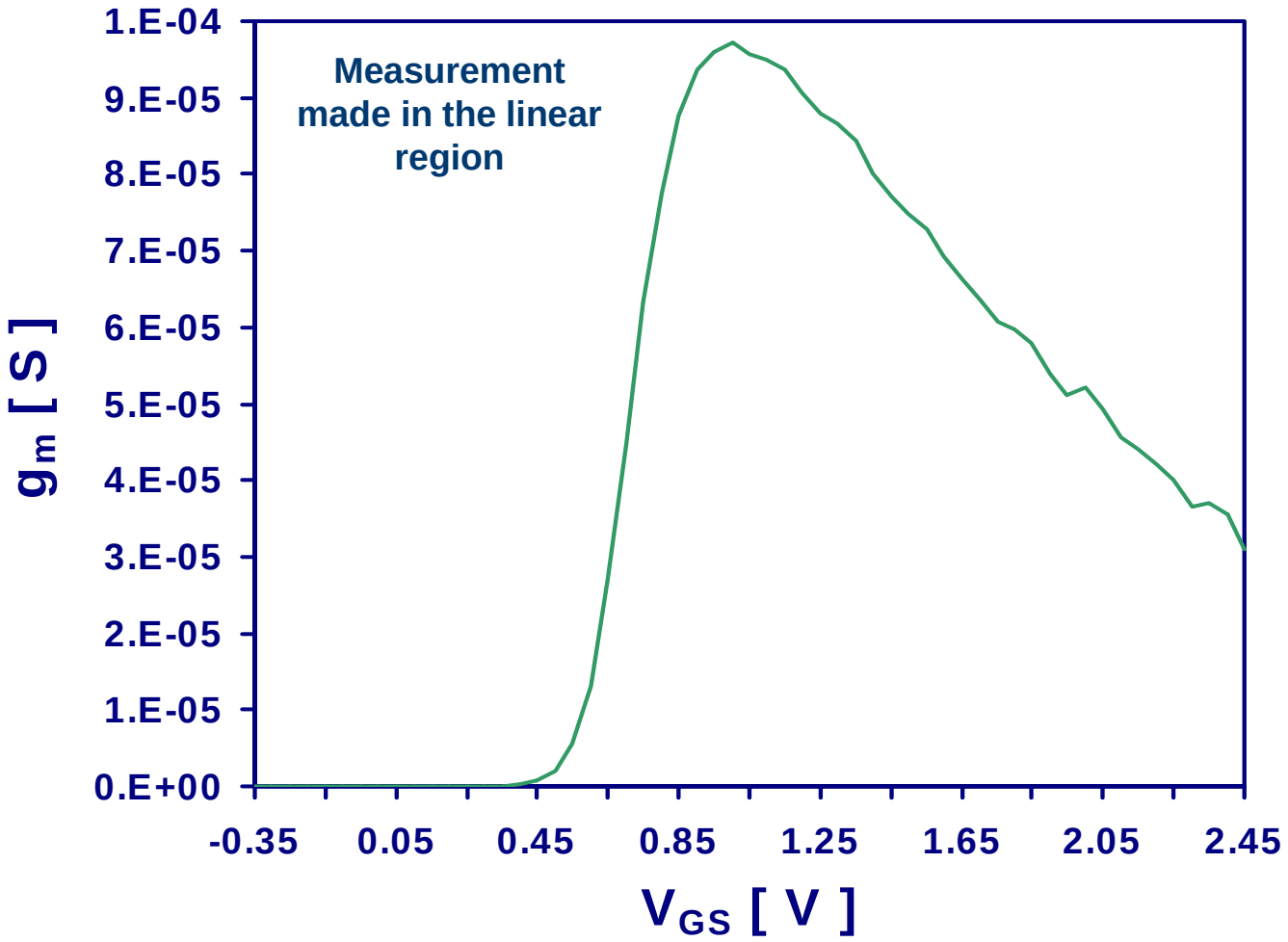
$$I_{DS} = I_{D0} \frac{W}{L} e^{\frac{V_{GS}}{n\phi_t}}$$

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{I_{DS}}{n\phi_t}$$

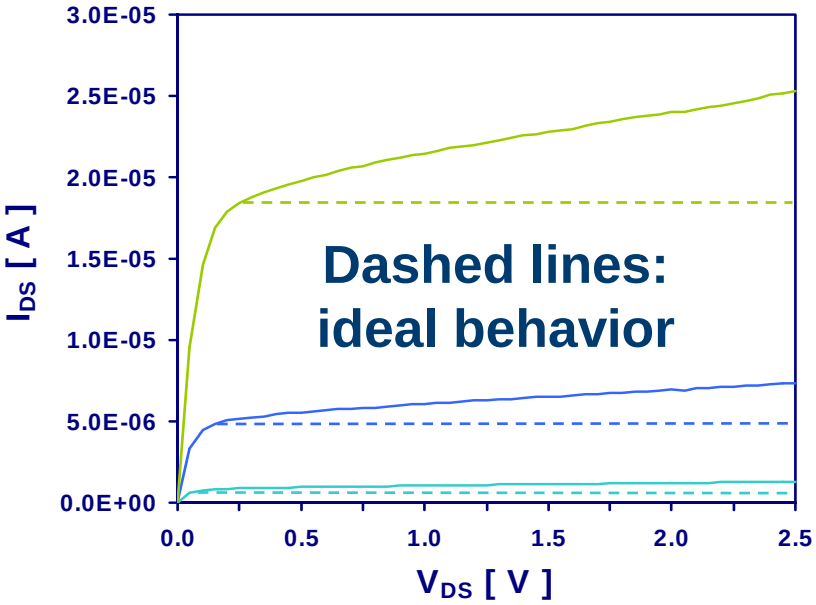
**Almost like a bipolar transistor!**

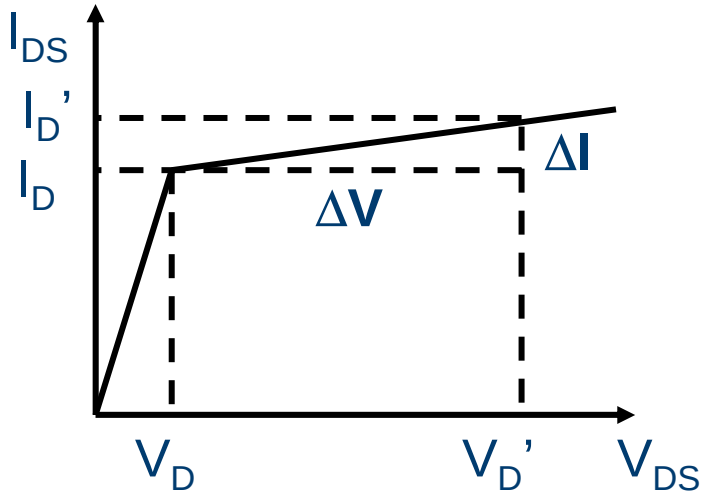
$$\phi_t = \frac{kT}{q} \approx 25 \text{ mV } @ \text{ 300 K}$$

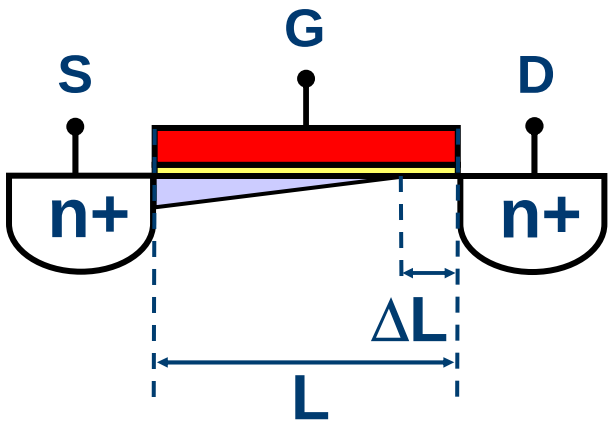
# Transcond. vs Gate voltage



# Output conductance

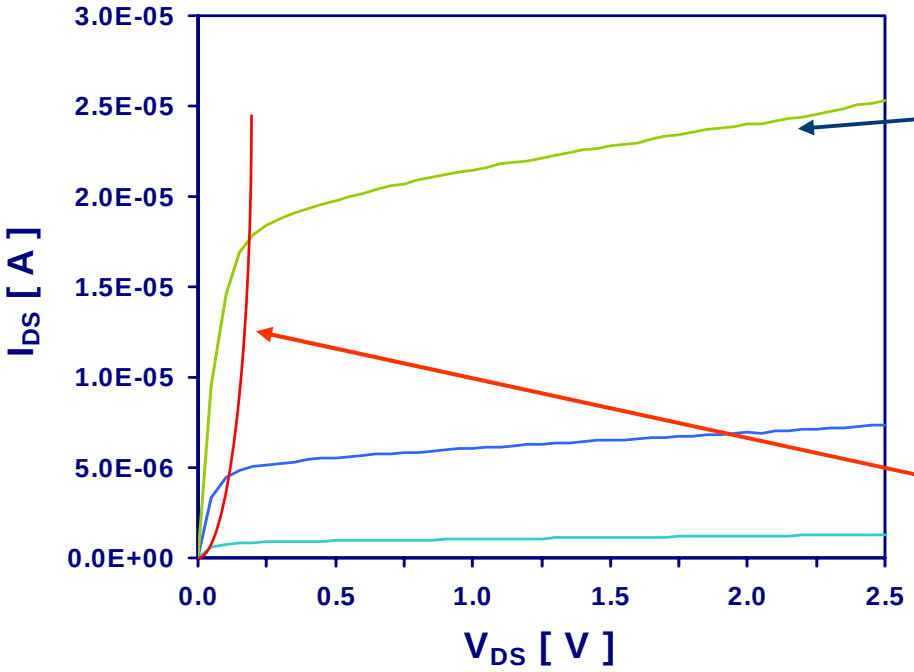



$$G_{out} = \frac{\Delta I}{\Delta V} = \frac{I_D}{\Delta V} \cdot \frac{\Delta L}{L - \Delta L}$$

# Equations: output conductance




$$I_{DS} = \frac{\beta}{2n}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$$V_{DS\_SAT} = \frac{V_{GS} - V_T}{n}$$

$$I_{DS\_SAT} = \frac{\beta}{2n}(V_{GS} - V_T)^2 = \frac{\beta}{2} n V_{DS\_SAT}^2$$

$$g_{out} = g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \lambda \cdot I_{DS\_SAT}$$

$$r_0 = \frac{1}{g_{ds}} = \frac{1}{\lambda \cdot I_{DS\_SAT}} = \frac{V_E \cdot L}{I_{DS\_SAT}}$$

$$\lambda = \frac{1}{V_{DS}} \cdot \frac{\Delta L}{L - \Delta L} \quad \text{where } \Delta L = f(V_{DS}, N_{Doping})$$

# Equations: addendum

**Bulk effect**

$$\Delta V_T = \gamma \cdot \left( \sqrt{V_{sb} + \phi_{Si}} - \sqrt{\phi_{Si}} \right) \qquad \gamma = \frac{\sqrt{2q\varepsilon_{Si}N_a}}{C_{ox}}$$

**Source parasitic resistance**

$$g_m' = \frac{g_m}{1 + g_m R_S}$$

**Vertical electric field effect**

$$\mu = \frac{\mu_0}{1 + \theta (V_{GS} - V_T)}$$

**Maximum frequency**

$$f_{max} = \frac{1}{2\pi} \frac{g_m}{C_{gs}} = \frac{1}{2\pi} \frac{\mu}{nL^2} (V_{GS} - V_T) \qquad \text{in s.i.}$$

K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, 1994, Chapter 1

# Equations: velocity saturation

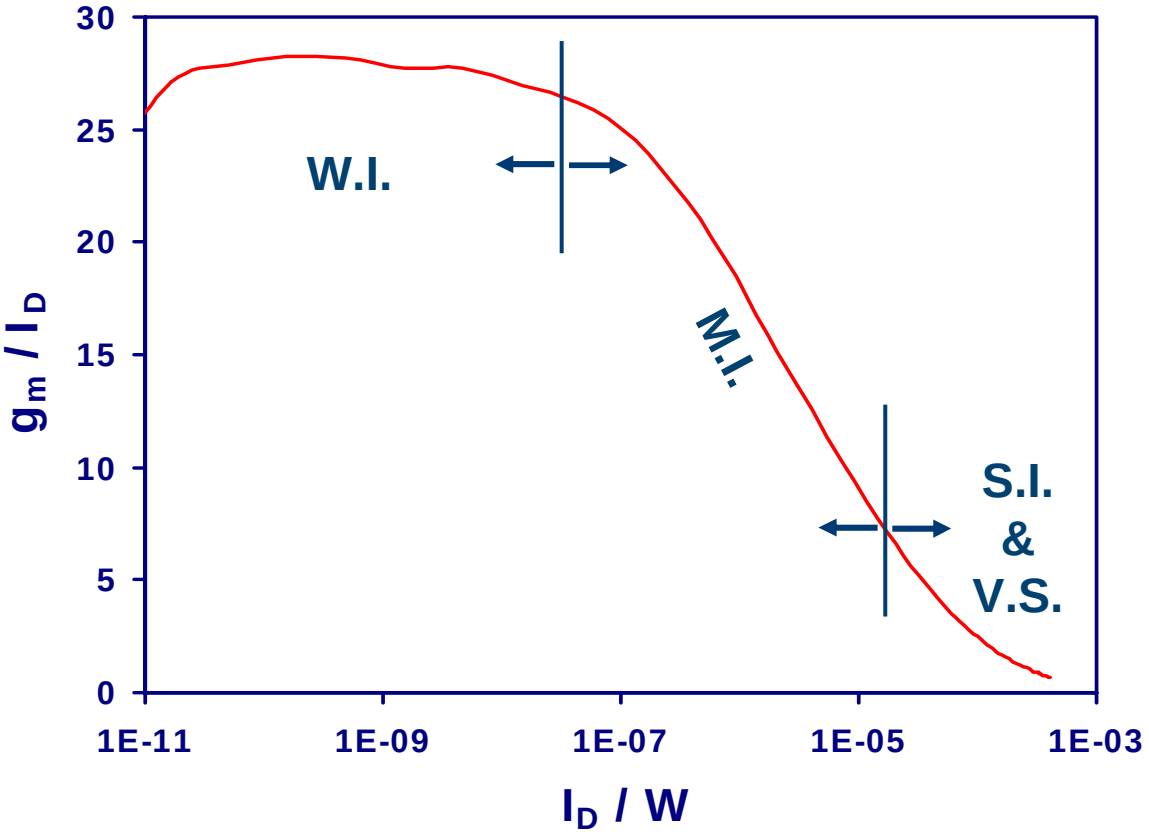
**For low values of the longitudinal electric field, the velocity of the carriers increases proportionally to the electric field (and the proportionality constant is the mobility). For high values of the electric field (3 V/μm for electrons and 10 V/μm for holes) the velocity of the carriers saturates.**

$$I_{DS\_v.s.} = WC_{ox}v_{sat}(V_{GS} - V_T) \quad \text{with } v_{sat} = 10^7 \frac{cm}{s}$$

$$g_{m\_v.s.} = WC_{ox}v_{sat}$$

$$f_{max\_v.s.} = \frac{1}{2\pi}\frac{g_m}{C_{gs}} = \frac{1}{2\pi}\frac{v_{sat}}{L}$$

# $g_m / I_D$ vs $\log(I_D / W)$




**Weak Inversion (W.I.)**

$$g_m = \frac{I_{DS}}{n\phi_t} \rightarrow \frac{g_m}{I_D} = \frac{1}{n\phi_t}$$

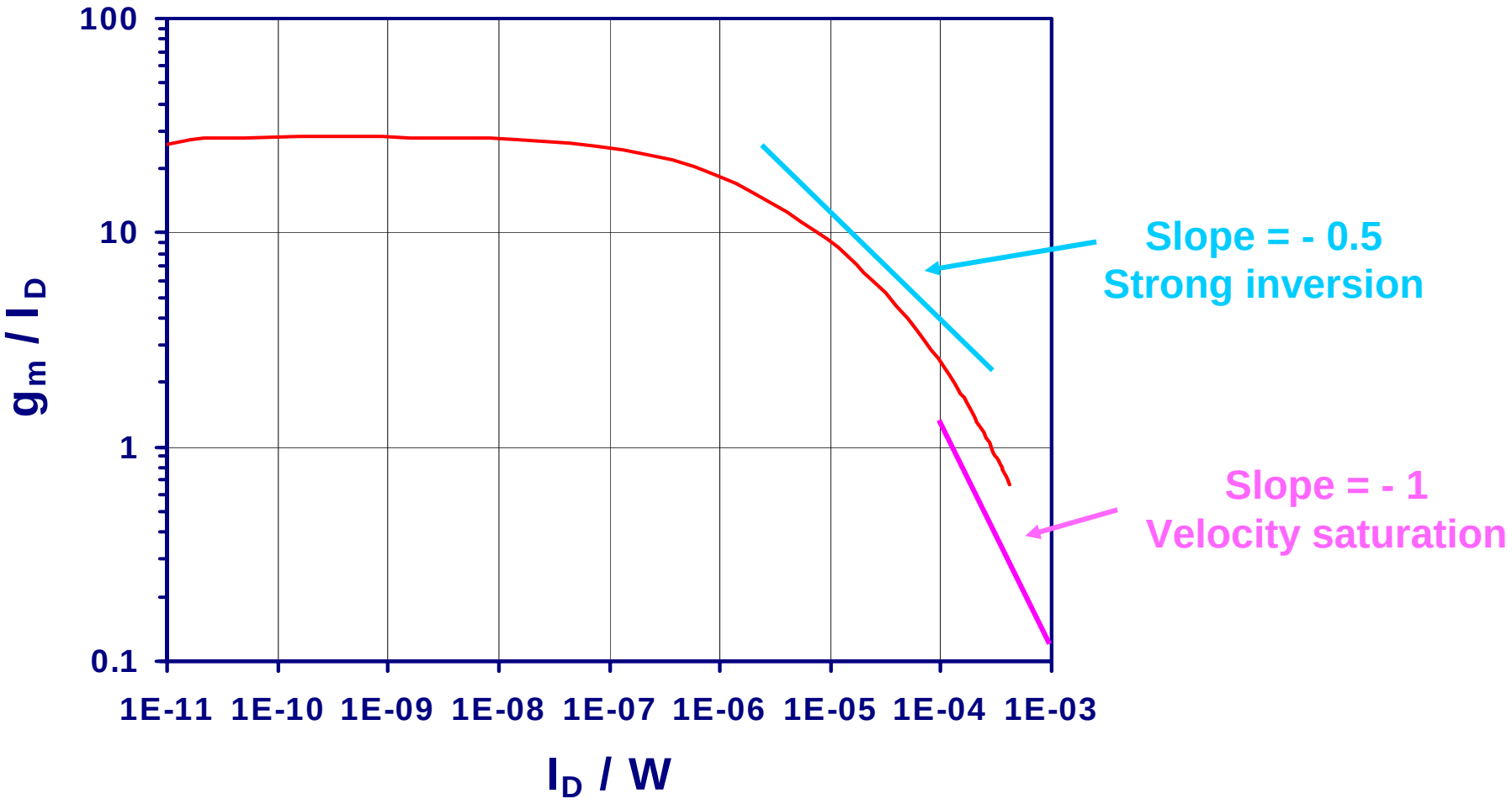
**Strong Inversion (S.I.)**

$$g_m = \sqrt{2\frac{\beta}{n}I_{DS}} \rightarrow \frac{g_m}{I_D} = \sqrt{2\frac{\beta}{n}\frac{1}{I_{DS}}}$$

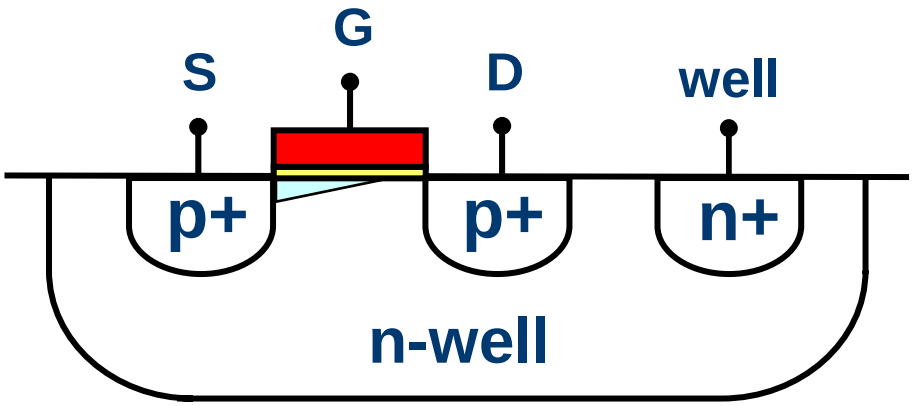
**Velocity Saturation (V.S.)**

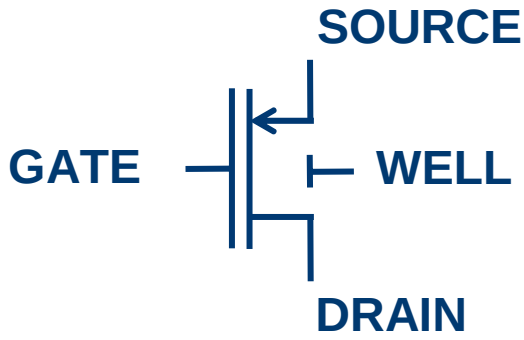
$$g_m = WC_{ox}v_{sat} \rightarrow \frac{g_m}{I_{DS}} = \frac{WC_{ox}v_{sat}}{I_{DS}}$$

# $Log(g_m / I_D)$ vs $log(I_D / W)$



# The poor PMOS transistor

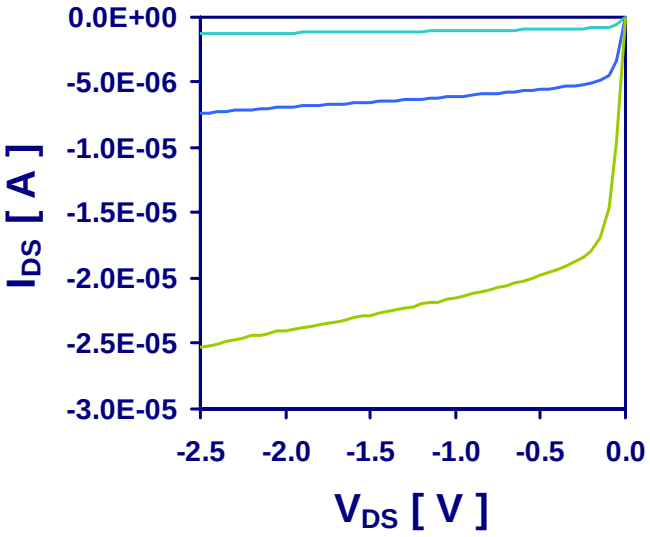



$V_T < 0$ V

$V_{GS} < 0$ V

$I_{DS} < 0$ V

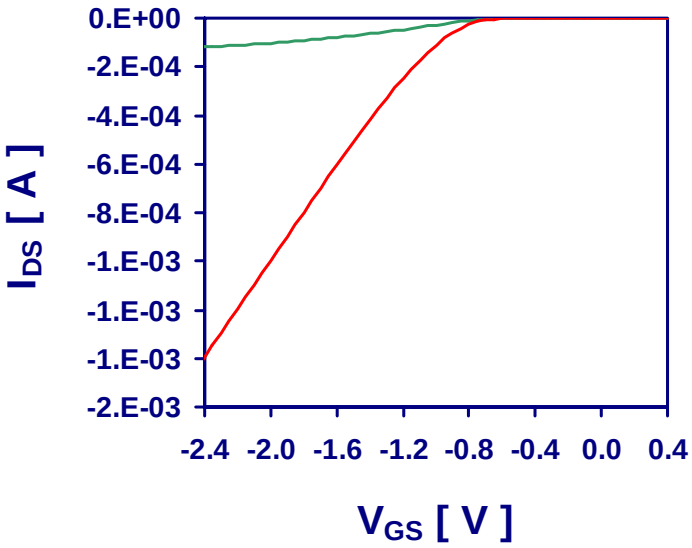



$$I_{DS} = -\frac{\beta}{2n}(V_{GS} - V_T)^2$$

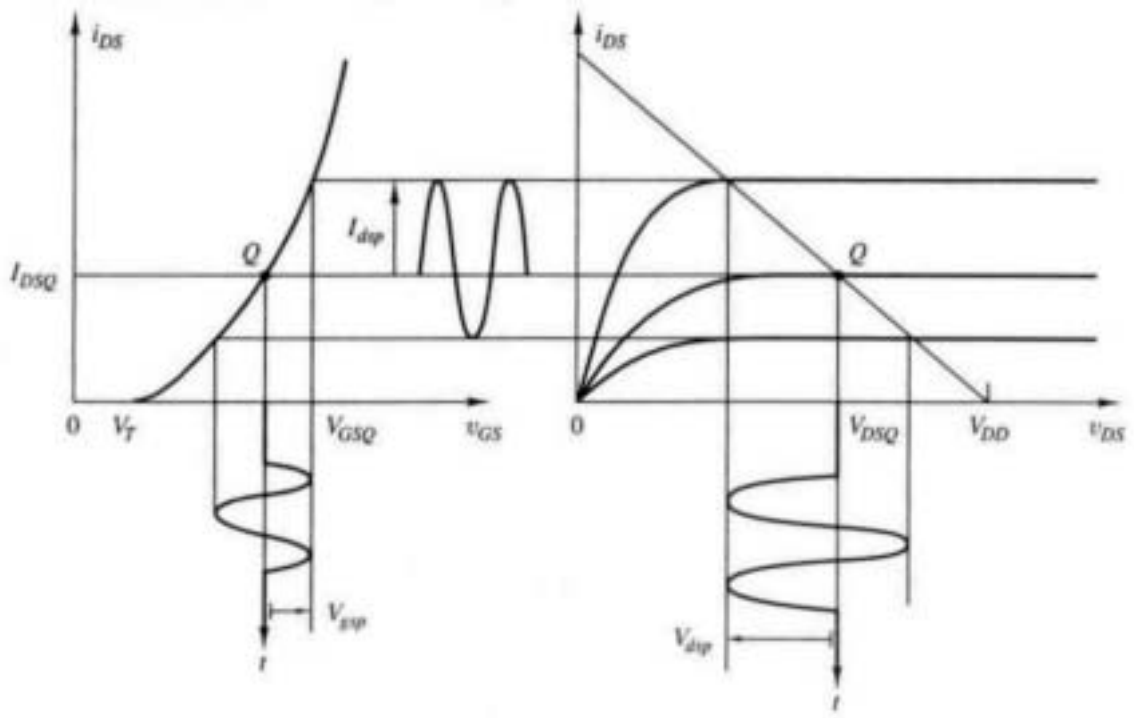
$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} =$$

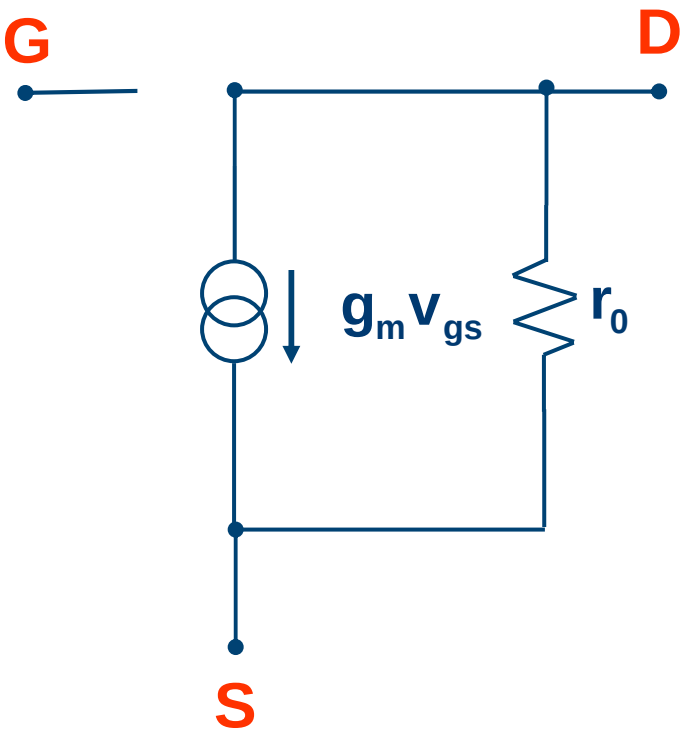
$$= -\frac{\beta}{n}(V_{GS} - V_T) =$$

$$= \sqrt{-2\frac{\beta}{n} I_{DS}}$$



# Small-signal equivalent circuit



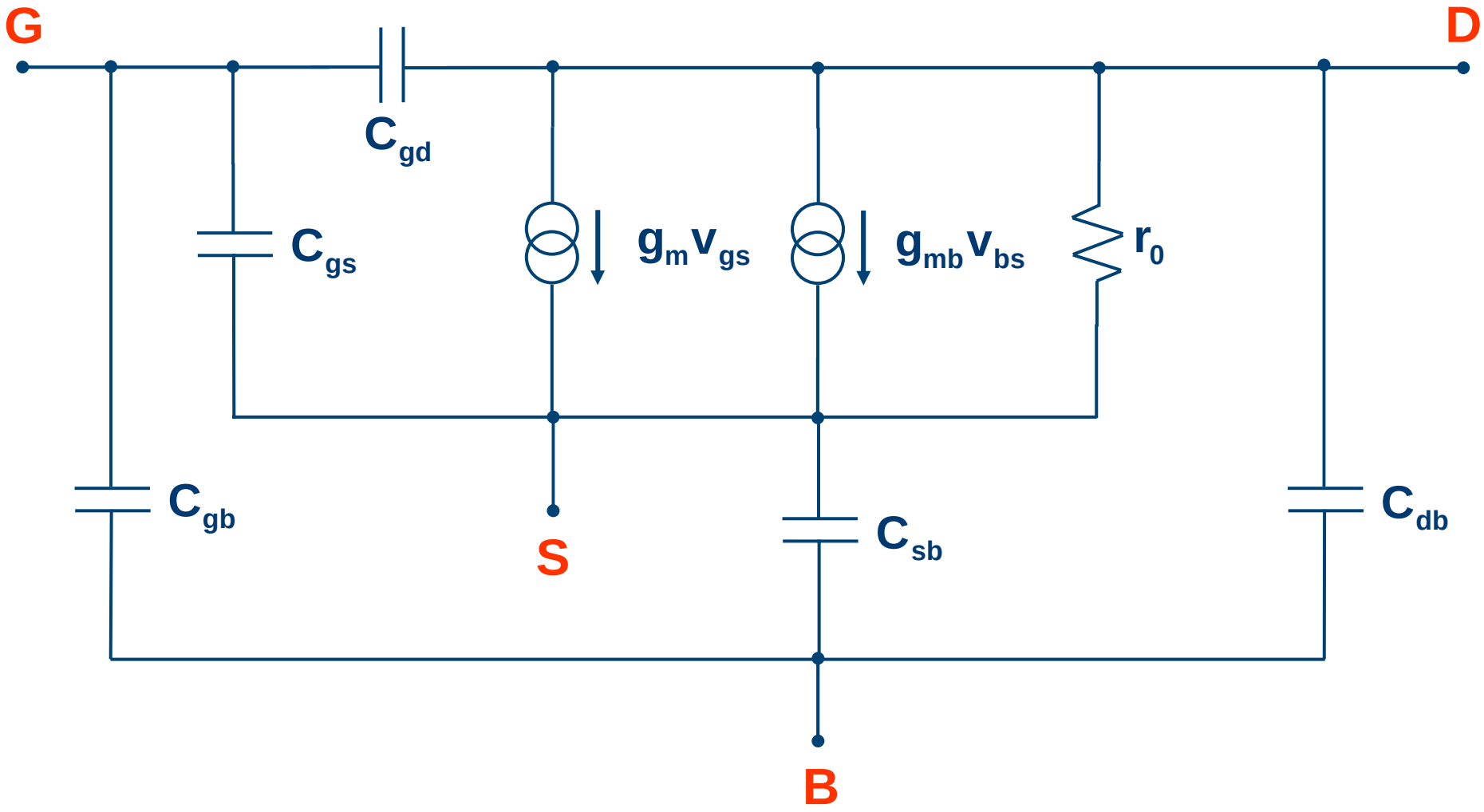




$$I_{DSQ} = \frac{\beta}{2n}(V_{GSQ} - V_T)^2 \longrightarrow \text{This equation fixes the bias point}$$

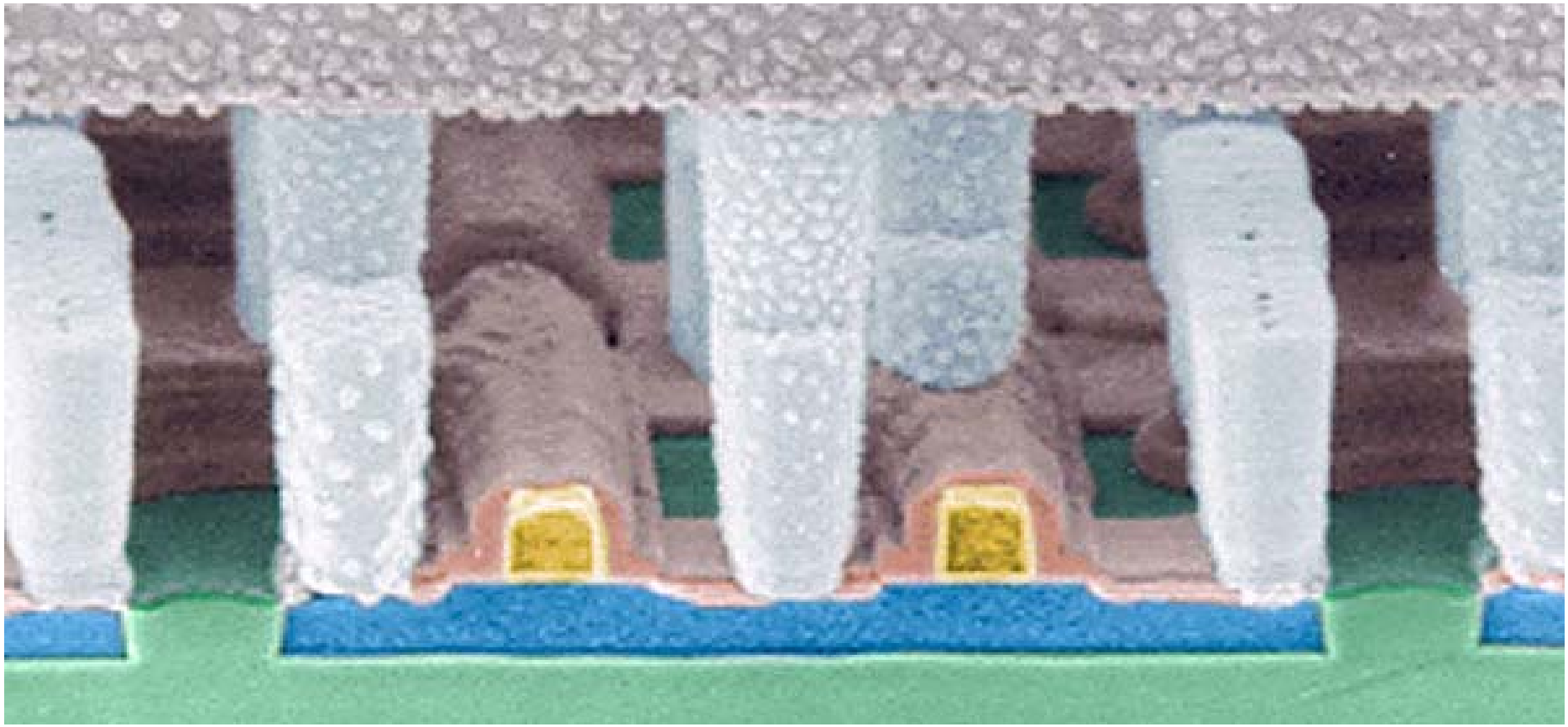
$$i_{DS} = g_m \cdot v_{GS} \longrightarrow \text{This equation defines the small signal behavior}$$

K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, 1994, p. 24.

# Small-signal equivalent circuit



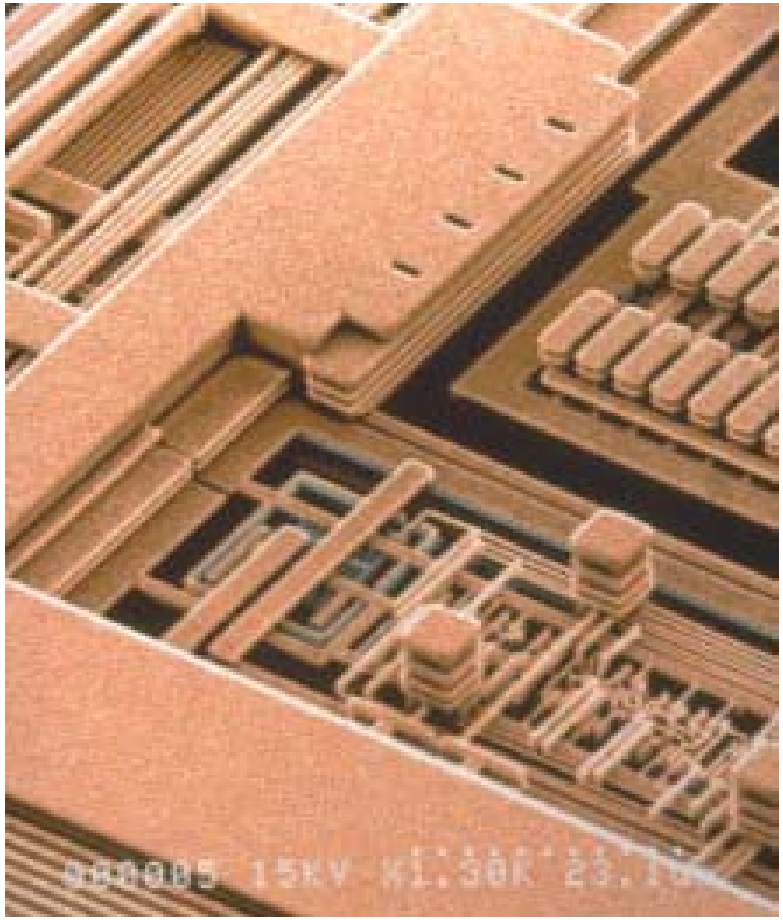
# The real thing!

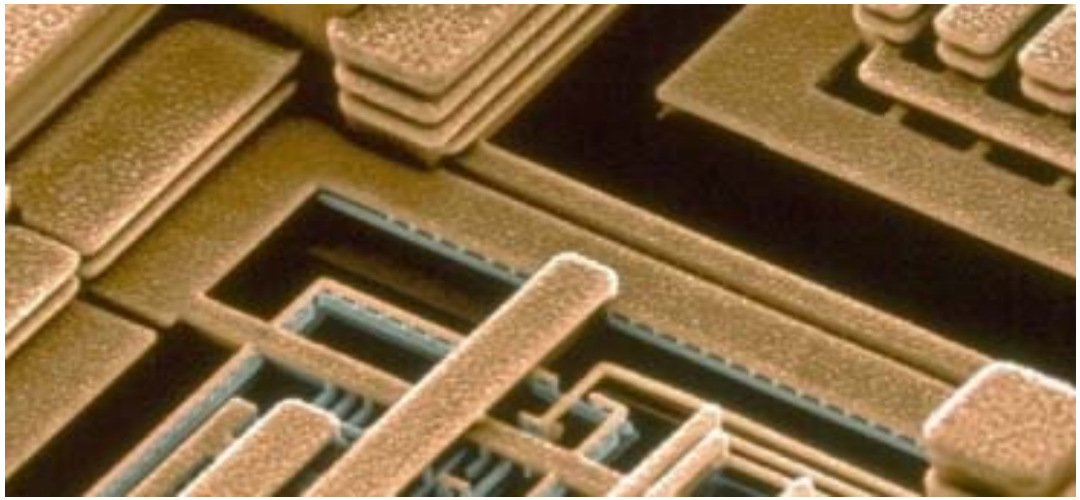


**SOI technology from IBM**

**http://www-3.ibm.com/chips/gallery/**

# The real thing!

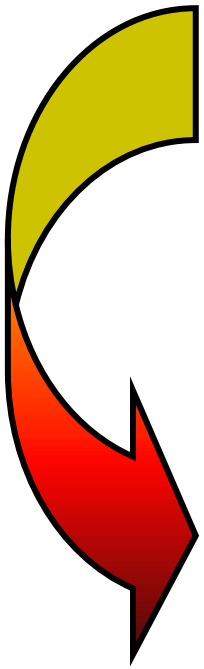




## Metallization examples

**http://www-3.ibm.com/chips/gallery/**

# Why is CMOS so widespread?



- **The IC market is driven by digital circuits (memories, microprocessors, …)**
- **Bipolar logic and NMOS - only logic had a too high power consumption per gate**
- **Progress in the manufacturing technology made CMOS technologies a reality**
- **Modern CMOS technologies offer excellent performance (especially for digital): high speed, low power consumption, VLSI, low cost, high yield**

**CMOS technologies occupies an increasing portion of the IC market**

**… and this is why we will only talk about CMOS.**