



ICTP Microprocessor Laboratory  
African Regional Course on Advanced VLSI Design Techniques  
Kwame Nkrumah University of Science and Technology, Kumasi, Ghana  
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# Scaling Impact on Analog Circuit Performance



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# Outline

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- Scaling down of CMOS technologies
  - Moore's law
  - An example: Intel Microprocessors
  - The International Technology Roadmap for Semiconductors: what will happen in the next 15 years?
- How scaling works for devices and interconnections
- Scaling impact on noise
- Scaling impact on matching
- Scaling impact on radiation tolerance
- Analog performance of submicron processes
- Substrate noise in mixed-mode integrated circuits

# Moore's law



**1965: Number of Integrated Circuit components will double every year**

G. E. Moore, "Cramming More Components onto Integrated Circuits", *Electronics*, vol. 38, no. 8, 1965.

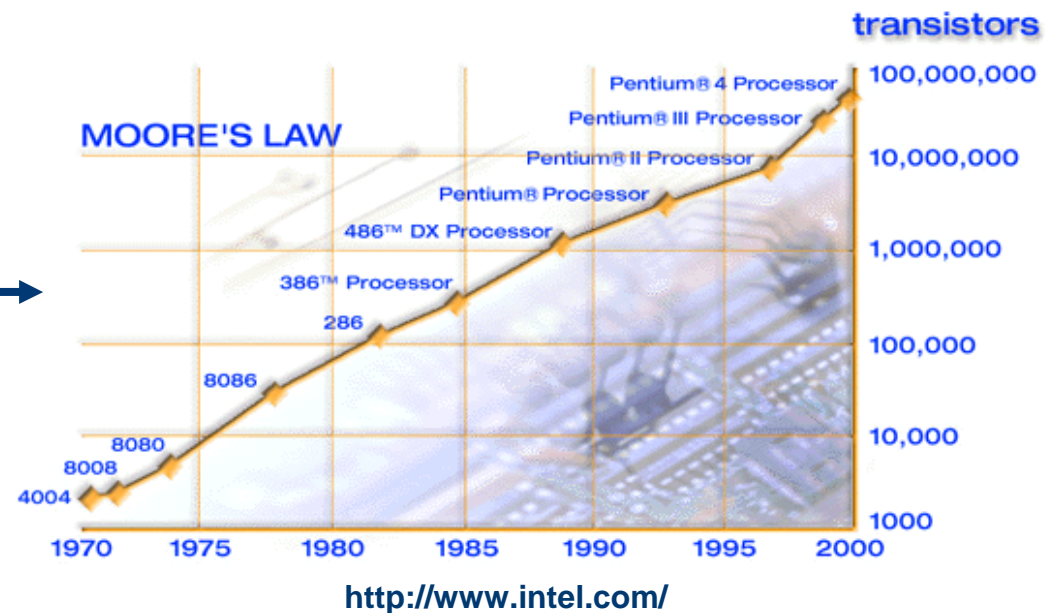
**1975: Number of Integrated Circuit components will double every 18 months**

G. E. Moore, "Progress in Digital Integrated Electronics", *Technical Digest of the IEEE IEDM* 1975.

**1996: The definition of "Moore's Law" has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line. I don't want to do anything to restrict this definition. - G. E. Moore, 8/7/1996**

P. K. Bondyopadhyay, "Moore's Law Governs the Silicon Revolution", *Proc. of the IEEE*, vol. 86, no. 1, Jan. 1998, pp. 78-81.

**An example:  
Intel's Microprocessors**





# The **intel.** Microprocessors

**4004**  
**11 / 1971**  
2300  
10  $\mu\text{m}$   
108 KHz



**8008**  
**04 / 1972**  
3500  
10  $\mu\text{m}$   
200 KHz



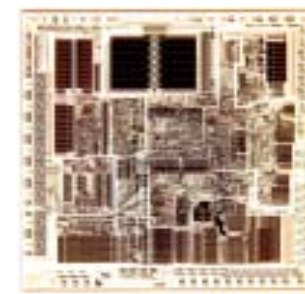
**8080**  
**04 / 1974**  
4500  
6  $\mu\text{m}$   
2 MHz



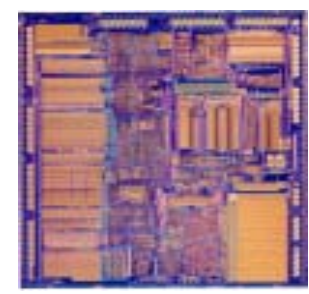
**8088**  
**06 / 1979**  
29000  
3  $\mu\text{m}$   
8 MHz



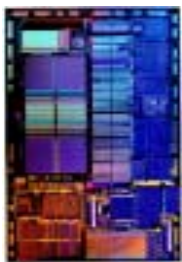
**80286**  
**02 / 1982**  
134000  
1.5  $\mu\text{m}$   
12 MHz



**Intel386™**  
**10 / 1985**  
275000  
1  $\mu\text{m}$   
16 MHz



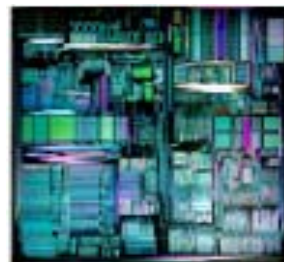
**Intel486™ DX**  
**04 / 1989**  
1.2 M  
1  $\mu\text{m}$   
25 MHz



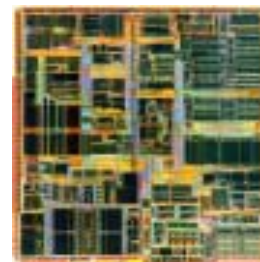
**Pentium®**  
**03 / 1993**  
3.1 M  
0.8  $\mu\text{m}$   
66 MHz



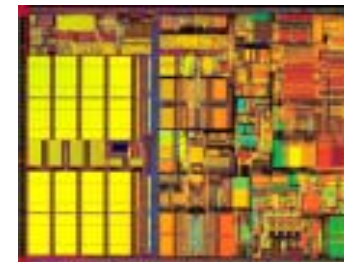
**Pentium® Pro**  
**11 / 1995**  
5.5 M  
0.6  $\mu\text{m}$   
150 MHz



**Pentium® II**  
**05 / 1997**  
7.5 M  
0.35  $\mu\text{m}$   
233 MHz



**Pentium® III**  
**02 / 1999**  
9.5 M  
0.25  $\mu\text{m}$   
500 MHz



**Pentium® 4**  
**11 / 2000**  
42 M  
0.18  $\mu\text{m}$   
1.5 GHz

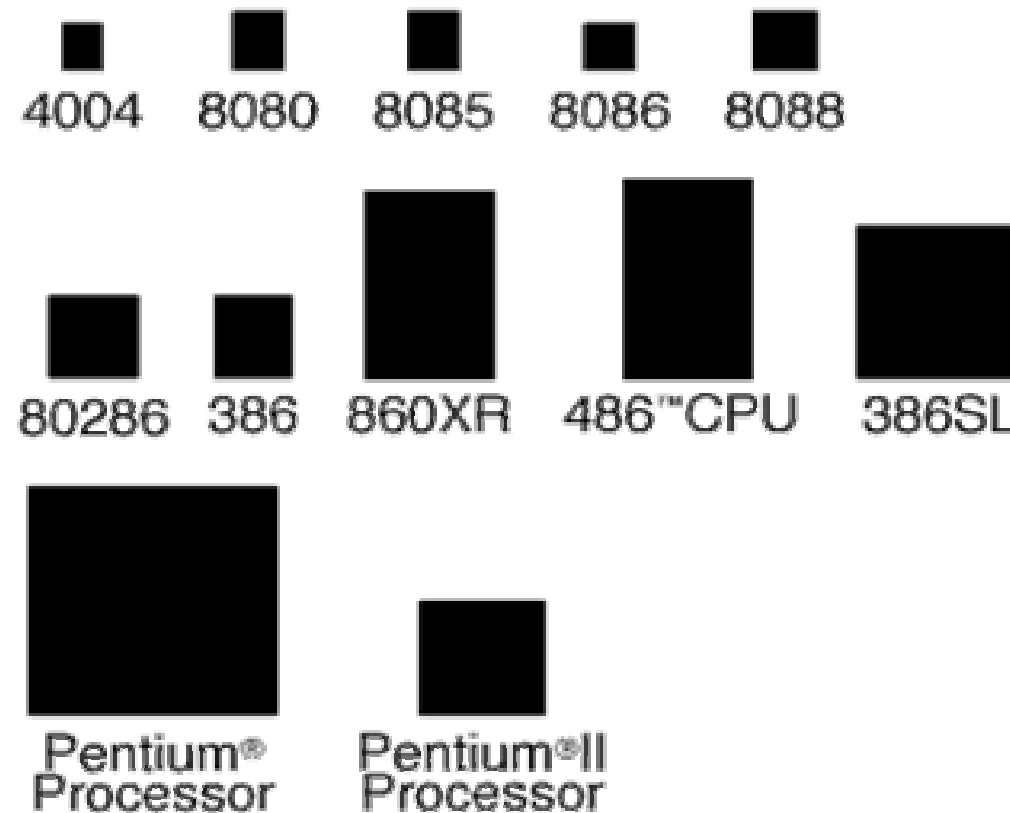


<http://www.intel.com/>



# The **intel** Microprocessors

**The correct size relationship.**



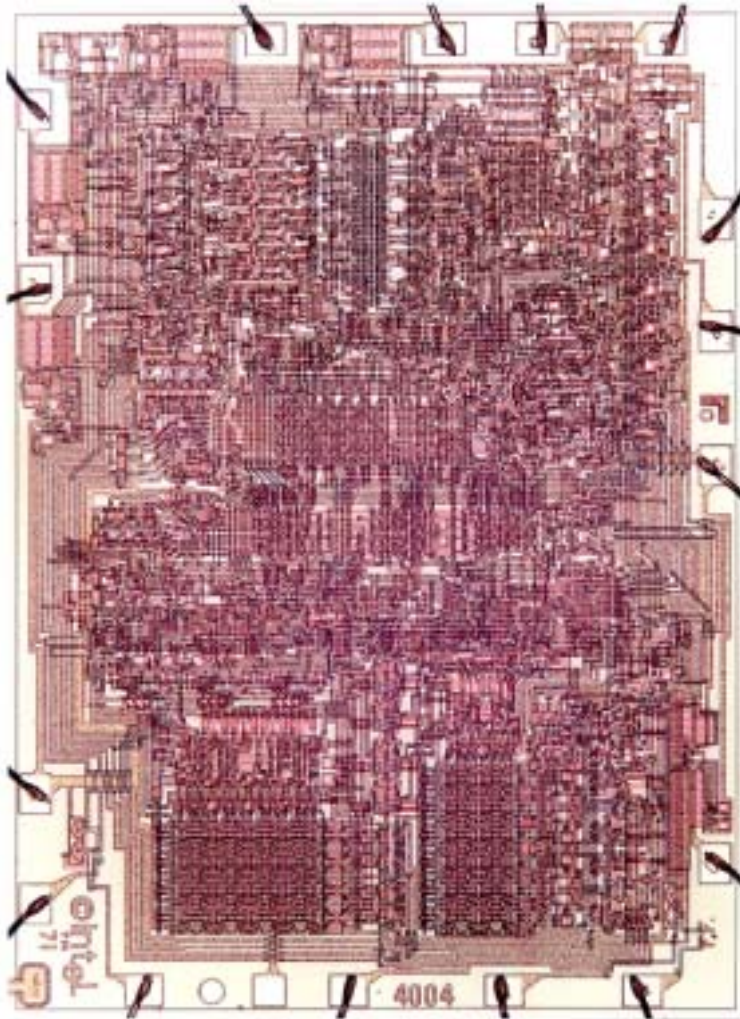
<http://www.intel.com/>





# The **intel.** 4004 processor

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<http://www.intel.com/>

- **Introduced: 15/11/1971**
- **Clock: 108 KHz**
- **2300 Transistors**
- **10  $\mu\text{m}$  technology (NMOS)**



# The Pentium® 4



<http://www.intel.com/>

## The first Pentium® 4

- Introduced: 20/11/2000
- Clock: 1.5 GHz
- 42 Million Transistors
- 0.18  $\mu\text{m}$  technology

## A more recent one

- Introduced: 23/06/2003
- Clock: 3.2 GHz
- 55 Million Transistors
- 0.13  $\mu\text{m}$  technology



# The Roadmap History

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- **The National Technology Roadmap for Semiconductors (NTRS):**  
Sponsored by the Semiconductor Industry Association (SIA)  
Edited in 1992, 1994 and 1997
- **The International Technology Roadmap for Semiconductors (ITRS):**  
Sponsored by:
  - Semiconductor Industry Association (SIA)
  - European Electronics Component Manufacturers Association (EECA)
  - Korea Semiconductor Industry Association (KSIA)
  - Japan Electronics and Information Technology Industries Association (JEITA)
  - Taiwan Semiconductor Industry Association (TSIA)Edited in 1998 (Update), 1999, 2000 (Update), 2001, 2002 (Update), 2003

**These documents always contained a 15-year outlook of the major trends of the semiconductor industry**



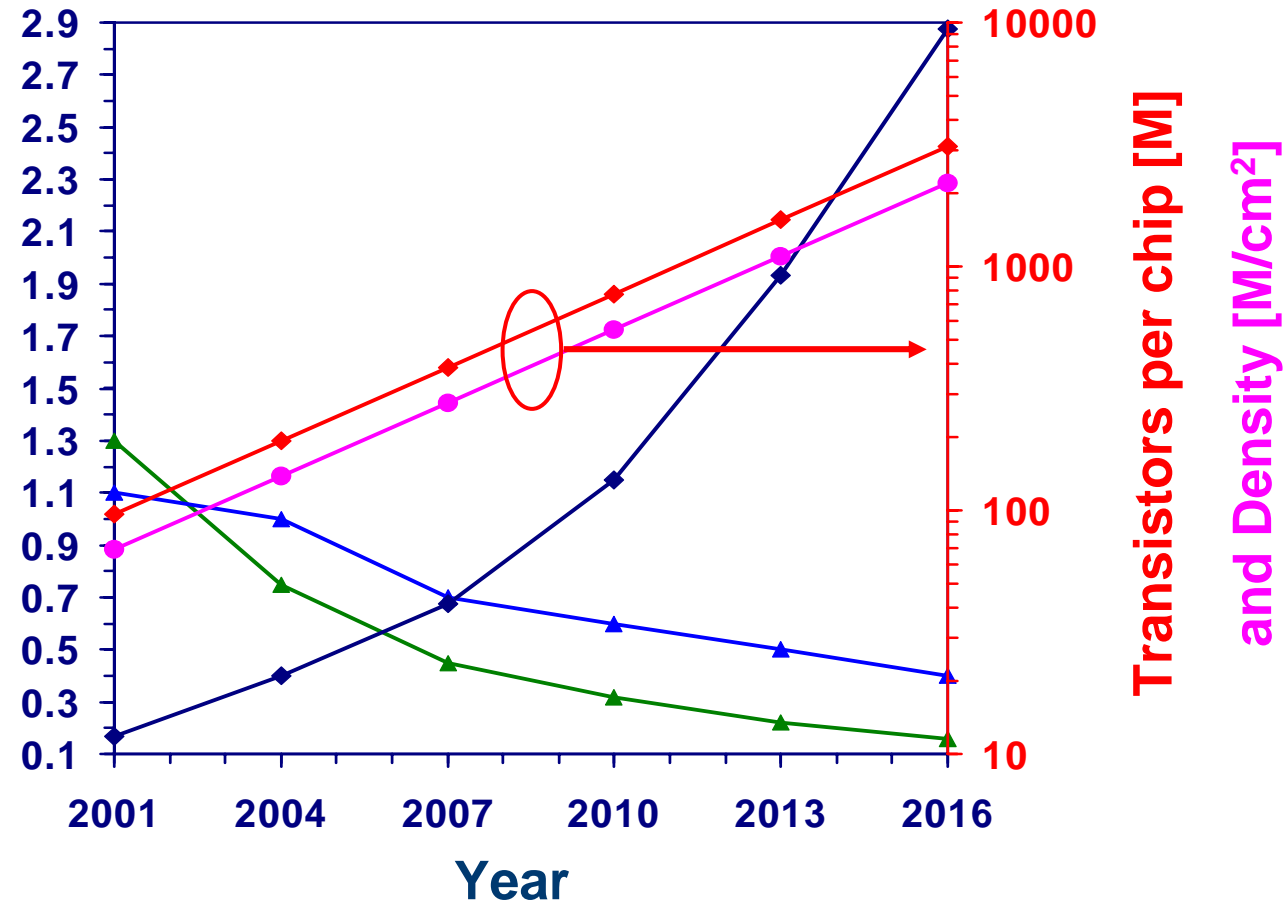


# Future perspectives

AISC Gate Length / 100 [nm]

Min. Supply Voltage [V]

On Chip Clock / 10 [GHz]

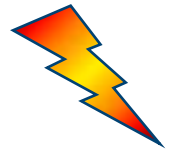


Data taken from the Executive Summary of  
The International Technology Roadmap for Semiconductors (2001 Edition)



# Outline

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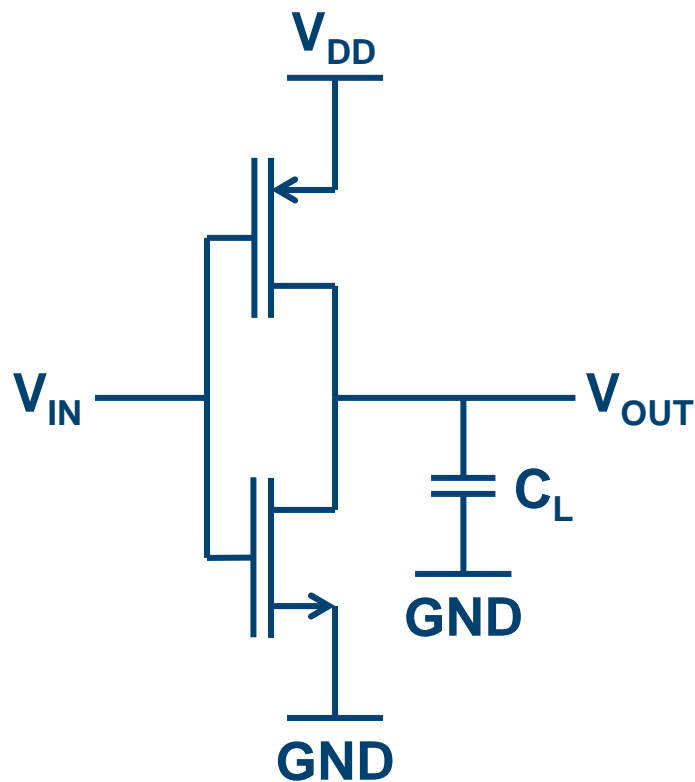
- Scaling down of CMOS technologies
- How scaling works for devices and interconnections
  - Constant field scaling
  - Generalized scaling
  - Scaling of interconnections
- Scaling impact on noise
- Scaling impact on matching
- Scaling impact on radiation tolerance
- Analog performance of submicron processes
- Substrate noise in mixed-mode integrated circuits



# Why scaling ???

**Scaling improves density, speed and power consumption of digital circuits**

**Example: CMOS inverter**



$$P_{\text{static}} = I_{\text{leakage}} \cdot V_{\text{DD}}$$

$$P_{\text{dynamic}} = C_L \cdot V_{\text{DD}}^2 \cdot f$$

$$\text{PDP} = C_L \cdot V_{\text{DD}}^2$$

Power-delay product

$t_{\text{ox}}$  ↓

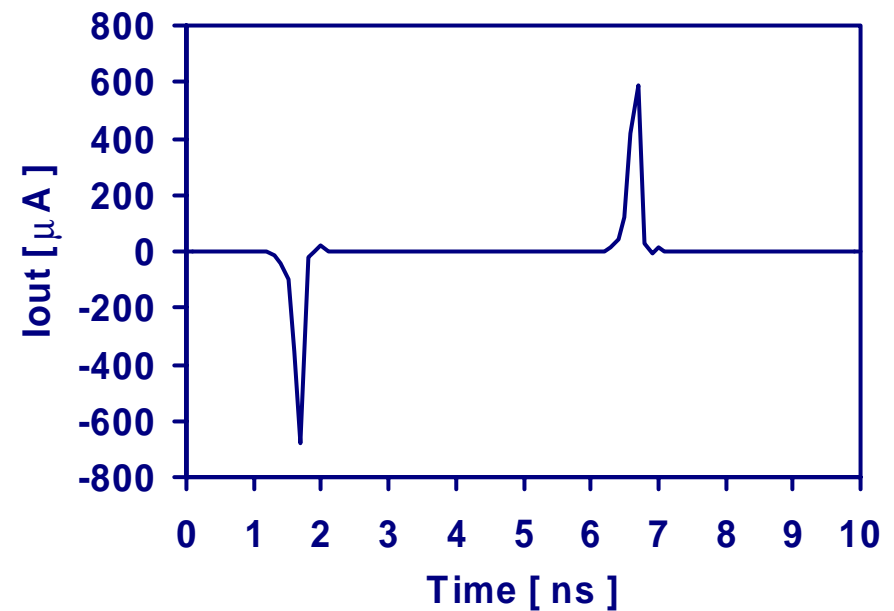
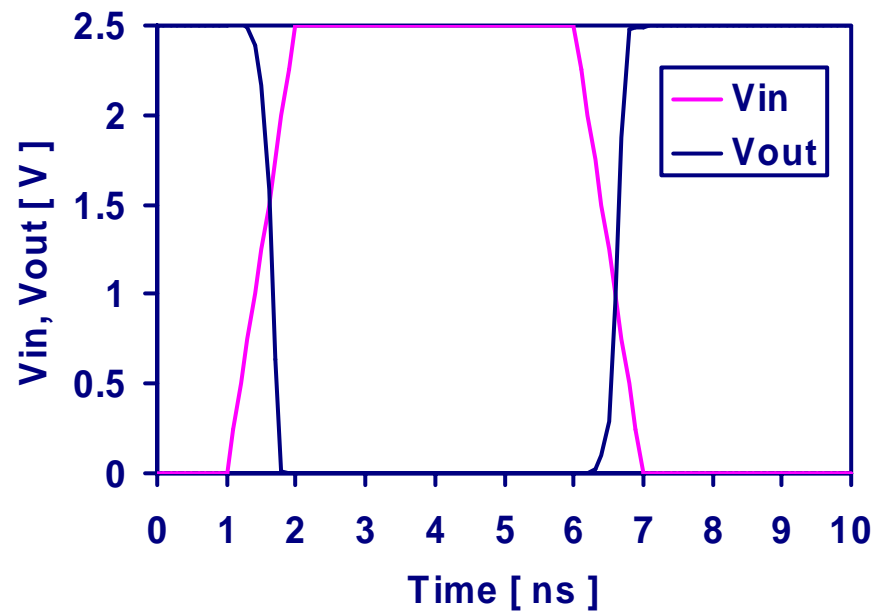
$V_{\text{DD}}$  ↓

$C_L$  ↓



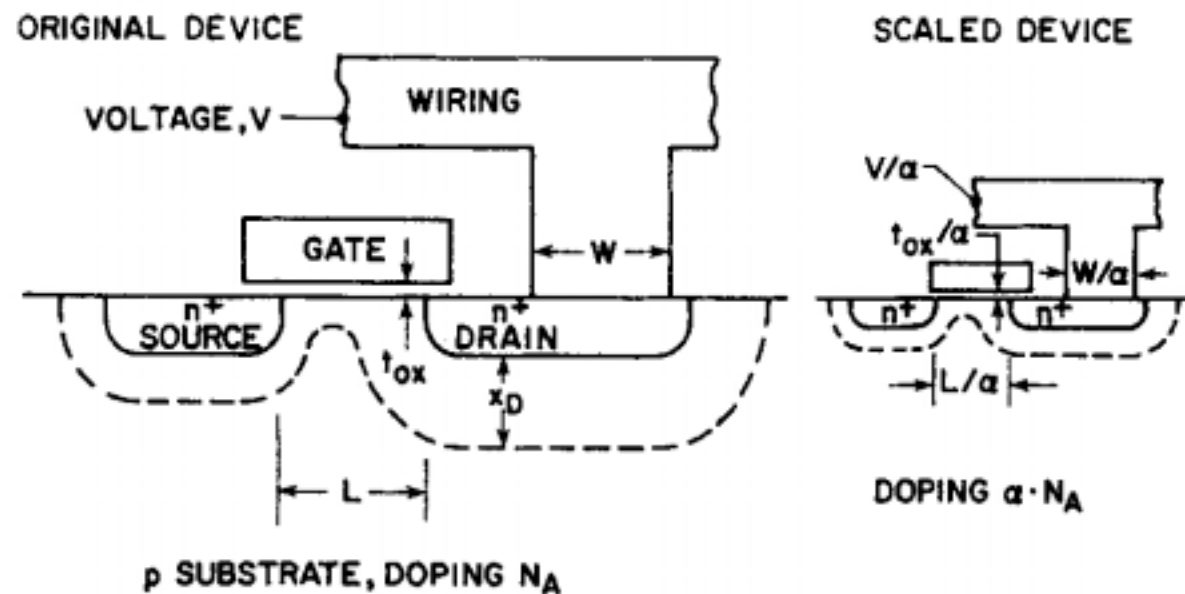
# Dynamic current in an inverter

Simulation of a chain of two inverters in a 0.25  $\mu\text{m}$  CMOS technology



# Constant field scaling

The aim of scaling is to reduce the device dimensions (to improve the circuit performance) without introducing effects which could disturb the good operation of the device.



$$x_d = \sqrt{\frac{2\epsilon_{Si}}{qN_A}} \sqrt{\phi_{bi} + V}$$





# Constant field scaling

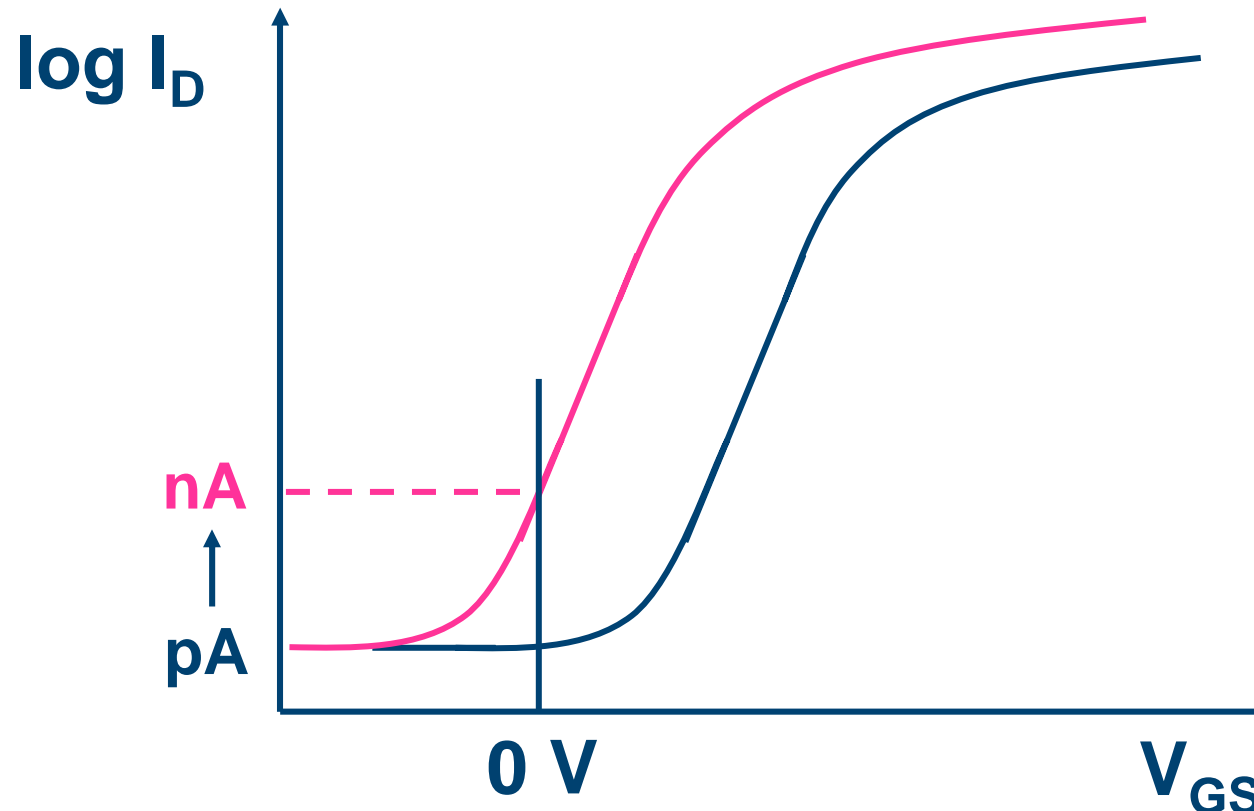
## Summary of the scaling factors for several quantities

| Quantity                                    | Scaling Factor | Quantity                             | Scaling factor    |
|---|----------------|--------------------------------------|-------------------|
| Device dimensions (L, W, $t_{ox}$ , $x_D$ ) | $1/\alpha$     | Capacitances                         | $1/\alpha$        |
| Area  | $1/\alpha^2$   | Capacitances per unit area           | $\alpha$          |
| Devices per unit of chip area (density)     | $\alpha^2$     | Charges                              | $1/\alpha^2$      |
| Doping concentration ( $N_A$ )              | $\alpha$       | Charges per unit area                | 1                 |
| Bias voltages and $V_T$                     | $1/\alpha$     | Electric field intensity             | 1                 |
| Bias currents                               | $1/\alpha$     | Body effect coefficient ( $\gamma$ ) | $1/\sqrt{\alpha}$ |
| Power dissipation for a given circuit       | $1/\alpha^2$   | Transistor transit time ( $\tau$ )   | $1/\alpha$        |
| Power dissipation per unit of chip area     | 1              | Transistor power-delay product       | $1/\alpha^3$      |

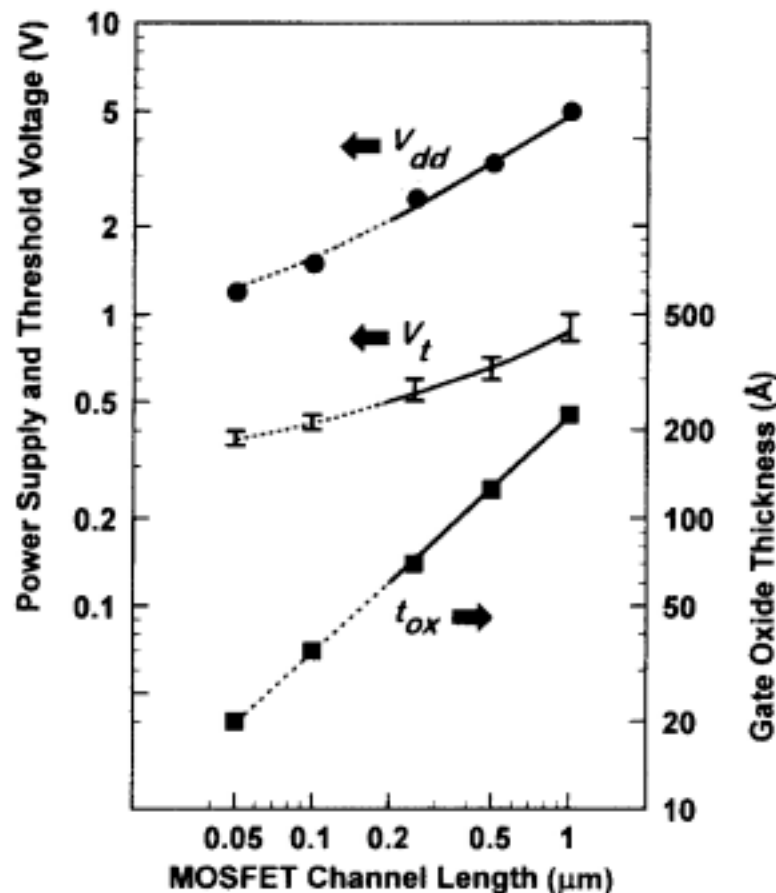


# Constant field scaling problem

**Subthreshold slope and width of the moderate inversion region do not scale. This can have a devastating impact on the static power consumption of a digital circuit.**



# Generalized scaling



- The dimensions in the device scale as in the *constant field* scaling
- $V_{dd}$  scales to have reasonable electric fields in the device, but slower than  $t_{ox}$ , to have an useful voltage swing for the signals
- The doping levels are adjusted to have the correct depletion region widths
- To limit the subthreshold currents,  $V_T$  scales more slowly than  $V_{dd}$

Y. Taur et al., "CMOS Scaling into the Nanometer Regime", *Proc. of the IEEE*, vol. 85, no. 4, Apr. 1997, pp. 486-504.

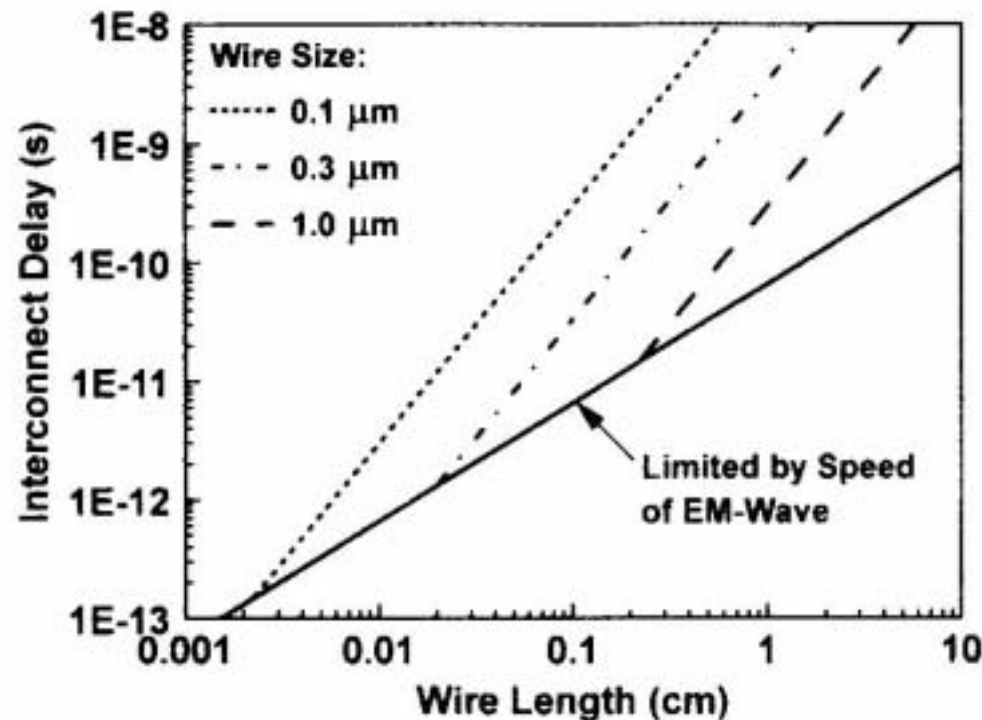
Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998, p. 186.



# Scaling of interconnections

An accurate scaling of the interconnections is needed as well, so that we can profit at the circuit level of the improvements made at the device level.

Interconnections are becoming more and more important in modern technologies because the delay they introduce is becoming comparable with the switching time of the digital circuits.

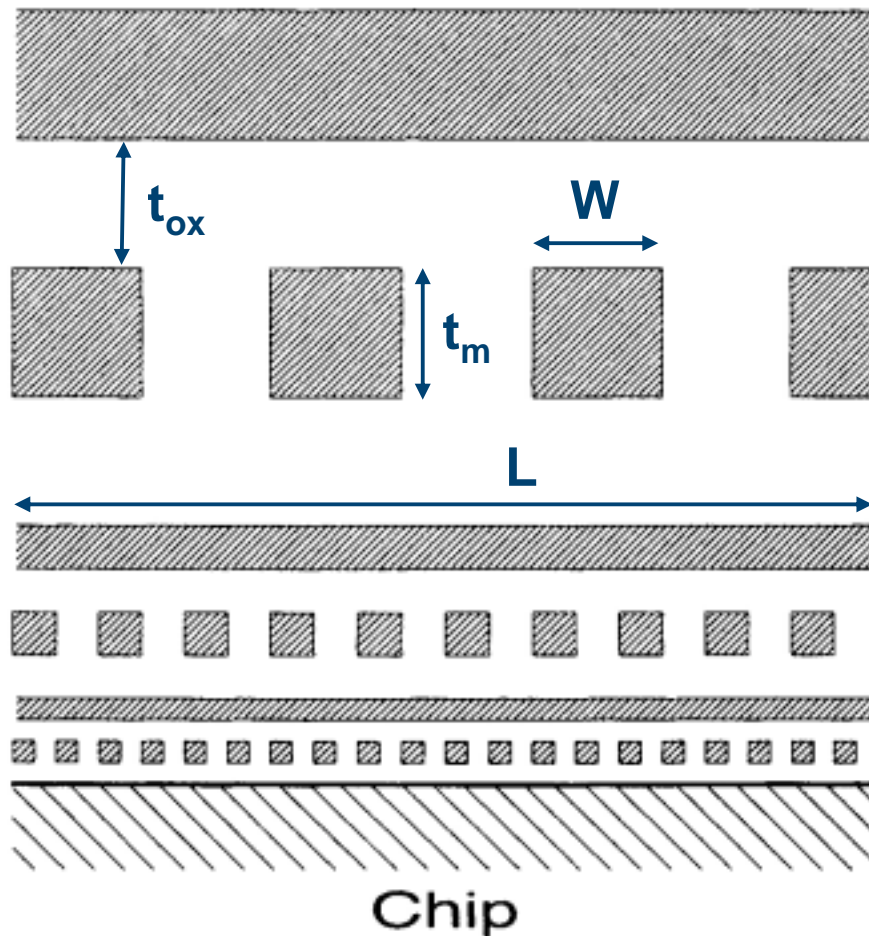


Y. Taur et al., "CMOS Scaling into the Nanometer Regime", *Proceedings of the IEEE*, vol. 85, no. 4, Apr. 1997, pp. 486-504.

T. N. Theis, "The future of interconnection technology", *IBM Journal of Research and Development*, vol. 44, no. 3, May 2000, pp. 379-390.

# “Reverse” scaling

The scaling method is different from the one applied to devices



If  $W$ ,  $L$ ,  $t_m$  and  $t_{ox}$  are scaled by  $1/\alpha$

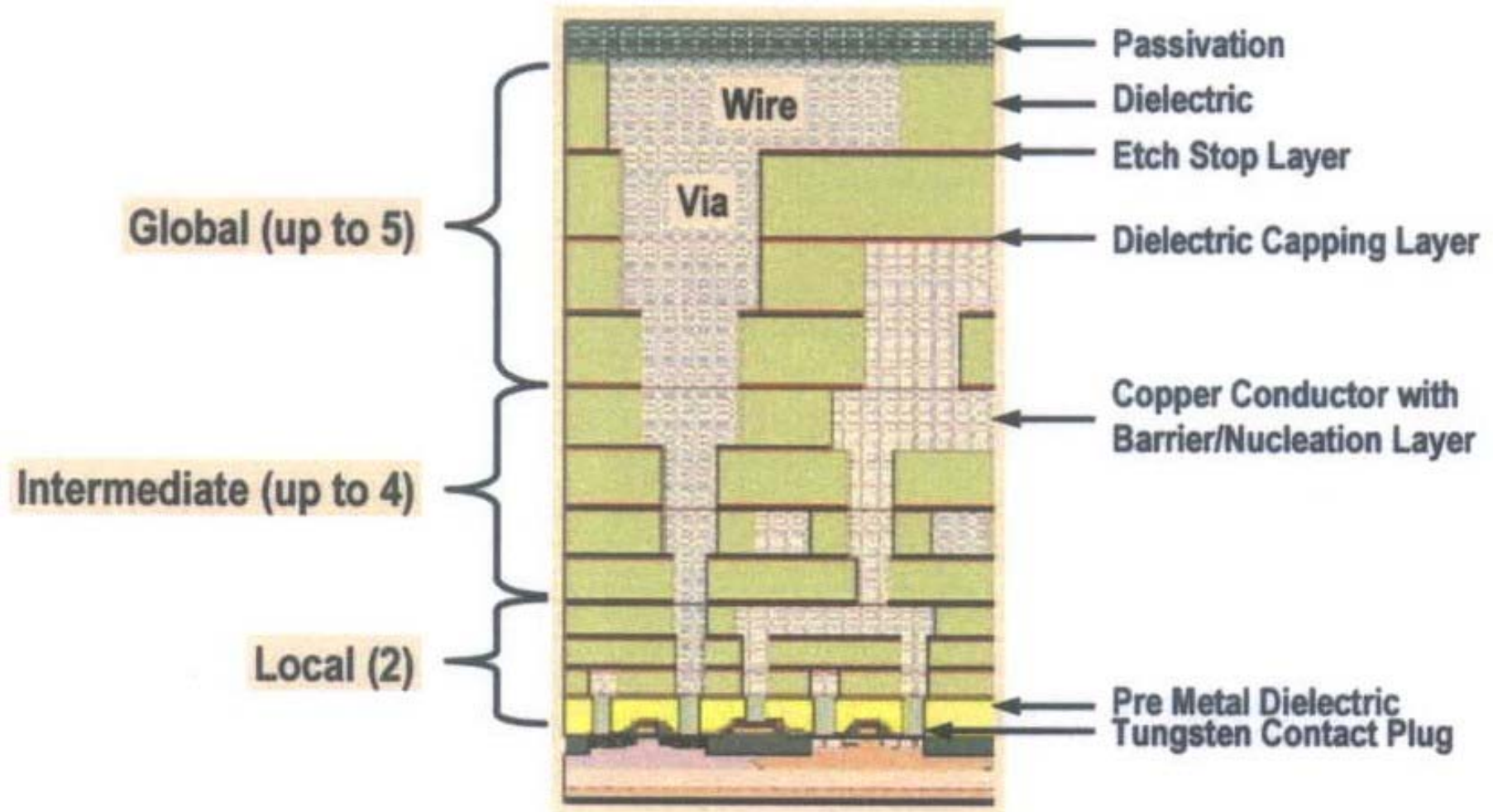


- Current density scales by  $\alpha$
- $R$  scales by  $\alpha$ ,  $C$  scales by  $1/\alpha$
- RC (delay) does not scale!!!

**In practice, wires dimensions are reduced only for local interconnections (but not  $t_m$ ). At the chip scale,  $t_m$  and  $t_{ox}$  are increased (reverse scaling).**



# Hierarchical scaling



*Figure 36 Cross-section of Hierarchical Scaling*



# Generalized selective scaling

| Physical parameter                  | Constant-Electric Field Scaling Factor | Generalized Scaling Factor | Generalized Selective Scaling Factor |
|-------------------------------------|--|----------------------------|--------------------------------------|
| Channel length, Insulator thickness | $1/\alpha$                             | $1/\alpha$                 | $1/\alpha_d$                         |
| Wiring width, channel width         | $1/\alpha$                             | $1/\alpha$                 | $1/\alpha_w$                         |
| Electric field in device            | 1                                      | $\varepsilon$              | $\varepsilon$                        |
| Voltage                             | $1/\alpha$                             | $\varepsilon/\alpha$       | $\varepsilon/\alpha_d$               |
| On-current per device               | $1/\alpha$                             | $\varepsilon/\alpha$       | $\varepsilon/\alpha_w$               |
| Doping                              | $\alpha$                               | $\varepsilon\alpha$        | $\varepsilon\alpha_d$                |
| Area                                | $1/\alpha^2$                           | $1/\alpha^2$               | $1/\alpha_w^2$                       |
| Capacitance                         | $1/\alpha$                             | $1/\alpha$                 | $1/\alpha_w$                         |
| Gate delay                          | $1/\alpha$                             | $1/\alpha$                 | $1/\alpha_d$                         |
| Power dissipation                   | $1/\alpha^2$                           | $\varepsilon^2/\alpha^2$   | $\varepsilon^2/\alpha_w\alpha_d$     |
| Power density                       | 1                                      | $\varepsilon^2$            | $\varepsilon^2\alpha_w/\alpha_d$     |

$\alpha$  is the dimensional scaling parameter,  $\varepsilon$  is the electric field scaling parameter, and  $\alpha_D$  and  $\alpha_W$  are separate dimensional scaling parameters for the selective scaling case.  $\alpha_D$  is applied to the device vertical dimensions and gate length, while  $\alpha_W$  applies to the device width and the wiring.

D. J. Frank et al., "Device Scaling Limits of Si MOSFETs and Their Application Dependencies", *Proc. IEEE*, vol. 89, no. 3, March 2001, pp. 259-288.



# Outline

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- Scaling down of CMOS technologies
- How scaling works for devices and interconnections
- **Scaling impact on noise**
- Scaling impact on matching
- Scaling impact on radiation tolerance
- Analog performance of submicron processes
- Substrate noise in mixed-mode integrated circuits



# Scaling impact on noise

$$\frac{\overline{v_{in}^2}}{\Delta f} = 4kTn\gamma \frac{1}{g_m} + \frac{K_a}{C_{ox}^2 WL} \frac{1}{f^\alpha}$$
$$g_m = \sqrt{\frac{2}{n}} \mu C_{ox} \frac{W}{L} I_{DS} \quad C_{ox} = \frac{\epsilon_{SiO_2}}{t_{ox}}$$

$t_{ox} \downarrow \quad C_{ox} \uparrow \quad g_m \uparrow$

**White noise:** keeping the same W/L ratio and the same current, we have an improvement in the noise since  $C_{ox}$  (and therefore  $g_m$ ) increases with scaling.

**1/f noise:** we suppose that the constant  $K_a$  does not change with scaling. In this case, we have an improvement in the noise if we keep the same device area (WL), or we have the same noise if we scale both W and L. Data taken from the Roadmap foresee that  $K_a$  will remain more or less constant even for the most advanced CMOS processes. This must, of course, be verified...



# Scaling impact on noise

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**For the same device dimensions and current, both the channel thermal noise and the flicker ( $1/f$ ) noise should decrease**

**BUT**

**there can be other effects in submicron MOSFETs that tend to increase the noise, such as, for example, carriers heating and parasitic resistances.**

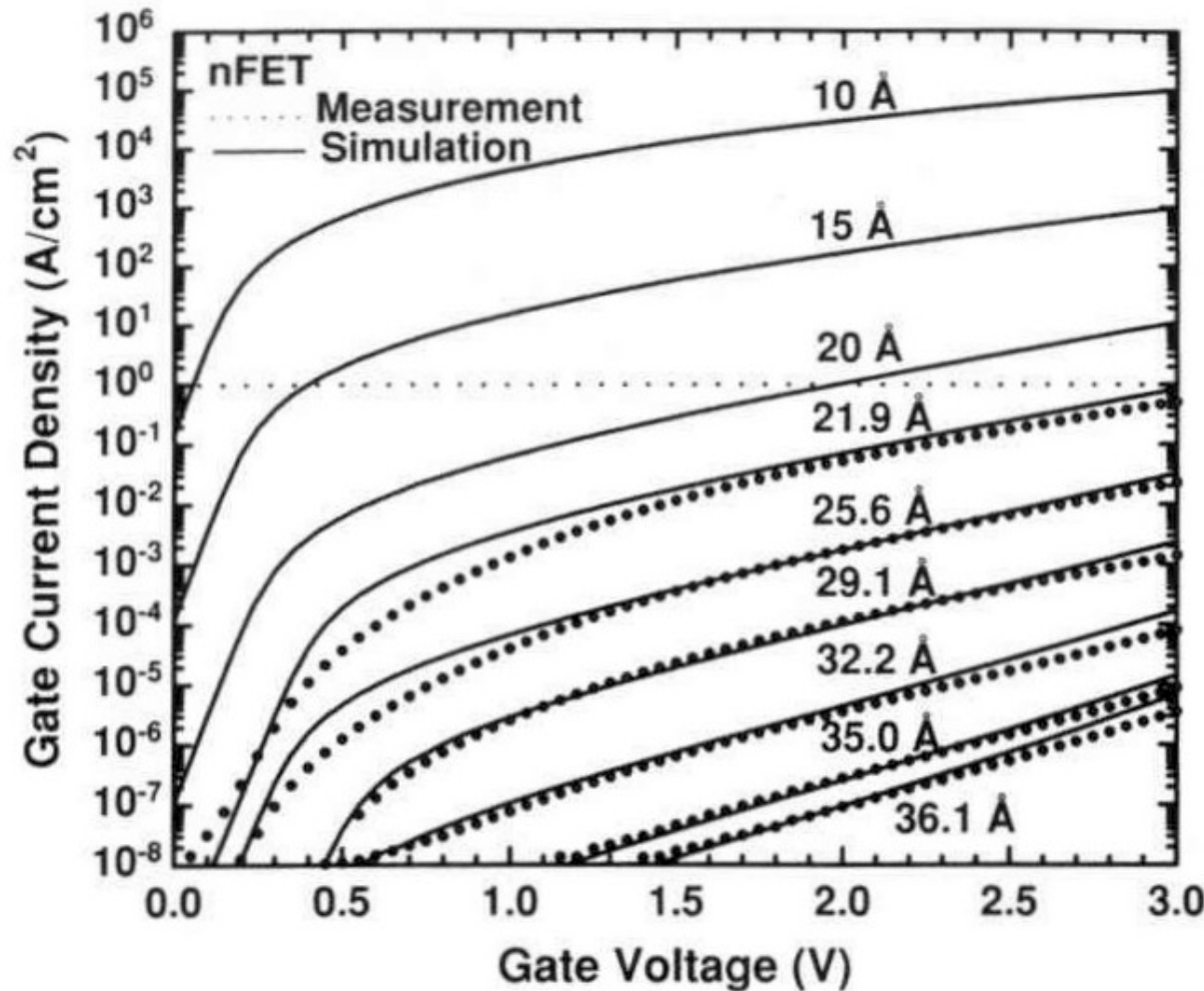
**The constant  $K_a$  is HIGHLY technology dependent. It might be difficult to keep it under control in new advanced processes. Moreover, the effect on  $1/f$  noise on new dielectric materials is not yet known.**

**Another (possibly serious) source of problems in the future will be the leakage current through the gate oxide. Thinner gate oxides will have a much higher leakage current, which will have a higher shot noise.**





# Gate leakage current shot noise



$$\sqrt{\frac{i_n^2}{\Delta f}} = 2qI$$

In the hypothesis:

- current density = 1 A/cm<sup>2</sup>
- W = 1000 μm
- L = 0.1 μm

We have

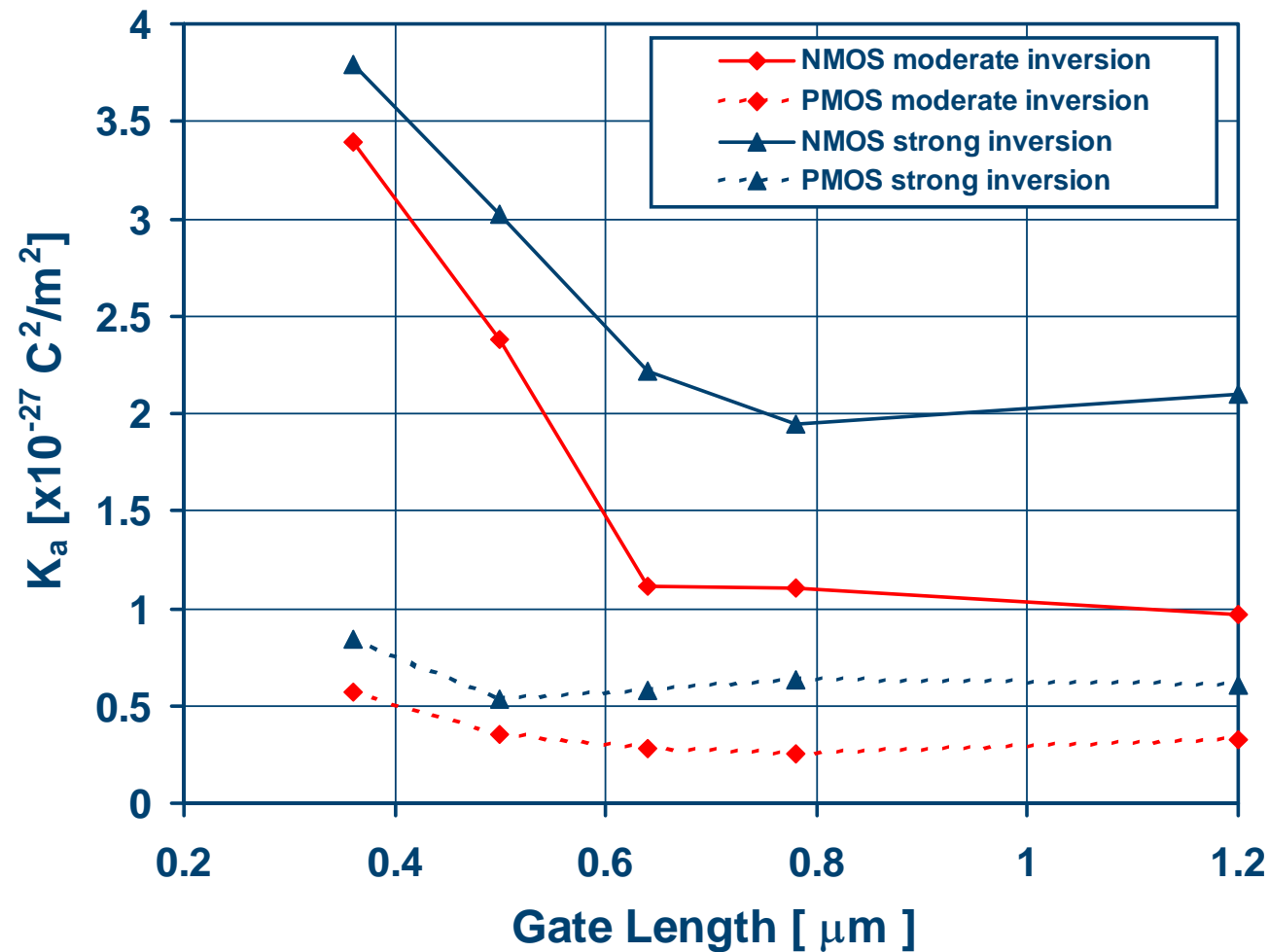
- I = 1 μA
- 2qI = 0.56 pA/√Hz

which are NOT negligible values!



# 1/f Noise parameter $K_a$

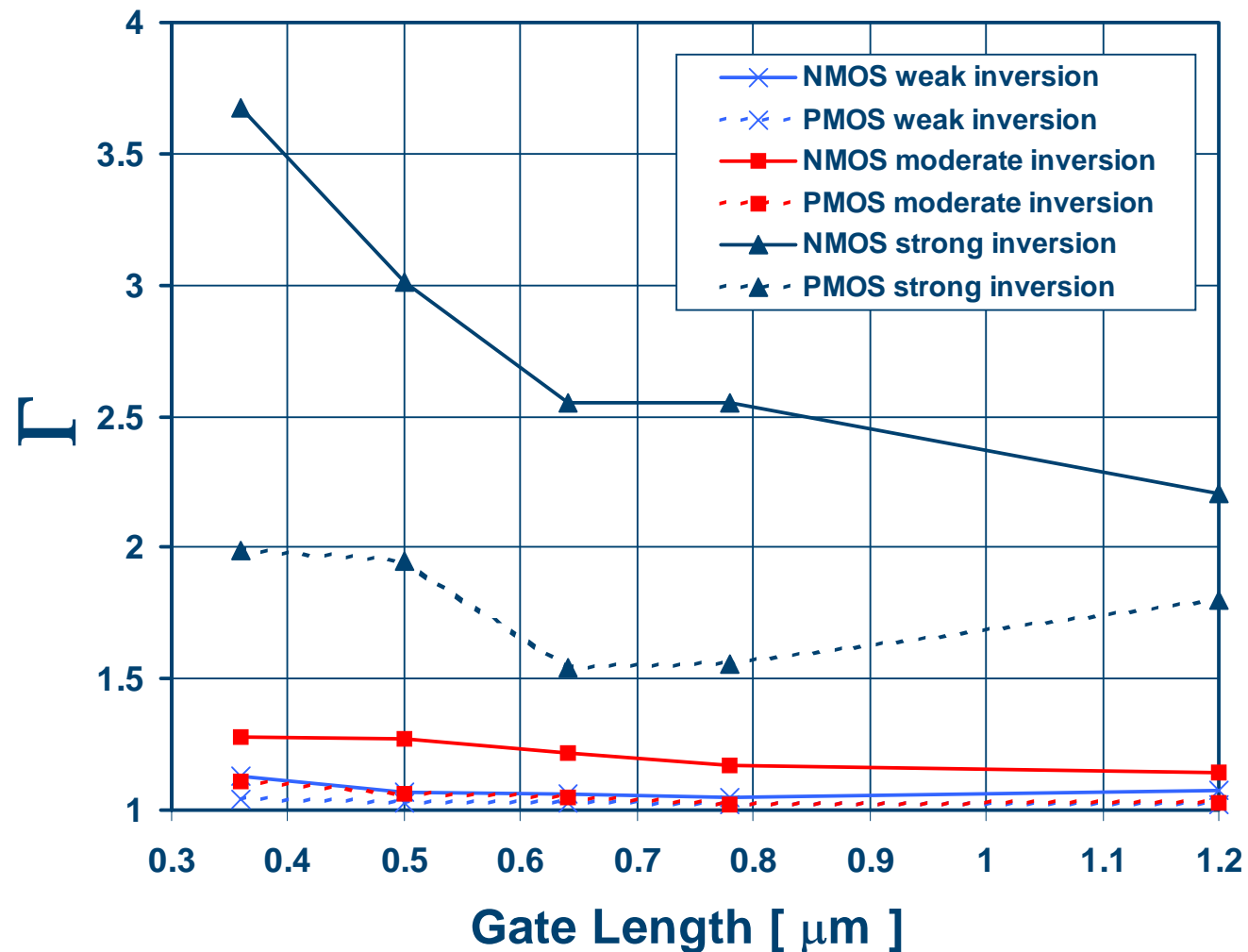
## 0.25 $\mu\text{m}$ CMOS technology





# Excess noise factor $\Gamma$

## 0.25 $\mu\text{m}$ CMOS technology





# Outline

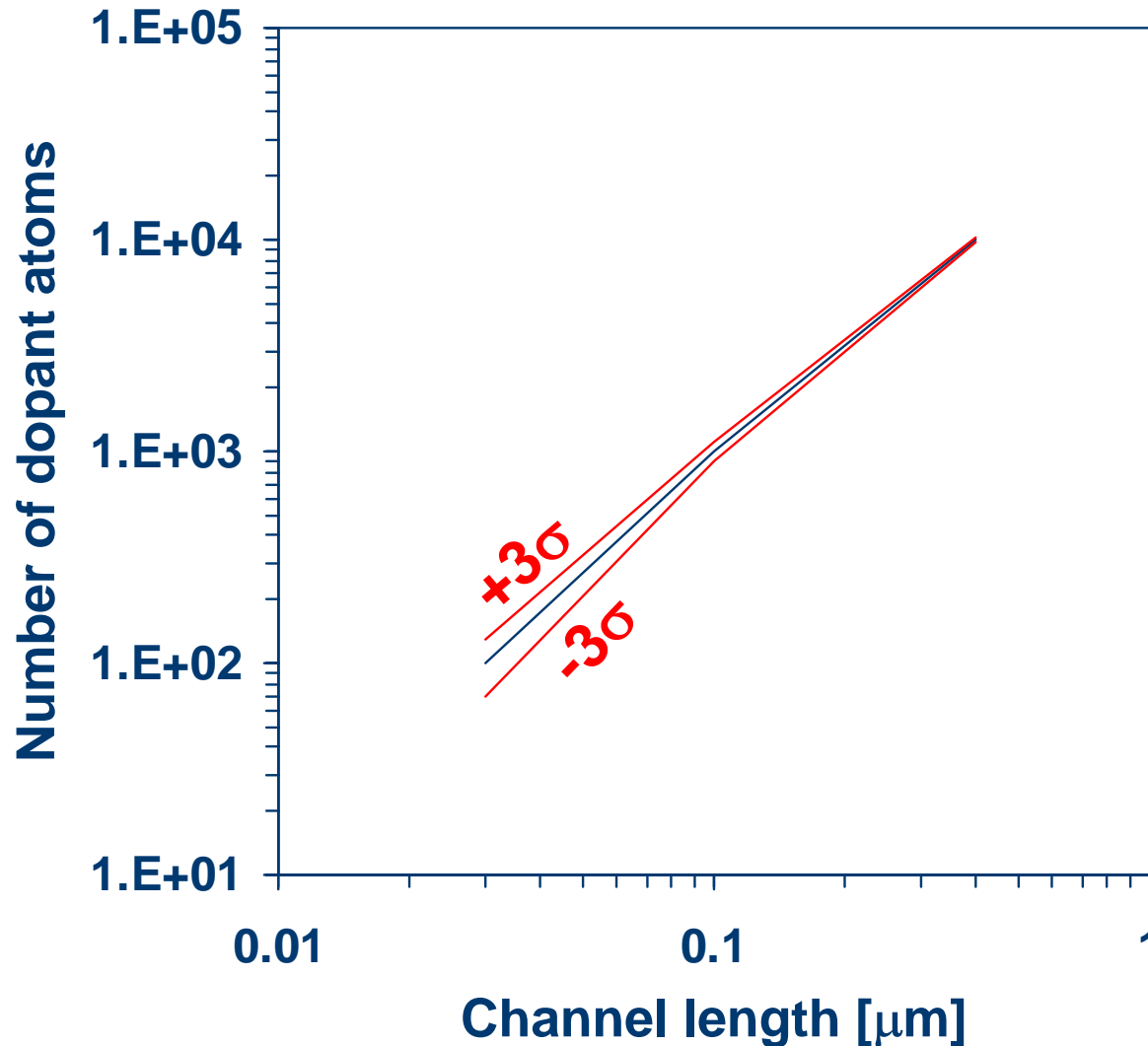
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- Scaling down of CMOS technologies
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- **Scaling impact on matching**
- Scaling impact on radiation tolerance
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# Channel dopant fluctuation



The ion implantation process follows Poisson statistics. Therefore, the uncertainty in the number of dopant implanted is given by the square root of the number.

**The error becomes proportionally more important for smaller devices! ( $=1/\sqrt{N}$ )**





# Scaling & dopant fluctuations

$$\sigma_{\Delta V_{th}} = C \cdot \frac{t_{ox} \cdot \sqrt[4]{N}}{\sqrt{W L}}$$

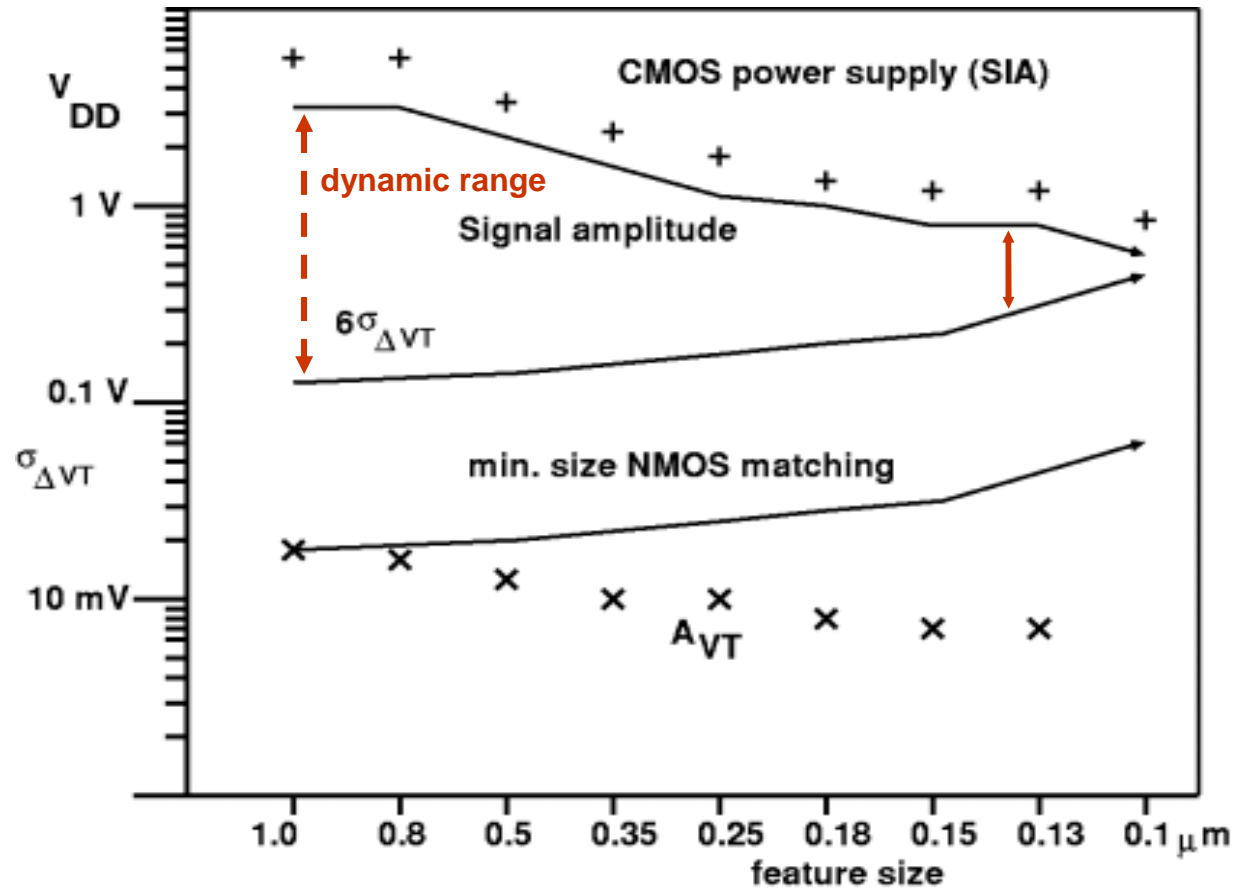
- For the same device dimensions, matching improves
- For minimum size devices, matching might be worse

| $L_{min}$<br>[ $\mu m$ ] | $t_{ox}$<br>[nm] | $N_a$ [ $cm^{-3}$ ] | $A_N / t_{ox}$<br>[mV· $\mu m$ / nm] | $A_N$<br>[mV· $\mu m$ ] | $\sigma_{\Delta V_{th}}$<br>[mV] | $6 \cdot \sigma_{V_{th}}$<br>[mV] |
|--------------------------|------------------|---------------------|--------------------------------------|-------------------------|----------------------------------|-----------------------------------|
| 1.2                      | 25               | $5 \cdot 10^{16}$   | 0.328                                | 8.2                     | 6.84                             | 29                                |
| 1                        | 20               | $6 \cdot 10^{16}$   | 0.344                                | 6.9                     | 6.89                             | 29.2                              |
| 0.8                      | 15               | $7.5 \cdot 10^{16}$ | 0.365                                | 5.5                     | 6.84                             | 29                                |
| 0.5                      | 10               | $1.2 \cdot 10^{17}$ | 0.414                                | 4.1                     | 8.28                             | 35.1                              |
| 0.25                     | 5.5              | $2.4 \cdot 10^{17}$ | 0.498                                | 2.7                     | 11                               | 46.5                              |
| 0.18                     | 4                | $3.3 \cdot 10^{17}$ | 0.542                                | 2.2                     | 12                               | 51.1                              |

P.A. Stolk et al., "Modeling Statistical Dopant Fluctuations in MOS Transistors", *IEEE Trans. Elect. Dev.*, vol. 45, no. 9, Sept. 1998 , pp. 1960-1971.



# Scaling impact on matching



**Matching will have a very important impact on the performance of deep submicron CMOS circuits**

M.J.M. Pelgrom et al., "Transistor matching in analog CMOS applications", *Technical Digest of the International Devices Meeting 1998*, pp. 915-918.

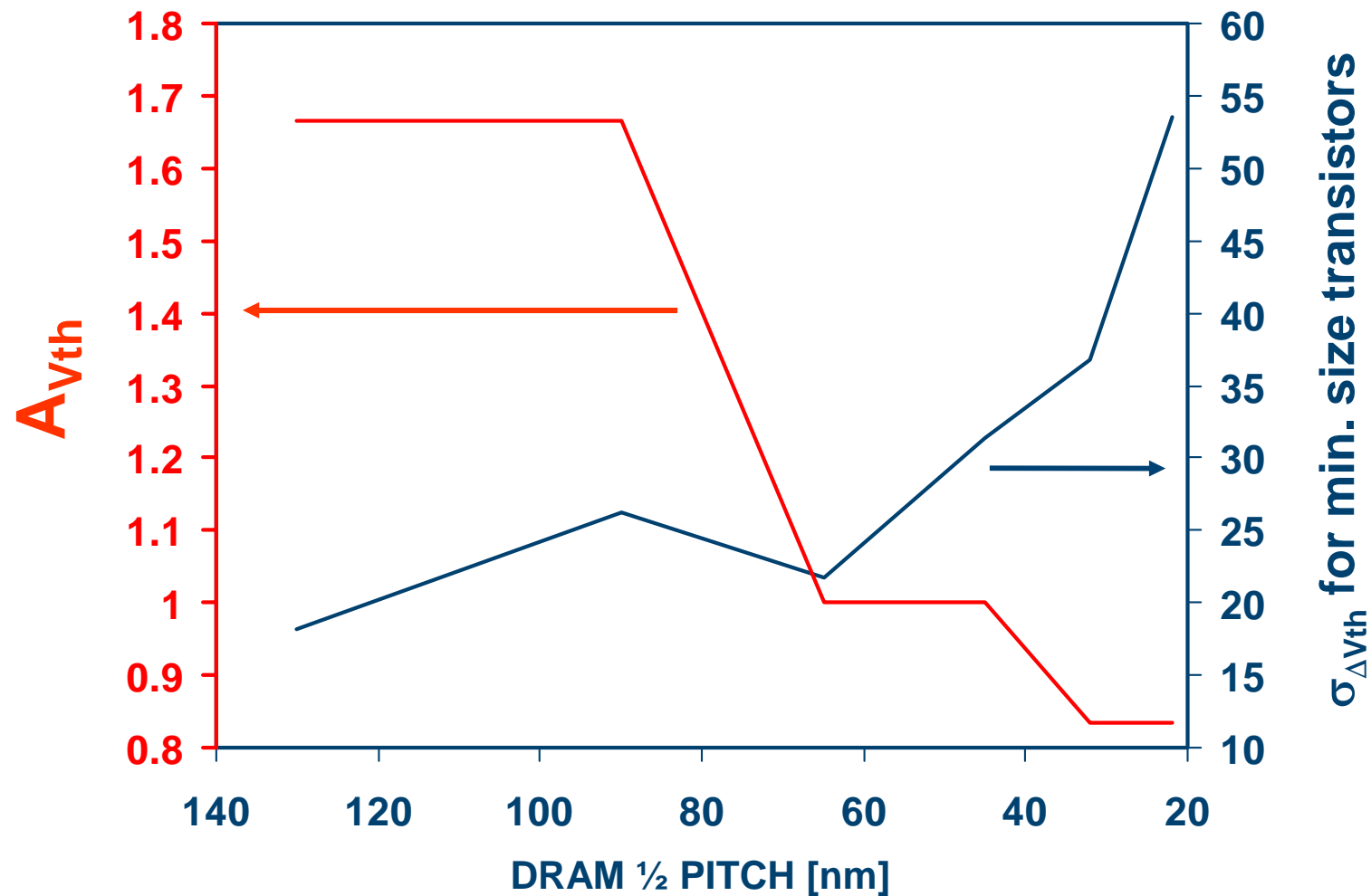
Kumasi, December 2003

Giovanni Anelli, CERN

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# Matching data from the Roadmap



Data taken from The International Technology Roadmap for Semiconductors (2001 Edition)



# Outline

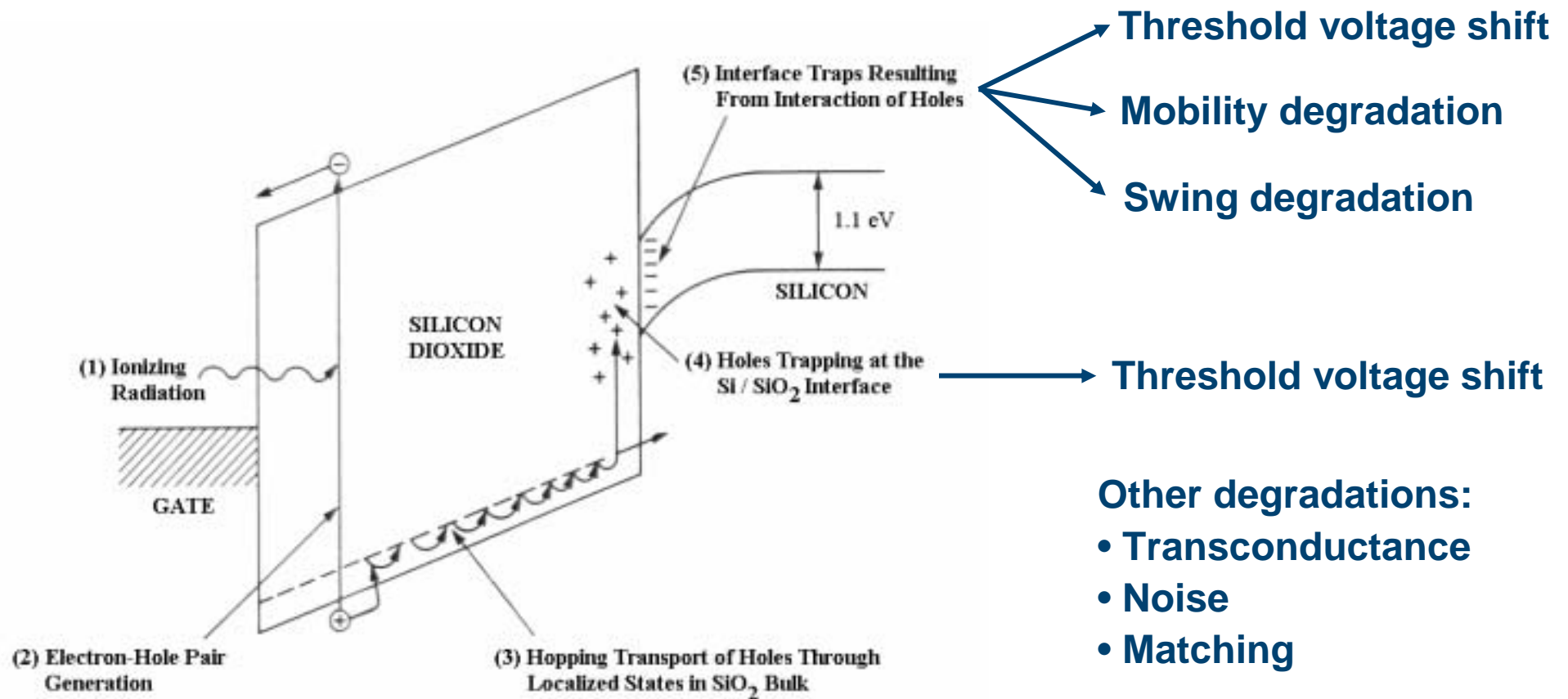
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- Scaling down of CMOS technologies
- How scaling works for devices and interconnections
- Scaling impact on noise
- Scaling impact on matching
- **Scaling impact on radiation tolerance**
  - Radiation effects in MOS transistors
  - Scaling impact on the radiation tolerance
  - Enclosed Layout Transistor
- Analog performance of submicron processes
- Substrate noise in mixed-mode integrated circuits





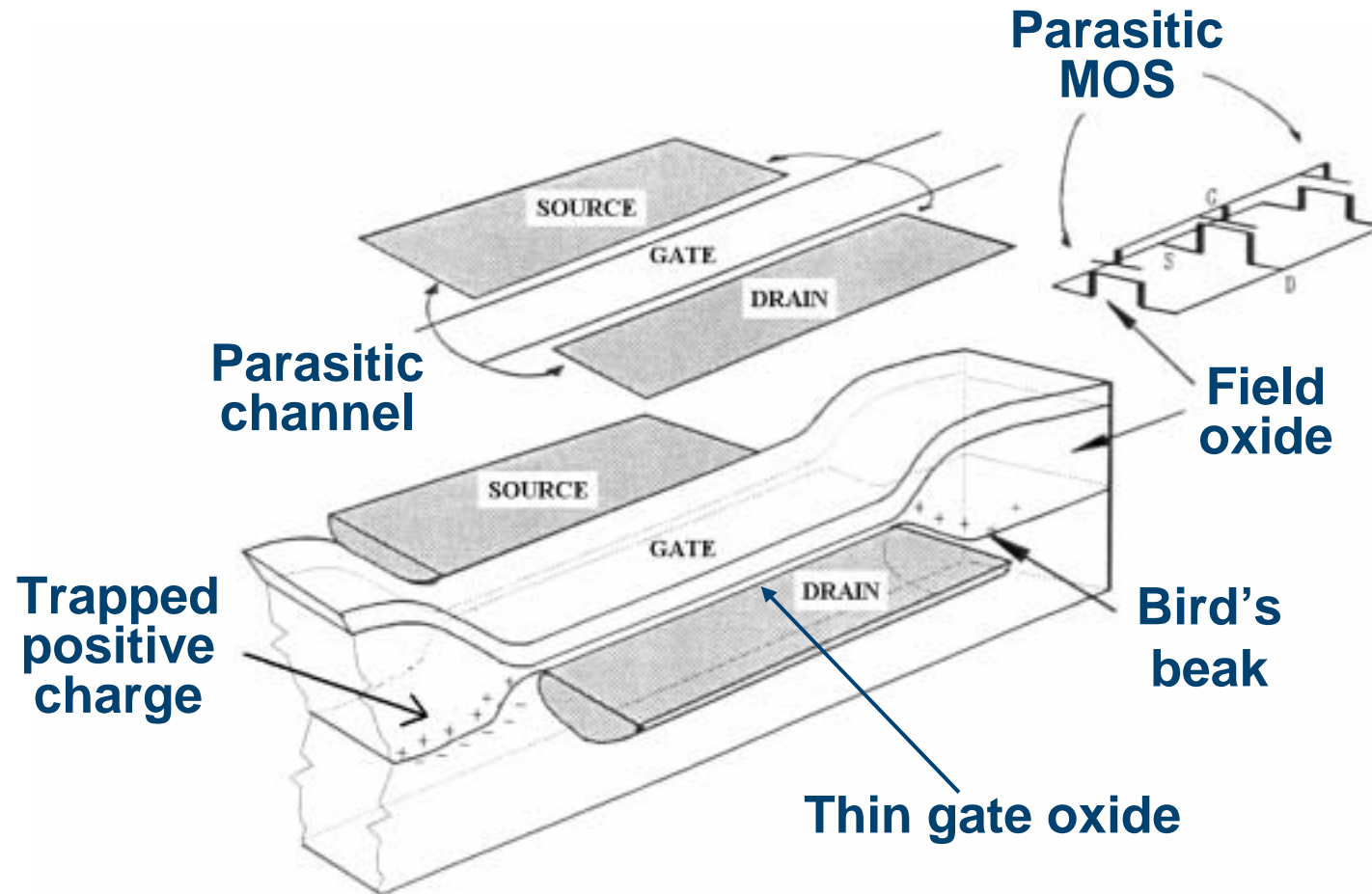
# Ionizing particles through a MOST



F. B. McLean and T. R. Oldham, Harry Diamond Laboratories Technical Report, No. HDL-TR-2129, September 1987.



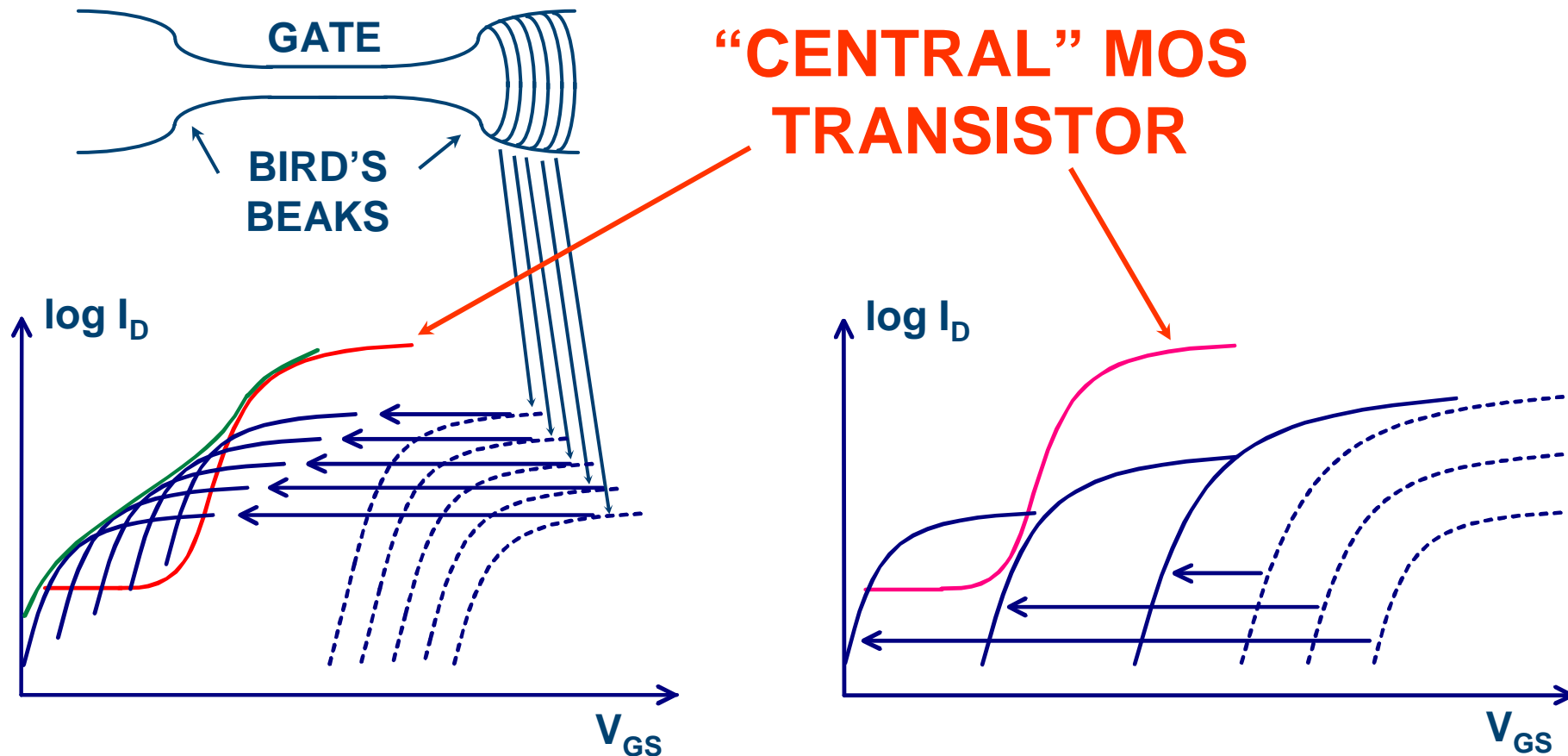
# Transistor level leakage (NMOS)



R. Gaillard, J.-L. Leray, O. Musseau et al., "Techniques de durcissement des composants, circuits, et systèmes électroniques", Notes of the Short Course of the 3<sup>rd</sup> European Conference on Radiation and its Effects on Components and Systems, Arcachon (France), Sept. 1995.



# Transistor level leakage



**This is for LOCOS, what about STI? Things do not improve!**

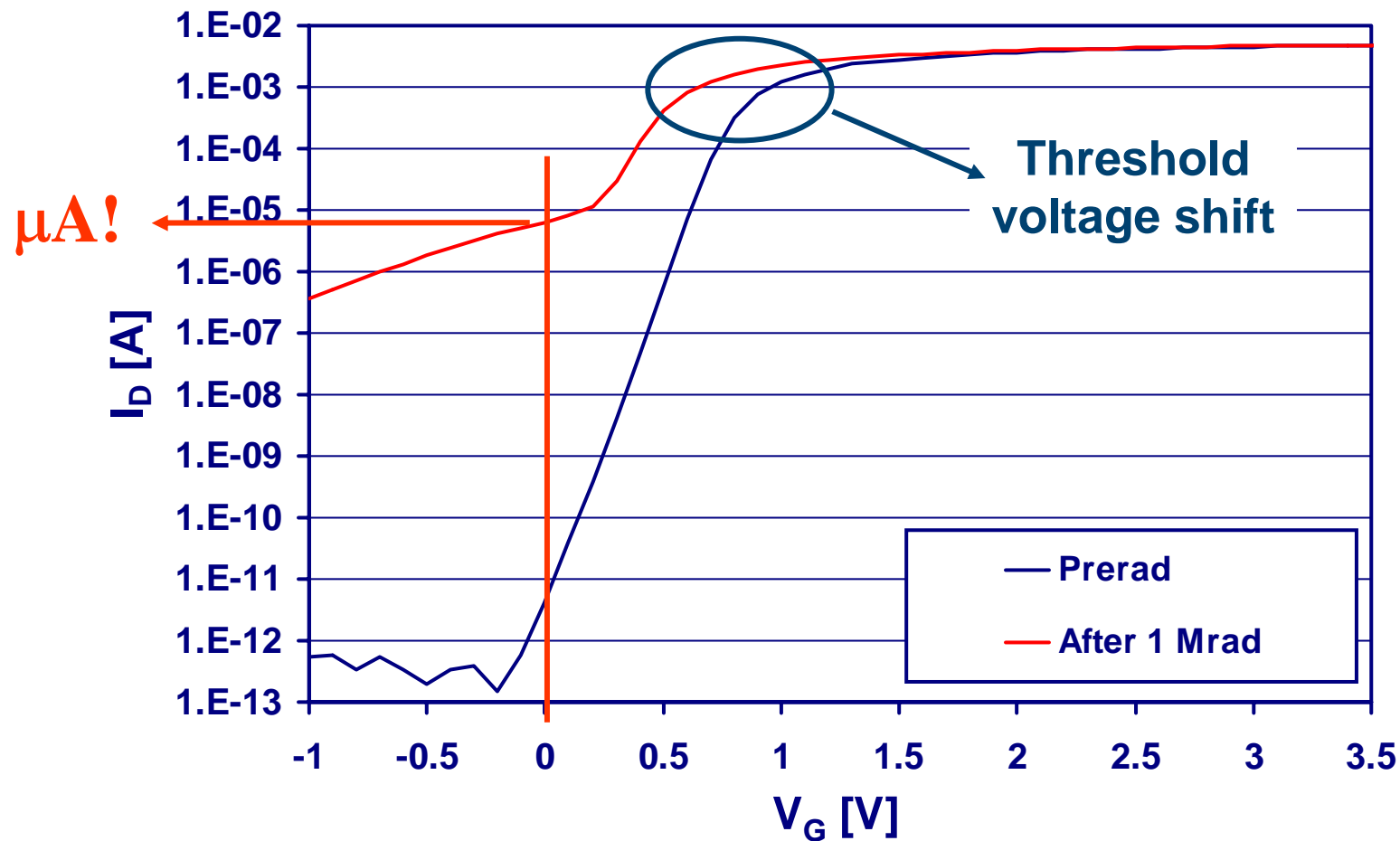
M. R. Shaneyfelt et al., "Challenges in Hardening Technologies Using Shallow-Trench Isolation", *IEEE TNS*, vol. 45, Dec. 1998, pp. 2584-2592.





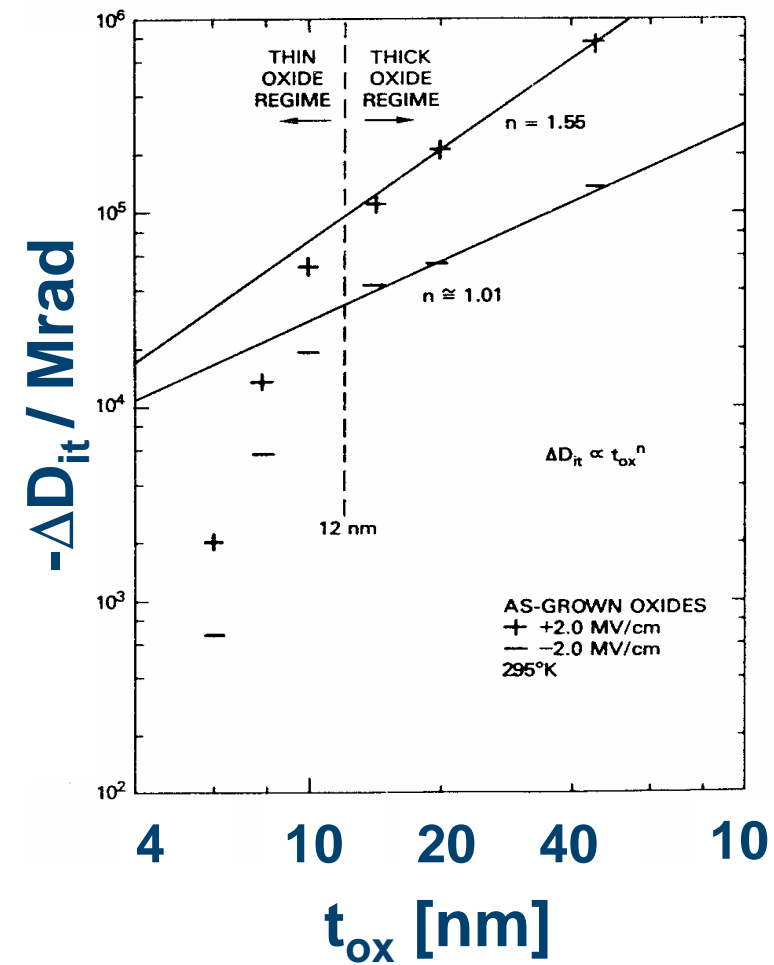
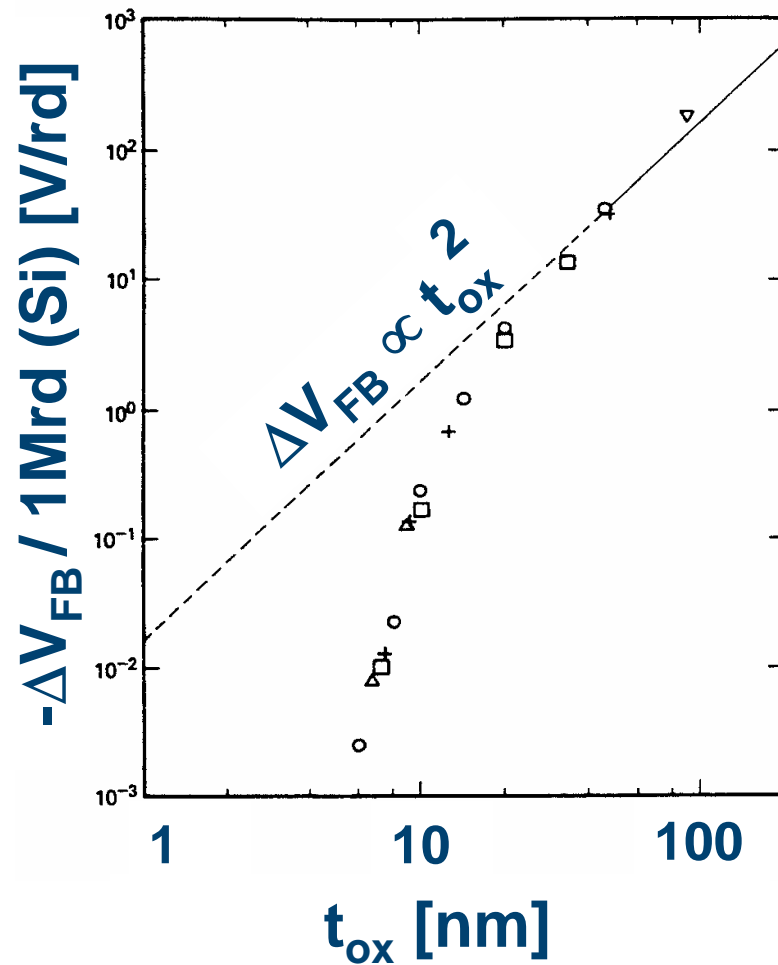
# Transistor level leakage: example

NMOS - 0.7  $\mu\text{m}$  technology -  $t_{\text{ox}} = 17 \text{ nm}$





# Total Dose damage and scaling

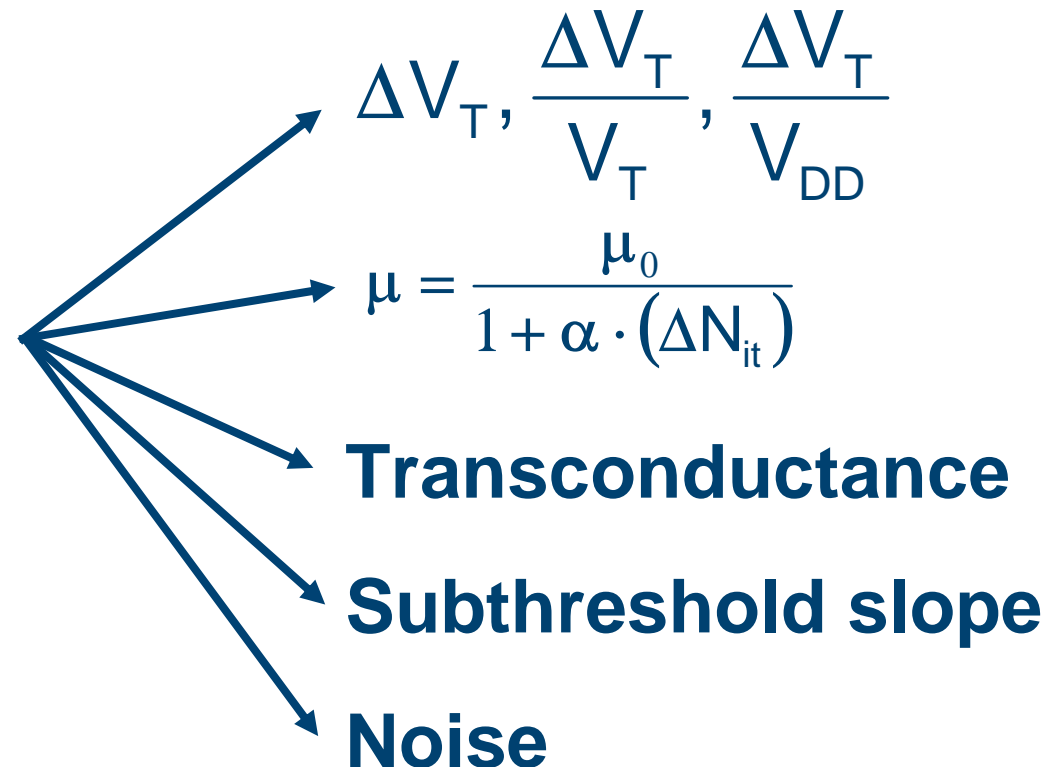


N. S. Saks et al., *IEEE TNS*, vol. 31, no. 6, Dec. 1984, and vol. 33, no. 6, Dec. 1986.



# Total Dose damage and scaling

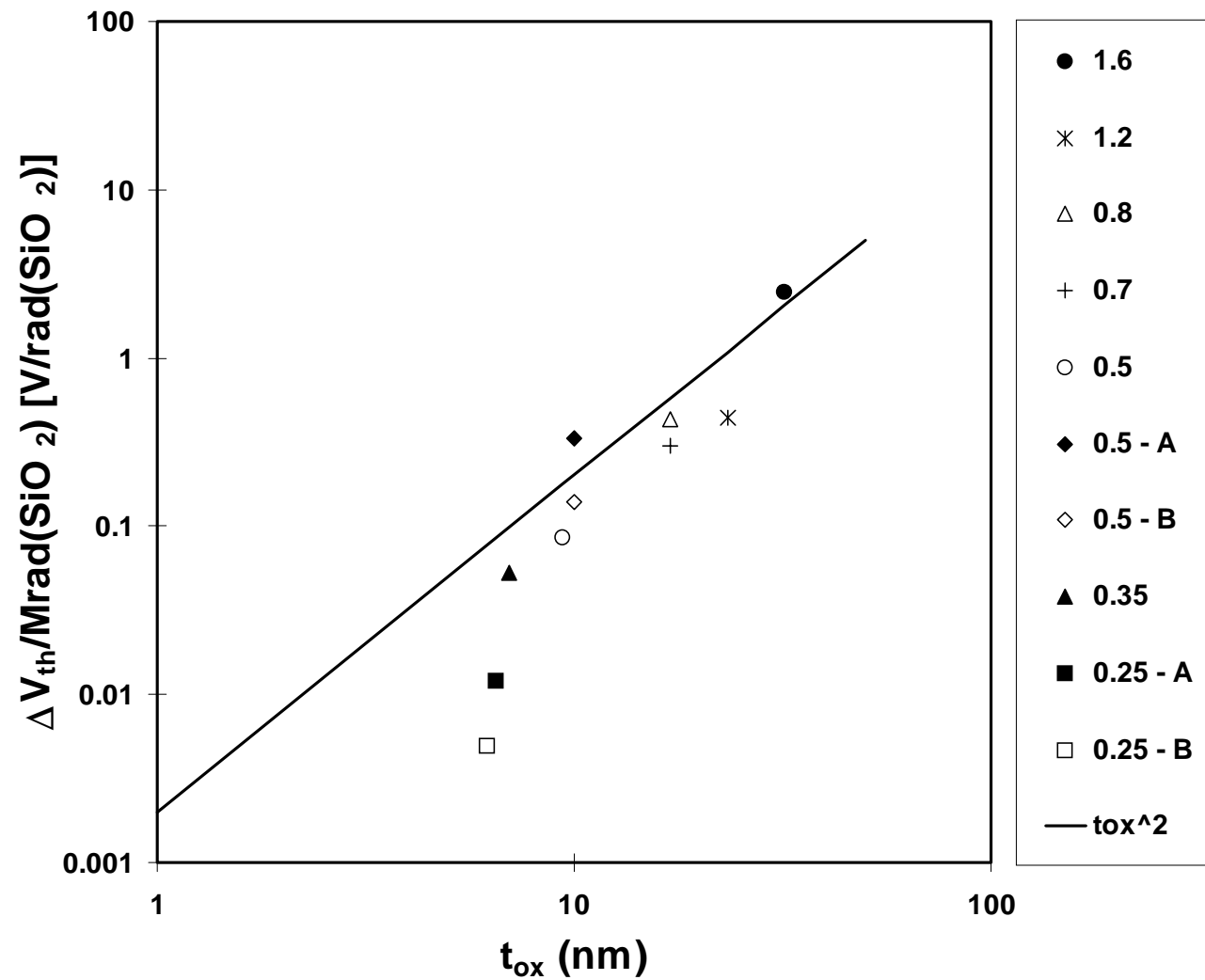
**Decreasing  $t_{ox}$  we decrease the degradation of:**



**And the threshold voltage shift for n-channel transistors might not be negative anymore...**



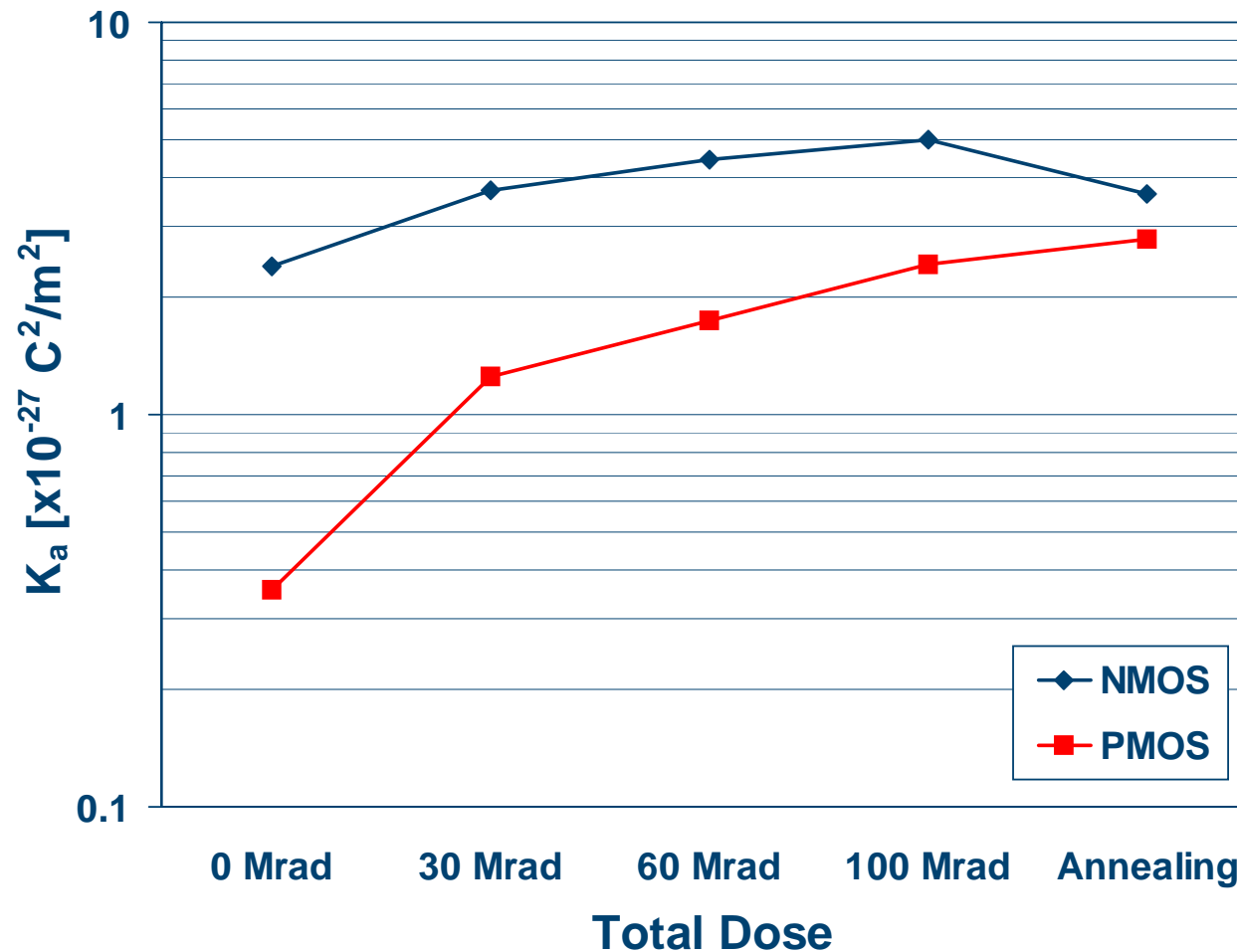
# $\Delta V_T$ and $t_{ox}$ scaling





# 1/f Noise and irradiation

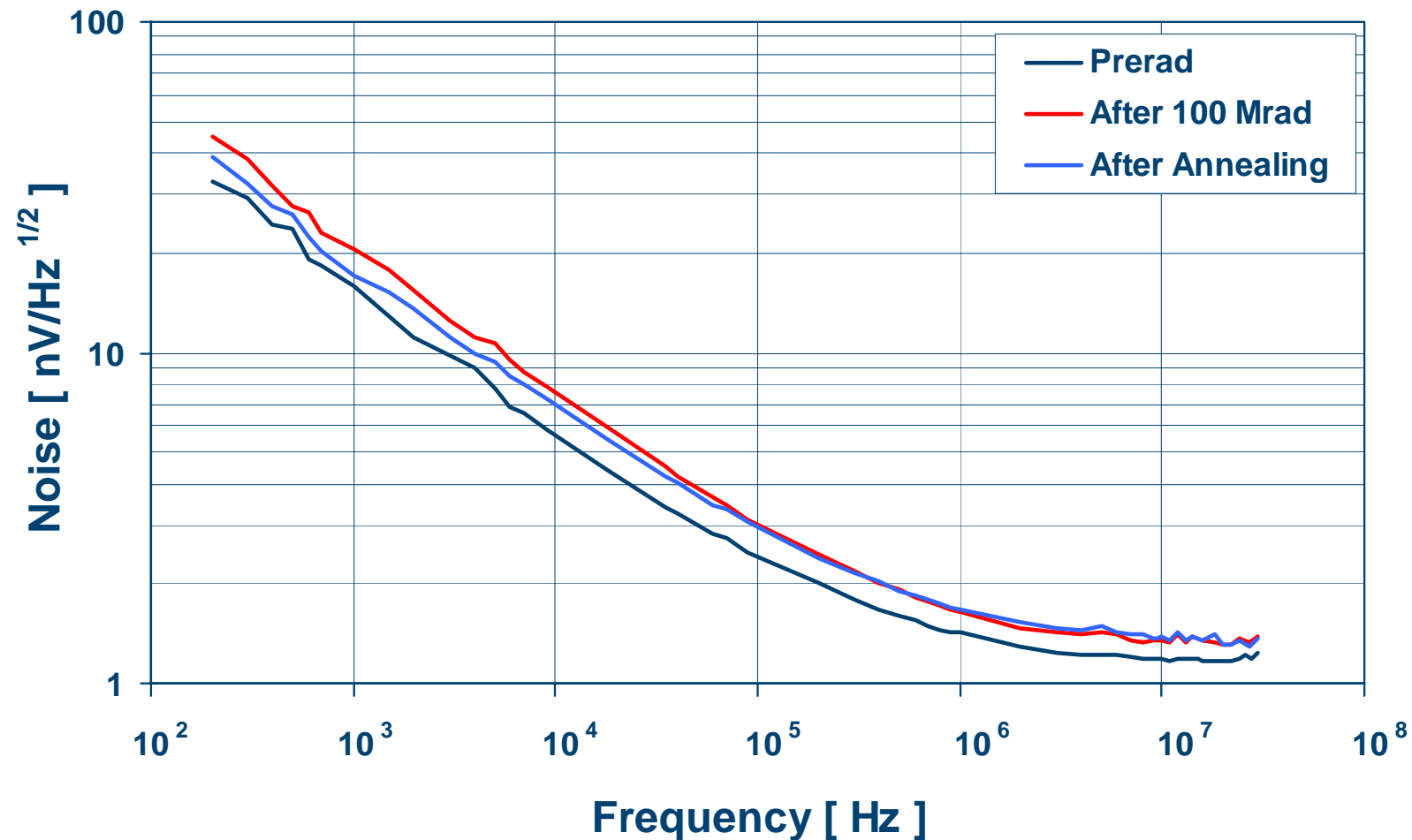
**$W/L = 2000/0.78$ ,  $I_{DS} = 0.5$  mA**





# White noise and irradiation

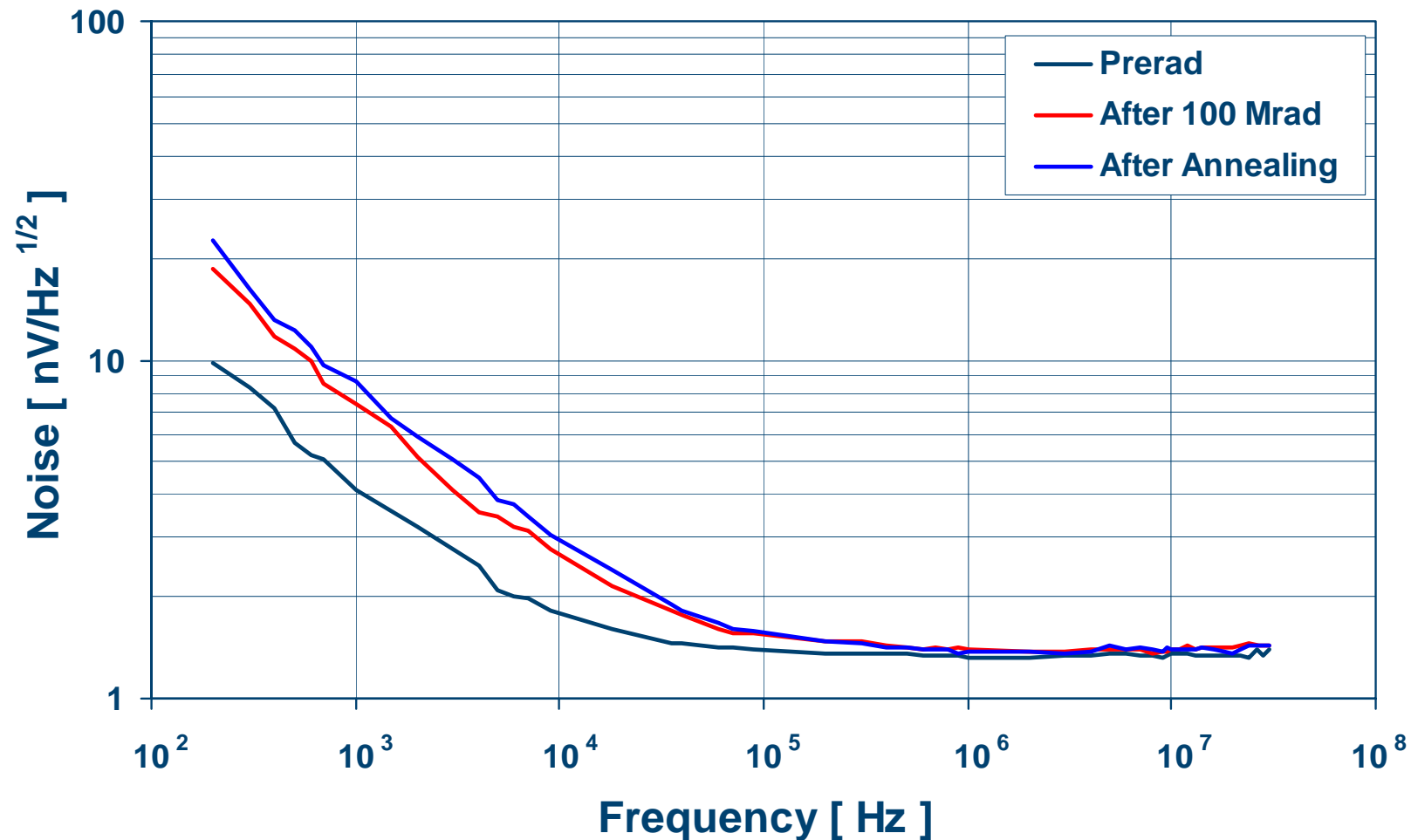
N-channel, ELT,  $W = 2 \text{ mm}$ ,  $I_{DS} = 0.5 \text{ mA}$ ,  $V_{DS} = 0.8 \text{ V}$ ,  $V_{BS} = 0 \text{ V}$





# White noise and irradiation

P-channel,  $W = 2 \text{ mm}$ ,  $I_{DS} = 0.5 \text{ mA}$ ,  $V_{DS} = 0.8 \text{ V}$ ,  $V_{BS} = 0 \text{ V}$

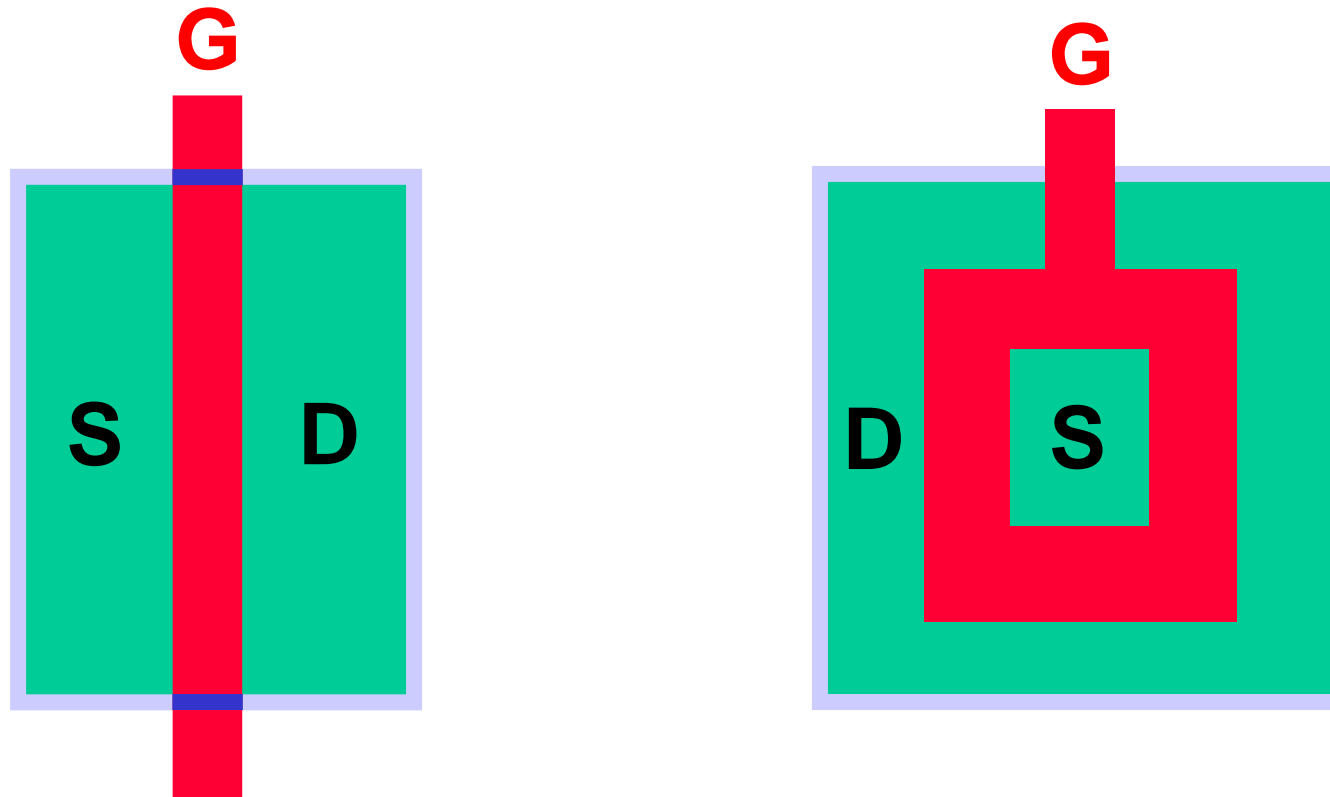






# Enclosed Layout Transistor (ELT)

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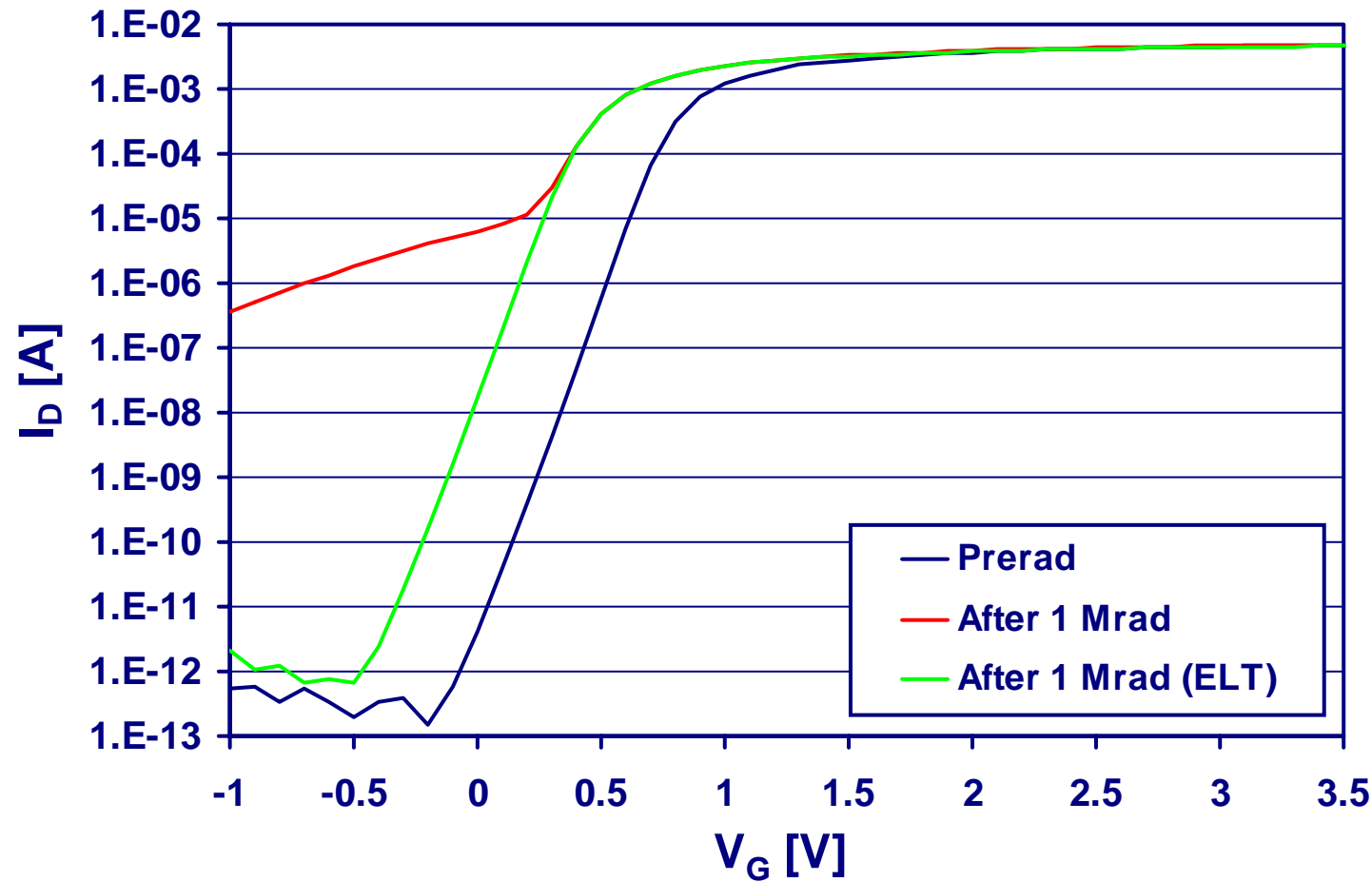


**ELTs solve the leakage problem in the NMOS transistors**  
**At the circuit level, guard rings are necessary**



# Effectiveness of ELTs

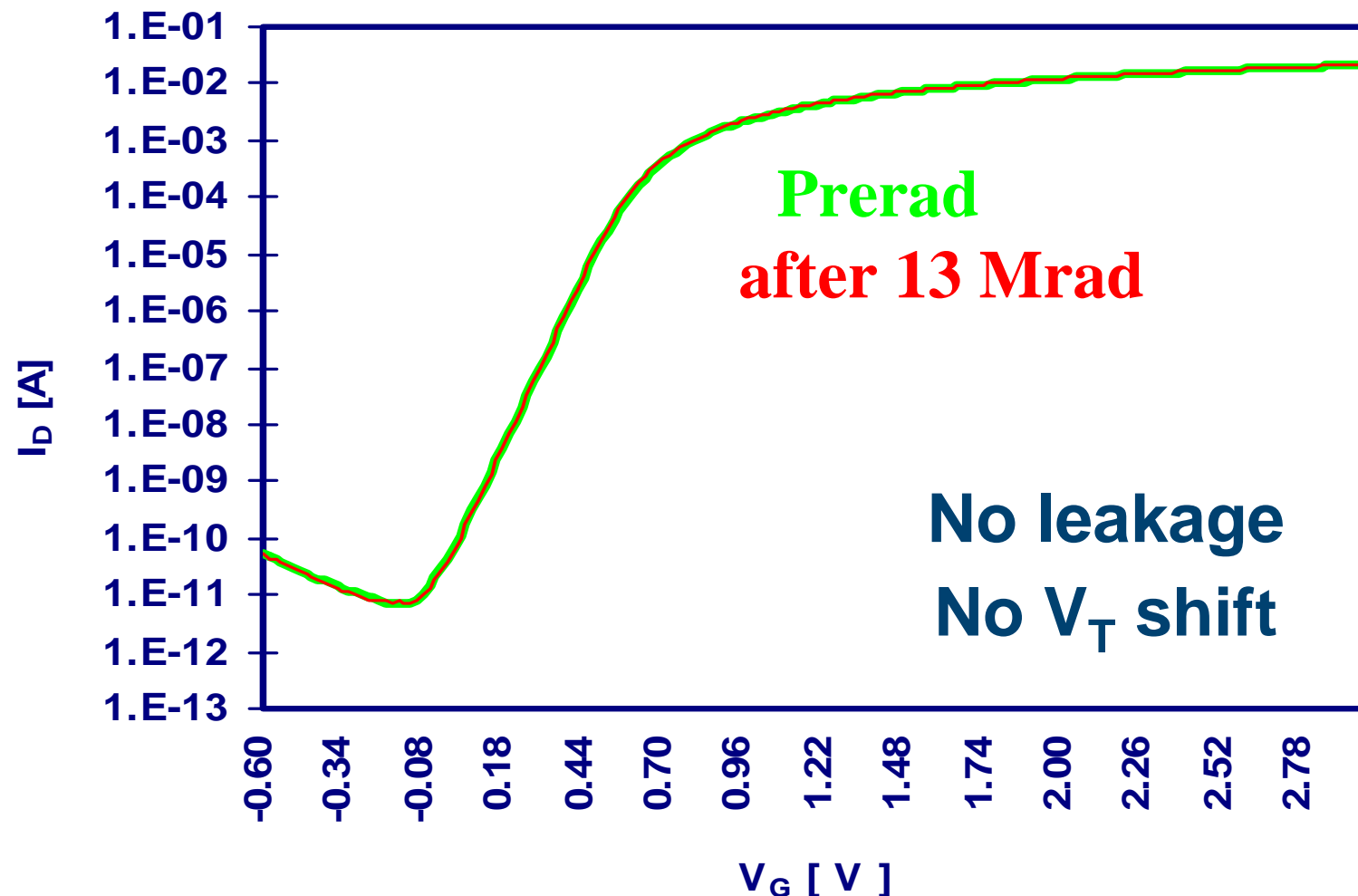
**NMOS - 0.7  $\mu\text{m}$  technology -  $t_{\text{ox}} = 17 \text{ nm}$**





# ELT & deep submicron


NMOS - 0.25  $\mu\text{m}$  technology -  $t_{\text{ox}} = 5 \text{ nm}$





# Outline

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- Scaling down of CMOS technologies
- How scaling works for devices and interconnections
- Scaling impact on noise
- Scaling impact on matching
- Scaling impact on radiation tolerance
-  Analog performance of submicron processes
  - Scaling impact on analog performance
  - Analog design in “digital” processes
  - Integrated capacitors
- Substrate noise in mixed-mode integrated circuits



# Scaling impact on $\mu C_{ox}$

Due to the scaling of the gate oxide thickness, the gate capacitance  $C_{ox}$  increases with scaling. This increases the driving capability of the transistor. For a given  $W/L$  ratio and a fixed bias current, the transconductance also increases with scaling.

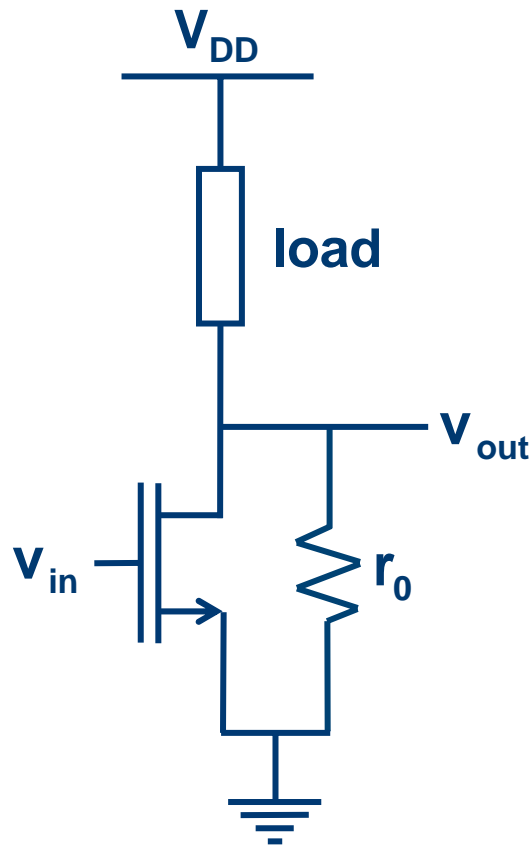
$$g_m = \sqrt{2 \frac{\beta}{n} I_{DS}} = \frac{\beta}{n} (V_{GS} - V_T) \quad \beta = \mu C_{ox} \frac{W}{L}$$

The following data are taken from the design manuals of different CMOS technologies

| $L_{min}$ [ $\mu m$ ] | $t_{ox\_physical}$ [nm] | $t_{ox\_effective}$ [nm] | $C_{ox}$ [fF/ $\mu m^2$ ] | $\mu C_{ox}$ [ $\mu A/V^2$ ] |
|-----------------------|-------------------------|--------------------------|---------------------------|------------------------------|
| 1.2                   | 24                      | ---                      | 1.44                      | 68                           |
| 0.8                   | 17                      | ---                      | 2.03                      | 90                           |
| 0.5                   | 10                      | ---                      | 3.45                      | 134                          |
| 0.25                  | 5.5                     | 6.2                      | 5.5                       | 280                          |
| 0.13                  | 2.2                     | 3.15                     | 10.9                      | 555                          |

N. D. Arora et al., "Modeling the Polysilicon Depletion Effect and Its Impact on Submicrometer CMOS Circuit Performance", *IEEE Transactions on Electron Devices*, vol. 42, no. 5, May 1995, pp. 935-943.

# Intrinsic gain



$$v_{out} = v_{in} \cdot g_m \cdot \frac{r_0 r_{load}}{r_0 + r_{load}}$$

$$\text{Gain} = \frac{v_{out}}{v_{in}} = g_m \cdot \frac{r_0 r_{load}}{r_0 + r_{load}}$$

The quantity  $g_m r_0$  is called intrinsic gain of the transistor. It represents the maximum gain obtainable from a single transistor, and it is a very useful figure of merit in analog design.



# Scaling impact on the intrinsic gain

$$g_m = \frac{\beta}{n} (V_{GS} - V_T)$$

$$\beta = \mu C_{ox} \frac{W}{L}$$

$$I_{DS\_SAT} = \frac{\beta}{2n} (V_{GS} - V_T)^2$$

$$\lambda = \frac{1}{V_{DS}} \cdot \frac{\Delta L}{L - \Delta L} \approx \frac{1}{V_{DS}} \cdot \frac{\Delta L}{L}$$

$$\Delta L \approx \sqrt{\frac{2\epsilon_{Si}}{qN_a}} \sqrt{V_{DS}}$$

$$g_{out} = \lambda \cdot I_{DS\_SAT}$$

$$r_o = \frac{1}{g_{out}} = \frac{1}{\lambda \cdot I_{DS\_SAT}}$$

$$\text{Intrinsic Gain} = g_m \cdot r_o$$

Supposing to have constant field scaling for the technology, we obtain:

| L          | W          | $\beta$    | $V_{GS}-V_T$ | $g_m$      | $V_{DS}$   | $\Delta L$ | $\lambda$ | $I_{DS\_SAT}$ | $g_{out}$    | $r_o$        | $g_m r_o$ |
|------------|------------|------------|--------------|------------|------------|------------|-----------|---------------|--------------|--------------|-----------|
| $1/\alpha$ | $1/\alpha$ | $\alpha$   | $1/\alpha$   | 1          | $1/\alpha$ | $1/\alpha$ | $\alpha$  | $1/\alpha$    | 1            | 1            | 1         |
| 1          | $1/\alpha$ | 1          | $1/\alpha$   | $1/\alpha$ | $1/\alpha$ | $1/\alpha$ | 1         | $1/\alpha^2$  | $1/\alpha^2$ | $\alpha^2$   | $\alpha$  |
| 1          | 1          | $\alpha$   | $1/\alpha$   | 1          | $1/\alpha$ | $1/\alpha$ | 1         | $1/\alpha$    | $1/\alpha$   | $\alpha$     | $\alpha$  |
| $1/\alpha$ | $\alpha$   | $\alpha^3$ | $1/\alpha$   | $\alpha^2$ | $1/\alpha$ | $1/\alpha$ | $\alpha$  | $\alpha$      | $\alpha^2$   | $1/\alpha^2$ | 1         |





# Analog power consumption

---

$t_{ox}$  scales  $\longrightarrow$   $V_{DD}$  must be scaled as well

**Min. power consumption for class A analog circuits:**

$$P_{min} = 8 \pi kT \cdot SNR \cdot f_{sig} \cdot \frac{V_{DD}}{V_{DD} - \Delta V}$$

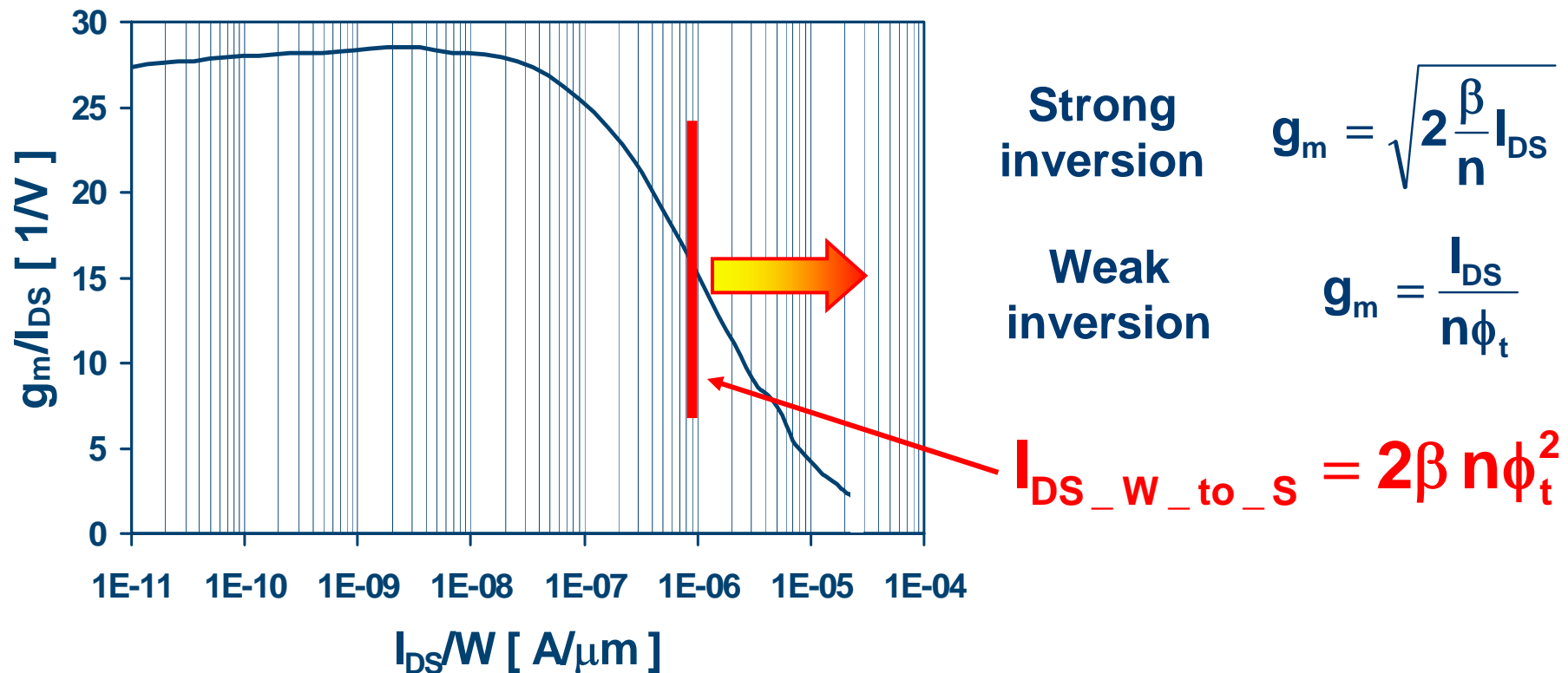
$\Delta V$  is the fraction of the  $V_{DD}$  not used for signal swing

**Optimal analog power/performance trade-off  
for 0.35 - 0.25  $\mu m$  technologies**



# Weak inversion region

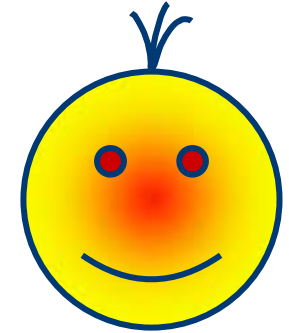
$t_{ox}$  scales  $\longrightarrow$  for the same device dimensions the boundary between weak inversion and strong inversion moves towards higher currents





# Scaling impact on analog circuits

$t_{ox}$  scales  $\longrightarrow$  for the same device dimensions



- Threshold voltage matching improves  $\sigma_{\Delta V_{th}} = \frac{\text{Const} \cdot t_{ox}}{\sqrt{W L}}$

- 1/f noise decreases  $\frac{\overline{v_{in\_1/f}^2}}{\Delta f} = \frac{K_a}{C_{ox}^2 W L} \frac{1}{f^\alpha}$

- Transconductance increases (same current)  $g_m = \sqrt{\frac{2}{n} \mu C_{ox} \frac{W}{L} I_{DS}}$

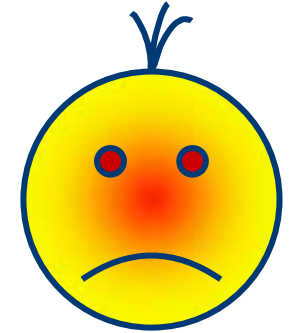
- White noise decreases



# Scaling impact on analog circuits

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- New noise mechanisms
- Modeling difficulties
- Lack of devices for analog design
- Reduced signal swing (new architectures needed)
- Substrate noise in mixed-signal circuits
- Velocity saturation. Critical field: 3 V/ $\mu\text{m}$  for electrons,  
10 V/ $\mu\text{m}$  for holes



$$g_{m\_vel.sat.} = WC_{ox} v_{sat}$$



# Analog design in digital processes

The integrated circuits market is driven by digital circuits, such as memories and microprocessors. This led to an increasing interest in integrating analog circuits together with digital functions in processes optimized for digital circuits, making what it is called a System on a Chip (SoC). This approach has several **advantages** and **disadvantages**.

## ADVANTAGES:

- Lower wafer cost
- Higher yield
- Higher speed
- Lower power consumption (not always)
- Complex digital functions on chip (DSP)

## DISADVANTAGES:

- Low power supplies
- Lack of “analog” components
- Inadequate modeling
  - Output conductance
  - Different inversion regions
- “Digital” noise

- E. A. Vittoz, "The Design of High-Performance Analog Circuits on Digital CMOS Chips", *IEEE JSSC*, vol. 20, no. 3, June 1985, pp. 657-665.
- W. Sansen, "Challenges in Analog IC Design in Submicron CMOS Technologies", *Proceedings of the 1996 IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design*, Pavia, Italy, 13-14 September 1996, pp. 72-78.
- C. Azaredo Leme and J. E. Franca, "Analog-Digital Design in Submicrometric Digital CMOS Technologies", *Proceedings of the 1997 IEEE International Symposium on Circuits and Systems*, Hong Kong, 9-12 June 1997, vol. 1, pp. 453-456.



# Analog components availability

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**Analog design needs high-quality passive components. These are not present in processes optimized for digital design, or at least not in the first stages of the process development. These analog “options” are:**

- **High-resistivity poly for resistors**
- **Diffusion resistors**
- **Trimming options**
- **Linear and dense capacitors**
  - **Metal to metal (at least one special metal layer required)**
  - **Metal to poly**
  - **Poly to poly**



# Integrated capacitors

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- **High-linearity capacitors can be obtained with metal-to-metal structures. This generally requires adding a special metal layer to the technology, in order to reduce the dielectric thickness between the metal plates. The density reached is generally below 1 fF/μm<sup>2</sup> (not very high...).**
- **Dense capacitors can be obtained exploiting the high capacitance density of the thin gate oxide. This allows having dense and precise capacitors, good matching but very poor linearity. This solution can be adopted in any process.**
- **A third possible solution is suggested by the availability of many interconnection layers. Exploiting the parasitic capacitance between metal wires in a clever way, one can obtain linear capacitors with good matching and linearity and densities up to 1.5 fF/μm<sup>2</sup>. These capacitors can be integrated in any process!!**

- A. T. Behr et al., "Harmonic Distortion Caused by Capacitors Implemented with MOSFET Gates", *IEEE JSSC*, vol. 27, no. 10, Oct. 1992, pp. 1470-1475.
- D. B. Slater, Jr. and J. J. Paulos, "Low-Voltage Coefficient Capacitors for VLSI Processes", *IEEE JSSC*, vol. 24, no. 1, February 1989, pp. 165-173.
- J. L. McCreary, "Matching Properties, and Voltage and Temperature Dependence of MOS Capacitors", *IEEE JSSC*, vol. 16, no. 6, Dec. 1981, pp. 608.
- S. Pavan, Y. Tsvividis and K. Nagaraj, "Modeling of accumulation MOS capacitors for analog design in digital VLSI processes", *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems*, Orlando, Florida, USA, 30 May – 2 June 1999, vol. 6, pp. 202-205.



# Multi-metal-layer capacitors

This solution is a possibility, but it does not exploit the fact that in deep submicron processes the highest parasitic capacitance can be obtained “horizontally” rather than vertically, i.e.  $t_{ox} > s$

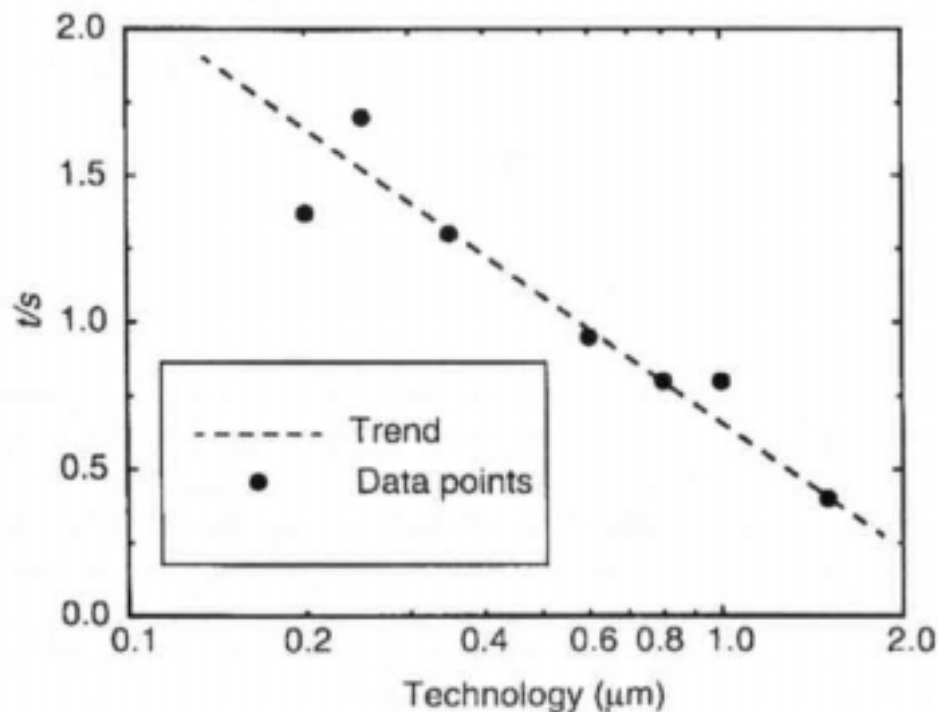
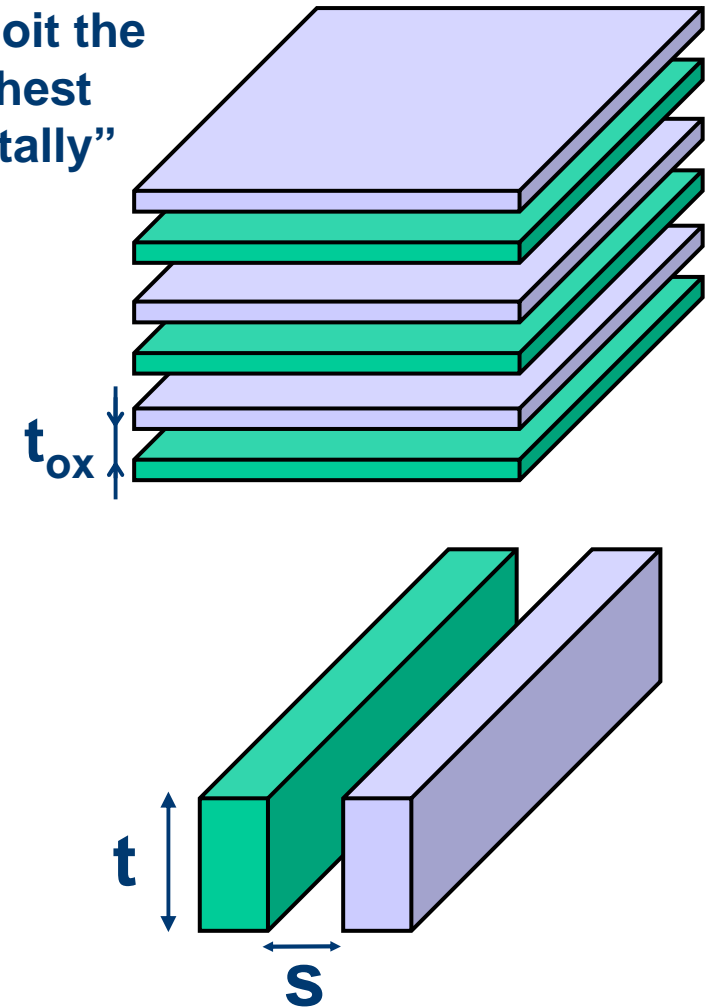


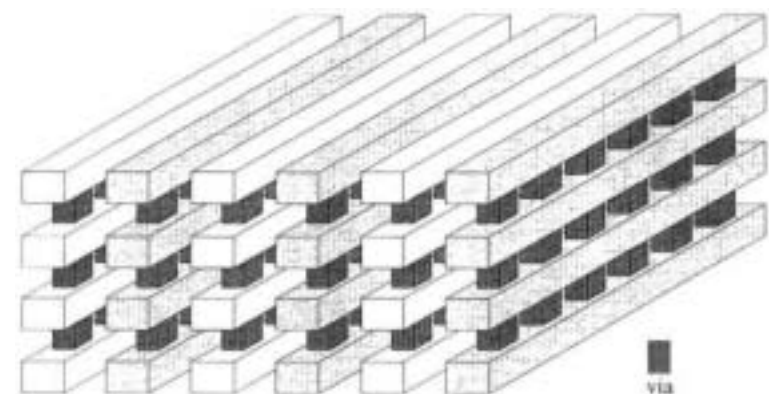
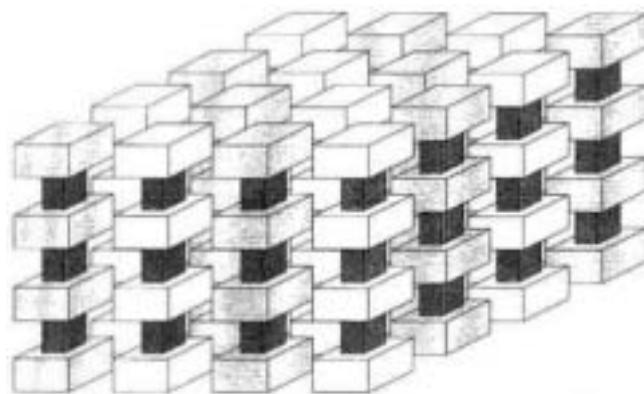
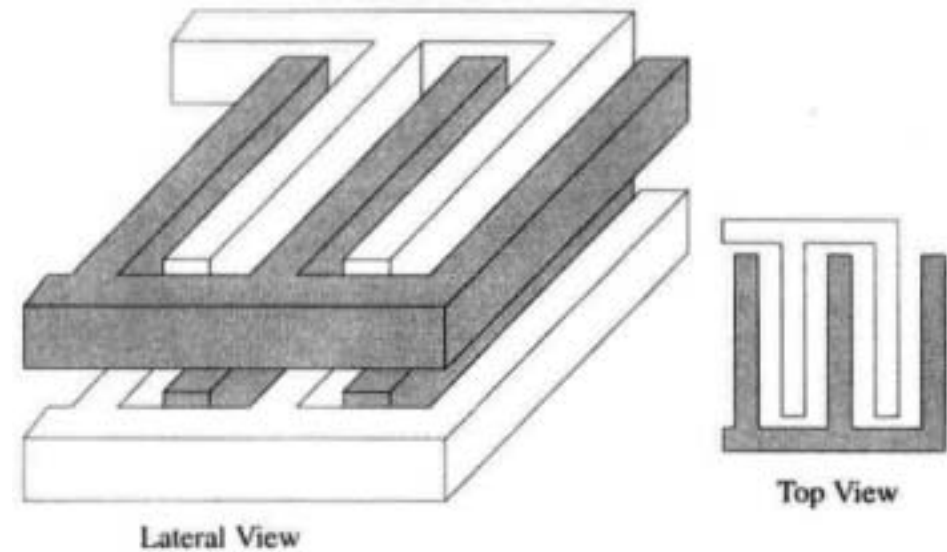
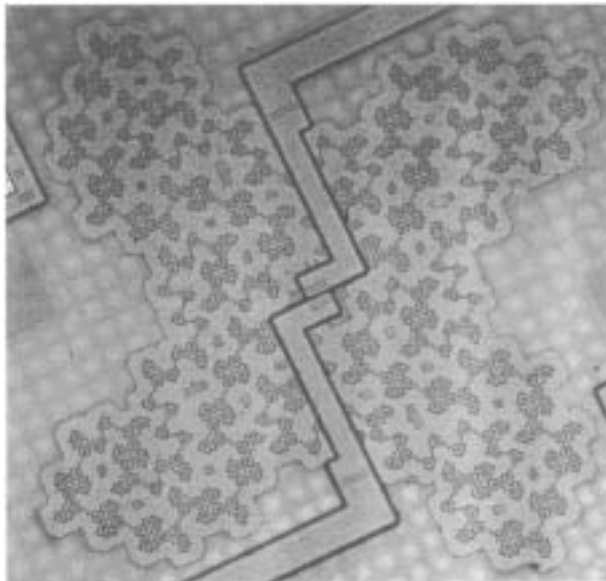
Fig. 3. Ratio of metal thickness to horizontal metal spacing versus technology (channel length).



- Hiran Samavati et al., “Fractal Capacitors”, *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, December 2002, pp. 2035-2041.



# Multi-metal-layer capacitors

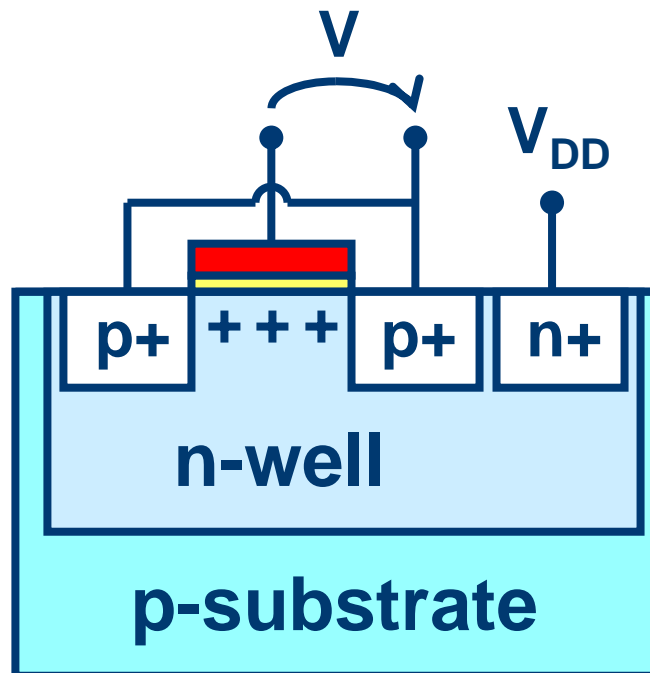


- Hiran Samavati et al., "Fractal Capacitors", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, December 2002, pp. 2035-2041.
- R. Aparicio and A. Hajimiri, "Capacity Limits and Matching Properties of Integrated Capacitors", *IEEE JSSC*, vol. 37, no. 3, March 2002, pp. 384-393.

# MOS capacitors

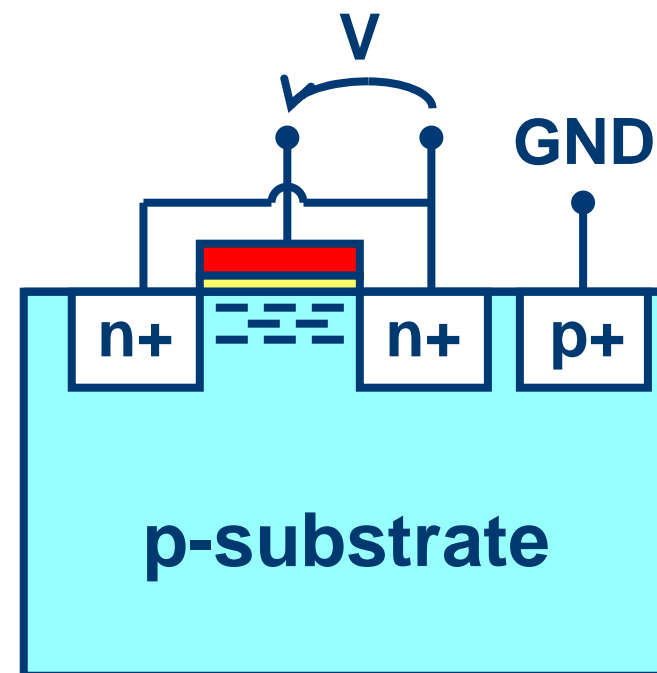
## PMOS

### Inversion Region



## NMOS

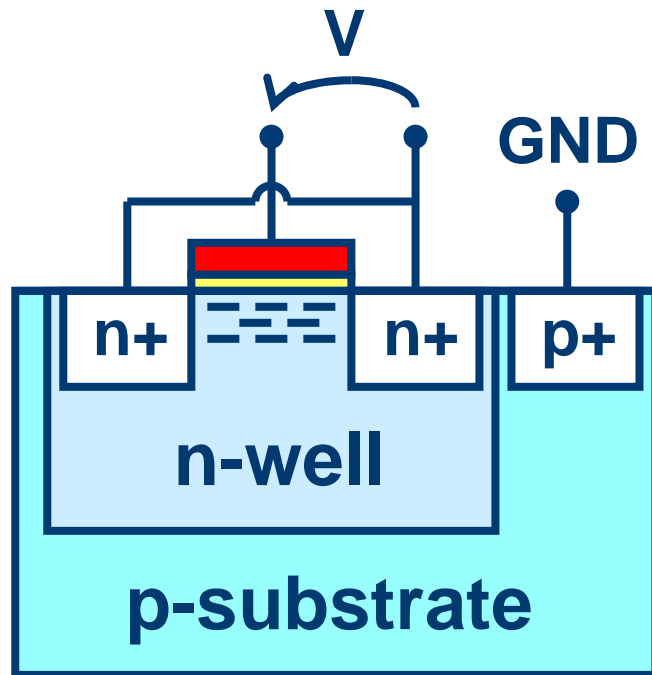
### Inversion Region



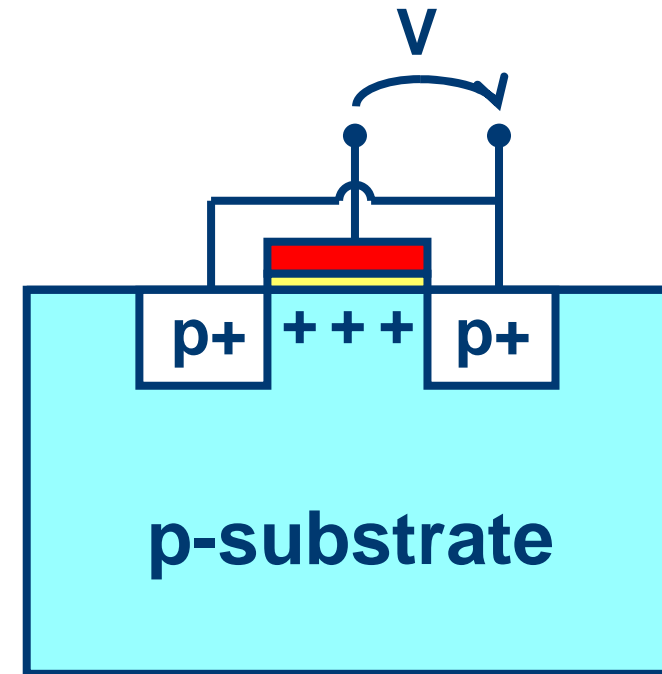


# MOS capacitors

## NMOS in an N well Accumulation Region

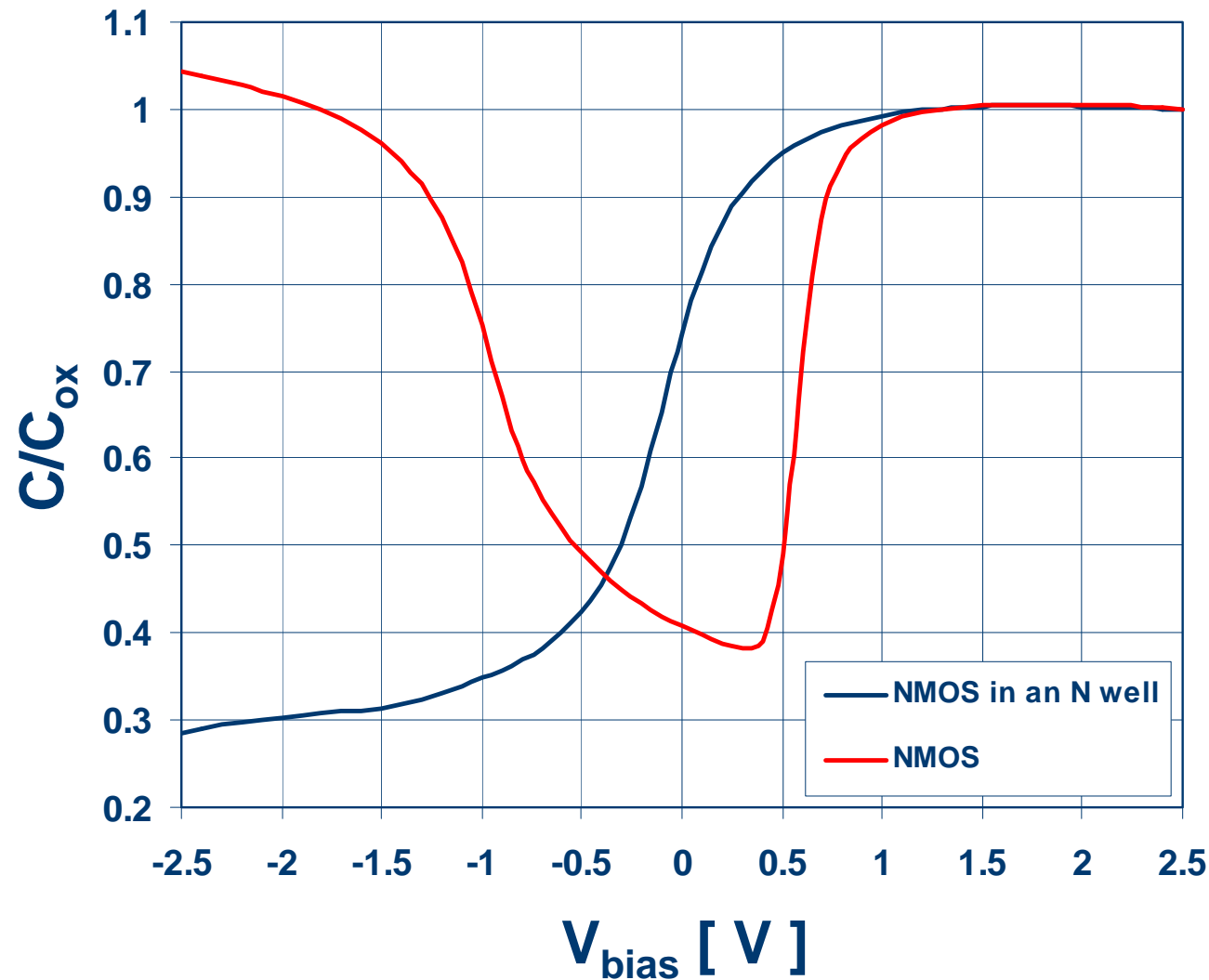


## MOS structure Accumulation Region





# C-V characteristics



**The NMOS in an N well capacitor is in accumulation for  $V > 0$  V.**

**The NMOS capacitor is in inversion for  $V > 0$ .**



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- Substrate noise in mixed-mode integrated circuits



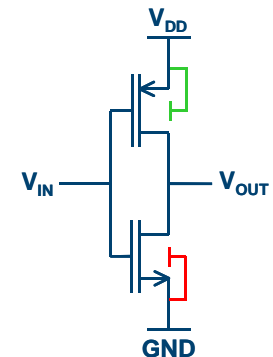


# Digital noise in mixed-signal ICs

Integrating analog blocks on the same chip with digital circuits can have some serious implications on the overall performance of the circuit, due to the influence of the “noisy” digital part on the “sensitive” analog part of the chip.

The switching noise originated from the digital circuits can be coupled in the analog part through:

- The power and ground lines
- The parasitic capacitances between interconnection lines
- The common substrate

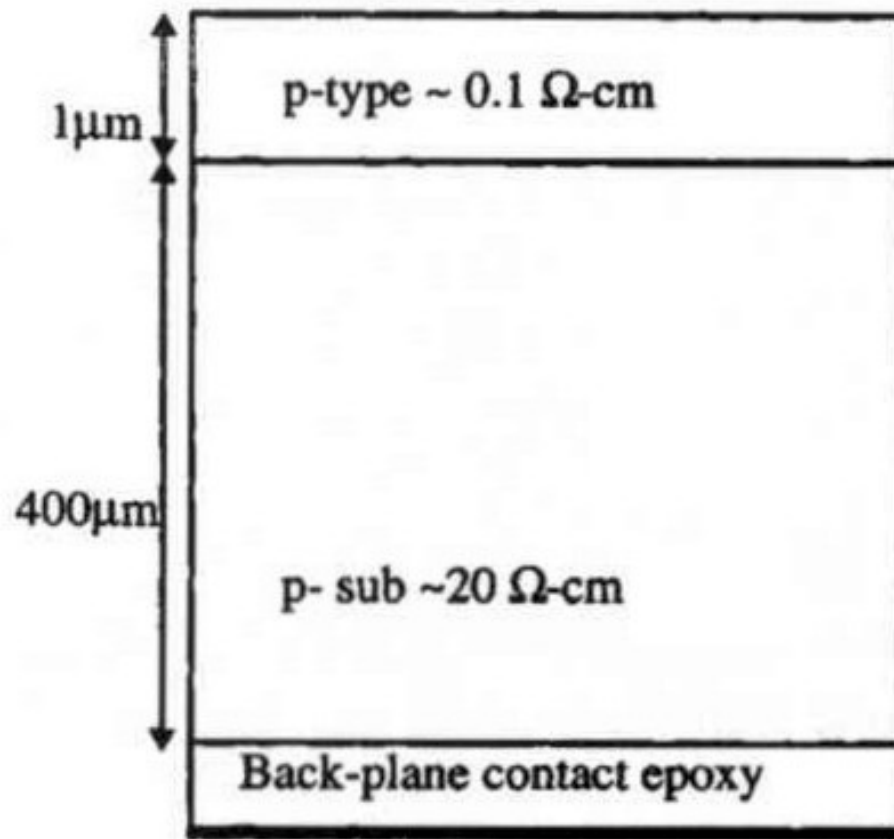


**The substrate noise problem is the most difficult to solve.**

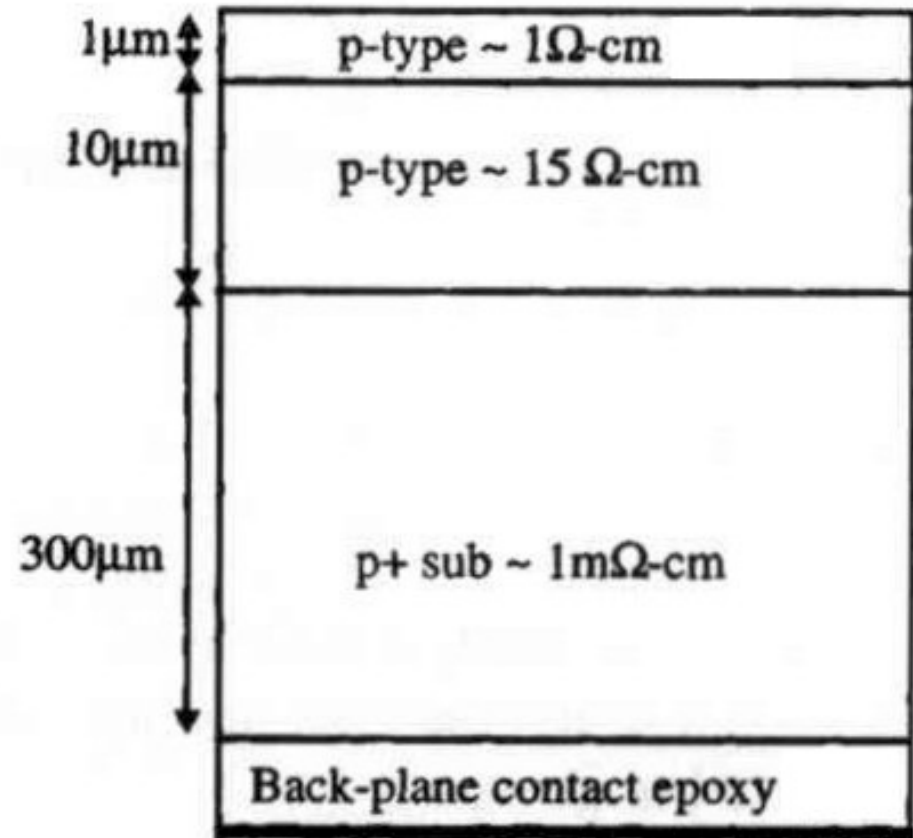
- A. Samavedam et al., "A Scalable Substrate Noise Coupling Model for Design of Mixed-Signal IC's", *IEEE JSSC*, vol. 35, no. 6, June 2000, pp. 895-904.
- N. K. Verghese and D. J. Allstot, "Computer-Aided Design Considerations for Mixed-Signal Coupling in RF Integrated Circuits", *IEEE JSSC*, vol. 33, no. 3, March 1998, pp. 314-323.
- M. Ingels and M. S. J. Steyaert, "Design Strategies and Decoupling Techniques for Reducing the Effects of Electrical Interference in Mixed-Mode IC's", *IEEE Journal of Solid-State Circuits*, vol. 32, no. 7, July 1997, pp. 1136-1141.



# Different types of substrates



High-Resistivity Substrate



Low-Resistivity Substrate

R. Gharpurey and R. G. Meyer, "Modeling and Analysis of Substrate Coupling in Integrated Circuits", *IEEE JSSC*, vol. 31, no. 3, 1996, pp. 344-353.





# Substrate noise: how to reduce it

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**To minimize the impact of disturbances coming from the substrate on the sensitive analog blocks, we have mainly three ways:**

- **Separate the “noisy” blocks from the “quiet” blocks. This is effective especially in uniform lightly doped substrates. For heavily doped substrates, it is useless to use a separation greater than about 4 times the epitaxial layer thickness.**
- **In n-well processes, p+ guard rings can be used around the different blocks. Unfortunately, this is again effective mainly for lightly doped substrates. Guard rings (both analog and digital) should be biased with separate pins.**
- **The most effective way to reduce substrate noise is to ground the substrate itself in the most “solid” possible way (no inductance between the substrate and ground). This can be done using many ground pins to reduce the inductance, or, even better, having a good contact on the back of the chip (metallization) and gluing the chip with a conductive glue on a solid ground plane.**
- **Separate the ground contact from the substrate contact in the digital logic cells, to avoid to inject the digital switching current directly into the substrate.**

D. K. Su, M. J. Loinaz, S. Masui and B. A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits", *IEEE Journal of Solid-State Circuits*, vol. 28, no. 4, April 1993, pp. 420-429.