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Essential Physics of Ballistic Nanotransistors: An Introduction with FETToy 2.0

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These are preliminary lecture notes, intended only for distribution to participants.

Essential Physics of Ballistic Nanotransistors:

An Introduction with FETToy 2.0

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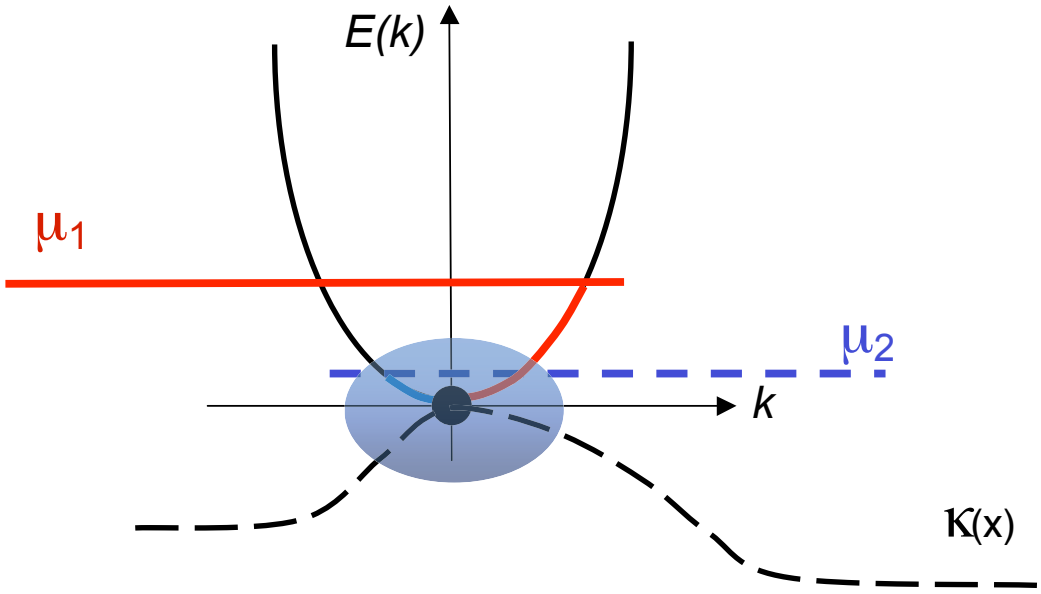

1. Introduction

The transistor has been called the most important invention of the 20th century. Along with the integrated circuit it made possible the computing and communications systems that shaped the modern world. Moore's Law, the doubling of the number of transistors per chip each technology generation, describes progress in integrated circuit technology. This doubling occurs because the linear dimensions of a transistor shrink by $1/\sqrt{2}$ each technology generation so that the area drops by a factor of two and twice as many transistors can fit on a chip. Current day technology (the so-called 90 nm technology node) manufactures transistors with 50 nm channel lengths using gate oxides less than 2 nm thick. Present-day silicon MOSFETs are, therefore, true nanoelectronic devices.

The grand challenges in digital electronics currently have to do with understanding the scaling limit of the silicon transistor, developing manufacturing technologies to reach that limit, learning how to design systems with such devices, and exploring new devices that might supplement (or possibly even replace) ultimate CMOS. Silicon MOS transistors with channel lengths of only 5 or 6 nm have already been produced [1, 2]. The traditional way of understanding MOSFETs was developed 40 years ago based on macroscopic concepts. To understand the ultimate limits of silicon transistors and to explore new devices that are designed and manufactured at the molecular scale, we need to learn how to think about transistors differently. These notes are an introduction to the basic operating principles of nanoscale transistors. A simple, toy model (FETToy, which is available on the web for live simulations), is used to illustrate some key concepts.

2. Physics of Ballistic Nanotransistors

Before we begin, it is important to understand that there are two different kinds of field-effect transistors. Traditionally, we think about a MOSFET in terms of the charge in the channel that is induced by the gate voltage. The contacts to the channel (the heavily doped source and drain regions) are "perfect" in the sense that they can supply to the channel any charge that the gate voltage demands. Alternatively, one can build a Schottky-barrier transistor, in which metals replace the doped source and drain regions. In this case, there is a Schottky barrier between the source and the channel. Transistor action occurs because the gate voltage modulates the width of the Schottky barrier, and, therefore, the tunneling current. It is important to understand which kind of transistor we are dealing with, because if we apply a MOSFET model to a SB FET and extract a mobility, it will have no physical significance. In general, a field-effect transistor will operate somewhere between the two limits of MOSFET-like or SB-like [3]. FETToy deals only with ballistic MOSFET-type field-effect transistors.

In the ballistic limit, carriers travel through a MOSFET without scattering. It is relatively easy to understand the physics of a ballistic nanotransistor, and to simulate its current vs. voltage characteristics. Understanding a ballistic transistor then provides a good starting point for adding complications, such as the scattering that is present in real devices. References [10] and [11] give an introductory overview of the physics of nanotransistors. In these notes, we discuss only a few essential physical ideas for the ballistic case.

Figure 1 shows the conduction band energy vs. position for a MOSFET under high drain bias. For low gate voltages (i.e. below threshold), there is a large energy barrier between the source and drain, so the current is low. A positive gate voltage pushes the energy barrier down, so that current can flow. One typically analyzes a MOSFET in terms of the charge in the channel, but it is actually the modulation of the energy barrier height by the gate voltage that permits charge to flow into the channel from the source.

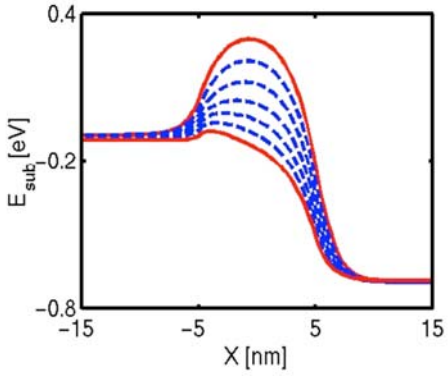

Fig. 1 Energy band diagrams (actually, the first conduction subband) vs. position) for a 10 nm channel length silicon MOSFET under high drain bias. With increasing gate voltage, the energy barrier between the source and drain decreases, and charge can flow.

Figure 2 is a sketch of the energy band profile under high gate and drain bias. We are interested in how the electronic states at the top of the energy barrier (beginning of the channel) are filled as a function of bias. For a well-designed MOSFET above threshold, the charge at the beginning of the channel is controlled mostly by the gate voltage according to

$$Q(0) - C_G\left(V_{GS} - V_T\right) \quad \text{C/cm}, \tag{1}$$

where C_G is the gate to source capacitance and V_T is the threshold voltage. This charge is accommodated in the electronic states at the top of the barrier.

Before we discuss the filling of the electronic states, we should briefly discuss units and the gate capacitance. The charge is in Coulombs per unit length (in the direction of the channel), and the gate capacitance is in units of Farads per unit length. For a MOSFET, we usually specify the oxide capacitance as

$$C_{ins} = \frac{\varepsilon_{ins}\varepsilon_0}{t_{ins}} \quad \text{F/cm}^2, \tag{2}$$

so the gate capacitance per unit length for a MOSFET is

$$C_G \approx W\, C_{ins}, \tag{3}$$

where W is the width of the MOSFET. For a nanowire MOSFET with the simple, cylindrical gating geometry assumed by FETToy, the gate capacitance is

$$C_{ins} = \frac{2\pi\varepsilon_{ins}\varepsilon_0}{\ln\left|\frac{2t_{ins} + t_{wire}}{t_{wire}}\right|} \text{ F/cm}, \tag{4}$$

where t_{wire} is the diameter of the nanowire. For the nanowire transistor, $C_G \approx C_{ins}$.

The reader will notice that the gate capacitance is only approximately the insulator capacitance. It is important to understand why. The reason is that the insulator capacitance is in series with the semiconductor capacitance [4], so the series combination is lower than the insulator capacitance. In a bulk MOSFET, the semiconductor capacitance is the depletion capacitance below threshold and the inversion layer capacitance above threshold. For ultra-thin body, fully depleted MOSFETs, only the inversion layer capacitance is important. This capacitance (sometimes called the quantum capacitance) is related to the density of states in the semiconductor by

$$C_Q = q^2\left\langle D(E_F)\right\rangle \text{ F/cm}, \tag{5}$$

where D is the density of states per unit energy and length. Equation (5) states that the semiconductor (or quantum) capacitance is proportional to the average density of states near the Fermi level. Until recently, the semiconductor capacitance above threshold was much greater than the insulator capacitance. This issue could be ignored and the gate capacitance was essentially the insulator capacitance. When the insulator is very thin or has a high dielectric constant or when the density of states in the semiconductor is low (e.g. when the effective mass is light), then the quantum capacitance can substantially lower the gate capacitance [5, 6].

The gate capacitance and the gate voltage determine the charge at the top of the barrier. That charge comes from electrons injected into the channel from the source and drain contacts, and it resides in the electronic states at the top of the barrier. In general, the local density of states at the top of the barrier needs to be computed from a quantum approach. Quantum tunneling introduces states below the bottom of the conduction band, and quantum interference influences states above the bottom of the conduction band. If we are dealing with a semiconductor transistor whose channel length is not exceptionally short (greater than about 10 nm for Si), however, then we can describe the local density of states at the top of the barrier by the *E(k)* relation for the corresponding bulk semiconductor, as sketched in Fig. 2.

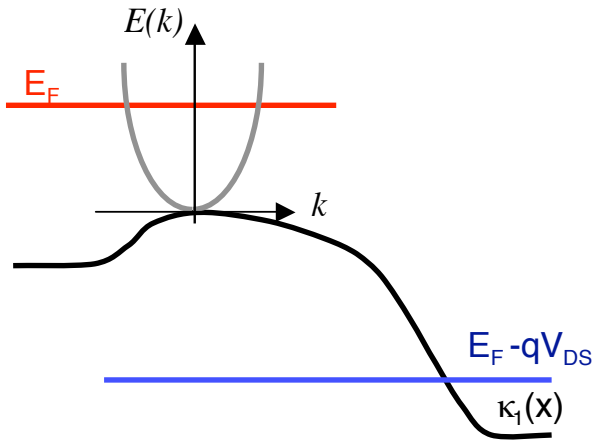

Fig. 2 *E-k* relation at the top of the source-channel barrier showing the source and drain Fermi levels, E_F and $E_F - qV_{DS}$. A high gate voltage, which sets the location of the Fermi level in the conduction subband, and a large drain voltage are assumed.

The states at the top of the barrier come in two flavors – those that can only be occupied by injection of electrons from the source and those that can be occupied only by injection from the drain. One can show that under ballistic conditions, the +k states at the top of the barrier are occupied by an equilibrium Fermi function with the appropriate Fermi level being that of the source. The –k states are also occupied according to an equilibrium Fermi function, but with the Fermi level being that of the drain. We conclude that the total charge at the top of the barrier has two components, one part having positive velocities and determined by the source Fermi level and one part having negative velocities and determined by the drain Fermi level. (This is what makes the ballistic case so easy. All positive velocity carriers at the top of the barrier must have come from the source, and all negative velocity carriers must have come fro the drain. When scattering is present, the two streams of carriers get mixed up, and things become much more complicated.)

In the ballistic case,

$$Q(0) = q\left(n^+(E_F) + n^-(E_F - qV_D)\right). \tag{6}$$

Similarly, there is a positive current determined by the source Fermi level and a negative current determined by the drain Fermi level, and the net current is

$$I_D = I^+(E_F) - I^-\left(E_F - qV_D\right). \tag{7}$$

By writing $I^+ = qn^+\upsilon^+$ and $I^\upsilon = qn^\upsilon\upsilon^\upsilon$, we can express the drain current as

$$I_D = Q(0)/^{+}\left|\frac{1 \mid n^{|}/^{|}/n^{+}/^{+}}{1+n^{|}/n^{+}}\right|. \tag{8}$$

Under non-degenerate conditions, $-^{+} = -^{-} = -_T$, the thermal velocity, and carrier densities are related exponentially to the Fermi level, so $n^{-}/n^{+} = e^{-qV_D/k_BT}$. The result is a very simple expression for the *I-V* characteristic of a ballistic MOSFET,

$$I_D = Q(0)/_T\left|\frac{1 \mid e^{|qV_D/k_BT}}{1+e^{|qV_D/k_BT}}\right| = C_G/_T(V_G \mid V_T)\left|\frac{1 \mid e^{|qV_D/k_BT}}{1+e^{|qV_D/k_BT}}\right|. \tag{9}$$

In practice, the semiconductor is degenerate above threshold, so the exponentials have to be replaced with Fermi-Dirac integrals, and the thermal velocity is a function of the position of the Fermi level. Although over simplified, eqn. (9) does illustrate some key points. For example, under high drain bias, the so-called on current is

$$I_D = C_G -_T (V_{GS} - V_T), \tag{10}$$

which is just like the traditional velocity saturated expression, which occurs when scattering limits the velocity to υ_{sat}, except that the equilibrium thermal injection velocity replaces the saturated velocity. Under low drain bias, we find

$$I_D = \left|C_G(V_{GS} \mid V_T)\frac{/_T/2}{k_BT/q}\right|V_D = G_{CH}V_D, \tag{12}$$

which shows that a ballistic MOSFET has a finite channel resistance. We might have expected it to be zero, because the mobility for a ballistic MOSFET is effectively infinite. When fully degenerate (i.e. at T = 0K), the channel conductance is simply the well-known quantum conductance of $2e^2/h$ per conducting mode [7].

This brief discussion indicates that ballistic MOSFETs can behave in unexpected ways. The FETToy exercises will allow you to gain some "feel" for the physics of ballistic nanotransistors. For a more thorough discussion of nanotransistor physics, see [8, 9, 10].

3. A Word Abut FETToy2.0

FETToy is a Matlab script that computes the current vs. voltage characteristics of ballistic, field effect nanotransistors. It implements the ideas discussed in Sec. 2, without the assumption that of nondegenerate carrier statistics. FETToy 2.0 treats MOSFETs with 2D channels as well as nanowire transistors with 1D channels. A simple capacitor model treats 2D electrostatics, which allows $Q(0)$ to be computed as a function of both the gate and drain bias. FETToy assumes a simple, parabolic $E(k)$ relation (or a numerical E(k) table for carbon nanotubes), but more complex energy bands can also be treated [9]. The underlying theory was first developed by Natori [11] and generalized by Rahman, et al. [9]. It is described more fully in the monograph by Lundstrom [10].

4. Running FETToy on the Simulation Hub

FETtoy can be accessed from www.nanohub.org by selecting Online Simulation. First log on to the simulation hub and request an account (one is created for you automatically). Then locate the program, FETToy, and familiarize yourself with the program by reading the Description. The FETToy Matlab script can be downloaded from this site, or you can run FETToy simulations directly through your web browser. To run FETToy, select Execute FETToy, fill out the form, then View /Download FETToy Output Files to see the results.

All parameters used in FETToy are in MKS units except energy, which is in eV. In addition to device specification, material constants, temperature and bias information, FETToy needs three parameters:

1) The "Source Fermi Level," Ef, which determines the off current. Increasing Ef increases the off current and vice versa.

2) The "Gate Control Parameter," alphag, ($0 < \text{alphag} < 1$) which describes the control of gate electrode over the potential at the top of the barrier. Increasing this parameter decreases the subthreshold swing, S and vice versa. For alphag =1, there is complete gate control, as for a long channel MOSFET.

3) The "Drain Control Parameter," alphad, which describes the control of drain electrode over the potential at the top of the barrier. Increasing this parameter increases DIBL and vice versa.

FETToy2.0 is a collection of Matlab scripts that simulate MOSFETs with 2D channels, nanowire MOSFETS with 1D channels, or carbon nanotube MOSFETs (also with 1D channels). An earlier version (still available for downloading) treats MOSFET with or without a "floating boundary condition" in the source as discussed by Rahman et al. [9].

In addition to an output file summarizing the key results from the simulation, several plots are produced.

i) Id vs. Vgs at low and high Vds

ii) $\text{Log}_{10}(\text{Id})$ vs. Vgs at low and high drain bias

iii) Id vs. Vds with Vgs as a parameter

iv) Mobile charge, Q, vs. Vgs at low and high Vds

v) $\log_{10}(Q)$ vs. Vgs at low and high Vds

vi) Q, vs. Vds with Vgs as a parameter

vii) Quantum capacitance vs. Vgs at low and high drain bias

viii) Injection velocity vs. Vgs at high Vds

Three data files containing the current data, the self-consistent potential data and mobile charge data that can be used to reproduced the above plots.

To run FETToy, a good starting point is the following ***default parameters:***

Recommended Default Parameters for FETToy 2.0

Select Device Type

- (•) Single Gate Si MOSFET
- ( ) Double Gate Si MOSFET
- ( ) Si NanoWire FET
- ( ) Carbon Nanotube FET

Device Specifications

Gate Insulator Thickness (m):	1.5e-9
Gate Insulator Dielectric Constant:	3.9
Transport Effective Mass (Si Only):	0.19
NT / NW Diameter (m):	1.0e-9
Temperature (K):	300

Terminal Voltage

Number of Bias Points:	13
Voltage Range (V):	0 to 0.6

FETToy Model Parameters

Source Fermi Level, *Ef* (eV):	-0.32
Gate Control Parameter, αg:	0.88
Drain Control Parameter, αd:	0.035

Plot Format(s)

- [x] GIF (Graphic Interchange Format)
- [ ] PDF (Portable Document Format)
- [ ] PS (PostScript)

Output Folder:	fettoy
Output File:	output

5. Exercises

The series of self-paced exercises presented in this section will help familiarize you with operating FETToy and at the same time, illustrate some key concepts for ballistic nanotransistors.

For traditional MOSFET models, $I_D \propto C_{ox}$, so reducing the oxide thickness by a factor of two doubles the current. Let's see what happens for nanotransistors.

1) Explore the role of gate oxide thickness on the on-current of a ballistic MOSFET. For these calculations, you should use **1D electrostatics** and vary the oxide thickness from **10nm** to **0.01nm**. You should use the ***default*** values of the other parameters.

   i) Produce a plot of the on-current (the current for Vg = Vd = Vdd) vs. oxide thickness. Compare the computed results to the result expected from conventional MOSFET theory (Id ~ Cox). (***Plot the two curves on the same figure, and have them cross at tox = 10nm***).

   ii) Provide a physical explanation for the shape of your plot. The characteristic should change when the oxide thickness is smaller than a certain value. Can you give a simple equation to estimate that value? (HINT: It is the gate capacitance that matters. The oxide capacitance is in series with a semiconductor or "quantum" capacitance)

   iii) Explain how you specified the FETToy input parameters to achieve a 1D solution

You might think that a lighter effective mass would give a transistor higher current, because with a lighter mass, carriers will travel faster. This exercise will demonstrate that this is not always the case.

2) Explore the role of effective mass on the on-current of a ballistic MOSFET. For this calculation, you should also use **1D electrostatics** and vary the effective mass from $\mathbf{10m_0}$ to $\mathbf{0.01m_0}$. You should use the ***default*** values for the other parameters.

   i) Produce a plot of the on-current (the current for Vg = Vd = Vdd) vs. effective mass. You might expect the on-current to be proportional to the velocity (which is inversely proportional to the square root of the effective mass). Compare your plot against this expectation. (***Plot the two curves on the same figure, and have them cross at $m^*=10m_0$***).

   ii) Provide a physical explanation for the shape of your plot. That is, explain why the plot of I_D(on) vs. m^* has a maximum.

The temperature dependence of a MOSFET sheds light on its device physics. For a ballistic nanotransistor, we might expect the on-current to decrease at 77K, because it is limited by the thermal velocity. That is certainly true for the non-degenerate case (where $\propto_T \propto \sqrt{T}$), but what happens when the electrons are degenerate, as they typically are above threshold?

3) Explore the role of temperature on the on-current of a ballistic MOSFET. For this calculation, you should also use **1D electrostatics** and vary the temperature from **10K** to **700K**. You should use the ***default*** values for the other parameters.

   i) Produce a plot of the on-current (the current for Vg = Vd = Vdd) vs. *T*. You might expect the on-current to be proportional to the velocity (which is proportional to the square root of the temperature). Compare your plot against this expectation. (***Plot the two curves on the same figure, and have them cross at T = 700K***).

   ii) Provide a physical explanation for the shape of your plot.

Is any of this relevant? Let's see how close to the ballistic limit modern day MOSFETs operate.

4) Estimate how close to the ballistic limit present-day MOSFETs operate.

   i) Read the paper – C. C. Wu et al, "A 90-nm CMOS Device Technology with High-speed, General-purpose, and Low-leakage Transistors for System on Chip Applications", *IEDM Tech Digest*, p. 65-69, San Francisco, Dec.9-11, 2002. (Focus on the High-Speed (HS) devices)

   ii) Use FETToy to simulate a ballistic MOSFET with parameters similar to those of the Std-Vt HS MOSFET described in the above paper (see Table II). To account for quantum confinement, you will need to use an effective oxide thickness, **1.8nm** (the insulator relative dielectric constant is **3.9**). Set the voltage range to be from **0V** to **1V** by a step of **0.05V**. Then run FETToy, using the ***default*** values for all the other parameters ***EXCEPT*** **the source Fermi level, Ef, the gate control parameter, κ_g, and the drain control parameter, κ_d.** You will need to adjust the values of these **three parameters** to achieve *S,* DIBL and I_{off} similar (within ~5% error) to those of the experimental device listed in Table 1.

      After finishing the simulation:

      Read Ef, κ_g, κ_d, S, DIBL, I_{off} and I_{on} from the output of FETToy and complete Table 1. Compare the on current of the experimental device with the ballistic limit.

Table 1 Device Characteristics of the experimental and simulated MOSFETs

	Ef (eV)	κ_g	κ_d	S (mV/dec)	DIBL (mV/V)	I_{off} (μA/μm)	I_{on} (μA/μm)
Experiment	N/A	N/A	N/A	105	130	0.075	830
Simulation (Ballistic)							

Nanowire transistors are getting a lot of attention these days. They seem to operate more nearly as SB FETs than as MOSFETs, but it's interesting so see what might happen if nanowire MOSFETs can be realized. The first exercise below will get you calibrated on silicon nanowire MOSFETs.

5) Examine the *I-V* characteristics of a hypothetical silicon nanowire MOSFET. Assume D = 1nm and that the insulator is 2 nm of SiO_2 and that $V_{DD} = 0.5$V. Ef =-0.32 eV.

   i) Compute I_D vs. V_{DS} at T = 300K and compare the low-V_{DS} drain conductance, G_D with the quantum conductance, $4e^2/h$.

   ii) Repeat problem i) but at T = 77K. The channel conductance vs. Vgs is strikingly different than a conventional MOSFET. Explain how.

   iii) The on-current can be written as $I_D = C_G\langle -(0)\rangle(V_{GS} - V_T)$. Deduce C_G, $\langle \upsilon(0)\rangle$, and V_T

Both silicon and carbon nanotube nanowire FETs are currently being explored. Let's compare the performance of these two different materials.

6) Compare the performance of a silicon nanowire MOSFET to a carbon nanotube MOSFET as follows:

   i) Simulate a Si nanowire MOSFET with D = 1nm, tins = 1.5nm, Vdd = 0.5V, and Ef = -0.3V. Assume SiO2 as the gate insulator.

   ii) Simulate a CNT MOSFET with D = 1nm, tins = 1.5 nm, Vdd = 0.5V, and Ef = -0.3V. Assume SiO2 as the gate insulator.

   ii) Compare the performance of the two nanowire transistors and explain what the key differences are and why they occur.

One of the potential advantages of carbon nanotubes is that they have no dangling bonds, so it should be easy to deposit high-k gate dielectrics on them. In the next exercise, you will examine carbon nanotube FETs with high-k gate dielectrics.

7) Compare the performance of a D = 1 nm carbon nanotube MOSFET with $\kappa = 3.9$ ($Si0_2$), $\kappa = 15$ (HfO_2) and $\kappa = 25$ (ZrO) and with $\kappa = 80$ (salt water).

   i) Plot Id(on) vs. κ. Explain why the benefits of high-κ gate dielectrics diminish at high κ.

It is possible for ballistic nanowire MOSFETs to operate in a regime where conventional MOSFET theory breaks down. For example, nanotubes have been gated in salt water (k = 80). In this case, the insulator capacitance is much higher that the semiconductor (or quantum capacitance), so that the gate capacitance (the series combination of the two) is simply the quantum capacitance of the nanotube. How does this affect a carbon nanotube MOSFET?

8) Explore the behavior of a carbon nanotube MOSFET in the quantum capacitance limit.

   i) Simulate a CNT MOSFET with D = 1nm, tins = 1.5nm, and k = 80. Set Ef = -0.3V and assume Vdd = 0.5V.

   ii) Compare the channel conductance, $\partial I_D / \partial V_{DS}\big|_{V_{GS}}$ at low drain bias to the transconductance, $\partial I_D / \partial V_{DS}\big|_{V_{GS}}$ at high drain bias. In the quantum capacitance limit, the two are related. Explain why.

Are nanowire MOSFETs inherently superior to conventional MOSFETs with 2D channels?

9) Compare the performance of a hypothetical ballistic Si nanowire MOSFET to that of a conventional ballistic MOSFET. Assume tins = 1 nm of SiO_2 in both cases and Vdd = 0.5V. For the nanowire, assume D = 1nm. Note: it will take some thought to perform a valid comparison.

6. *Quiz*

After performing these exercises and reading the references, you should develop a thorough understanding of ballistic nanotransistors. Test your understanding by answering the following questions.

1) Explain why the on current approaches a finite limit as the gate insulator thickness approaches zero.

2) Explain why the on current of a ballistic MOSFET shows a maximum as the effective mass increases from a very small value to a large value.

3) Explain why the on current of a ballistic MOSFET approaches a limit as the dielectric constant of the gate insulator approaches infinity.

4) How close to the ballistic limit does a state of the art MOSFET operate?

5) If you were measuring a nanoswire MOSFET, how would you know that is was operating as a quantum wire (i.e. with a 1D channel)?

6) Why is the quantum capacitance more important for a nanowire transistor than for a conventional MOSFET?

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