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ICTP 40th Anniversary

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SPRING COLLEGE ON SCIENCE AT THE NANOSCALE
(24 May - 11 June 2004)

CMOS for Scientists

M. LUNDSTROM
School of Electrical & Computer Engineering, Purdue University
West Lafayette, IN, USA

These are preliminary lecture notes, intended only for distribution to participants.

Spring College on Science at the Nanoscale - Trieste, Italy, June 2004

CMOS for Scientists

Mark Lundstrom
Purdue University
Network for Computational Nanotechnology
West Lafayette, IN USA

1) Introduction
2) CMOS Tutorial
3) CMOS Today
4) CMOS Limits
5) Conclusions

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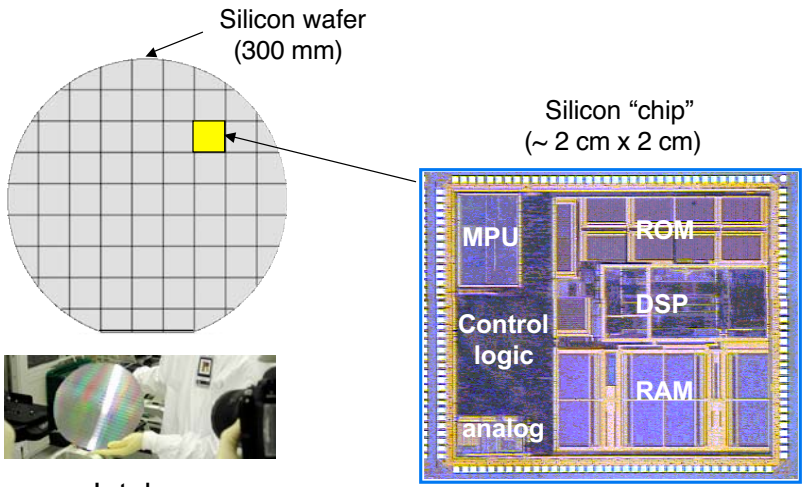
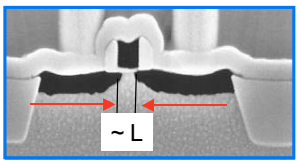
1. Introduction: microelectronics



Intel

TI cell phone chip

1. Introduction: transistors



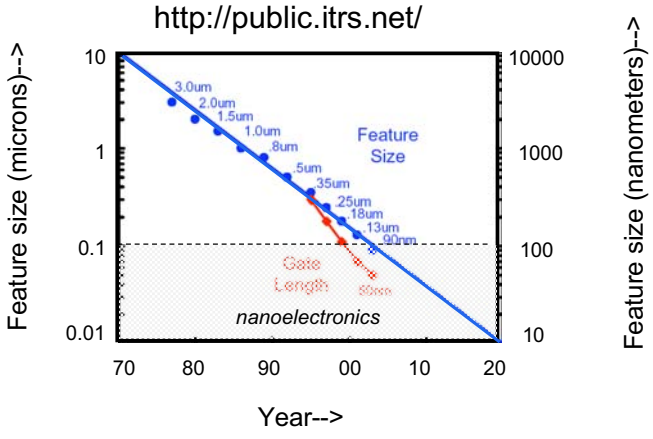
Each technology generation: **(scaling)**

$$L \rightarrow L/\sqrt{2} \qquad A \rightarrow A/2$$

Number of transistors per chip doubles **(Moore's Law)**

1. Introduction: Moore's Law and the ITRS

http://public.itrs.net/



L = 6 nm (IBM, 2002)
L = 5 nm (NEC, 2003)

1. Introduction

The promise of (bottom-up) nanoelectronics…..

- *understanding devices at the molecular scale*
- *new tools for metrology*
- *new materials*
- *unit processes for directed self-assembly*
- *new devices for new applications*
- *new architectures for ultra-dense systems*
- ***terascale electronics***

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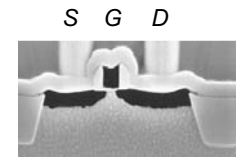
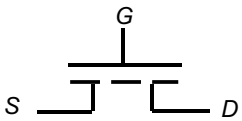
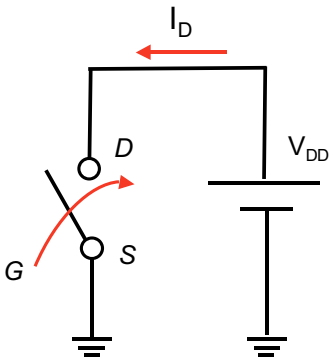
2. CMOS Tutorial: MOSFETs



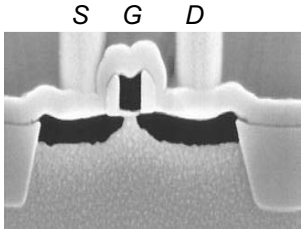




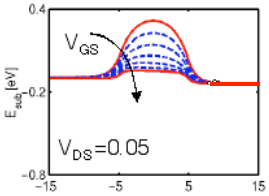
$V_G > V_T$: I_D ---> ∞ "on-current"

$V_G < V_T$: $I_D = 0$ "off-current"

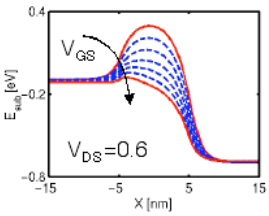
2. CMOS Tutorial: MOSFETs



electron energy vs. position



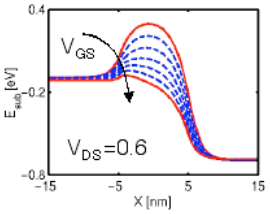
$V_D \approx 0V$

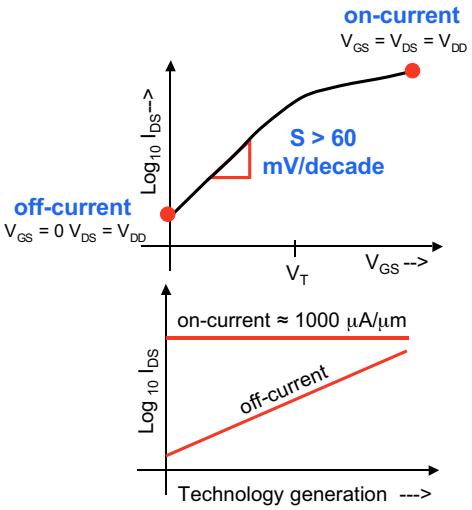


$V_D = V_{DD}$

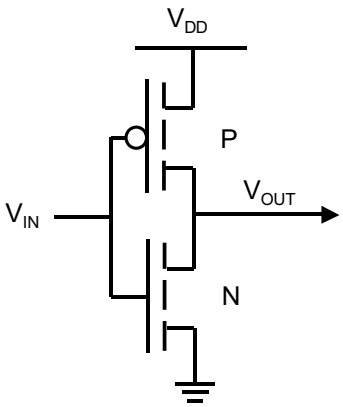
2. CMOS Tutorial: MOSFETs

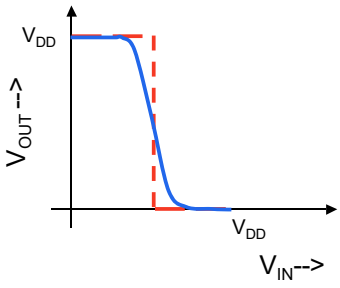
electron energy vs. position



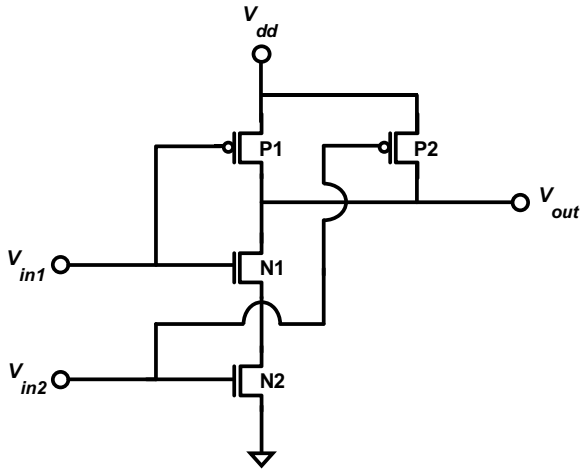


2. CMOS Tutorial: circuits

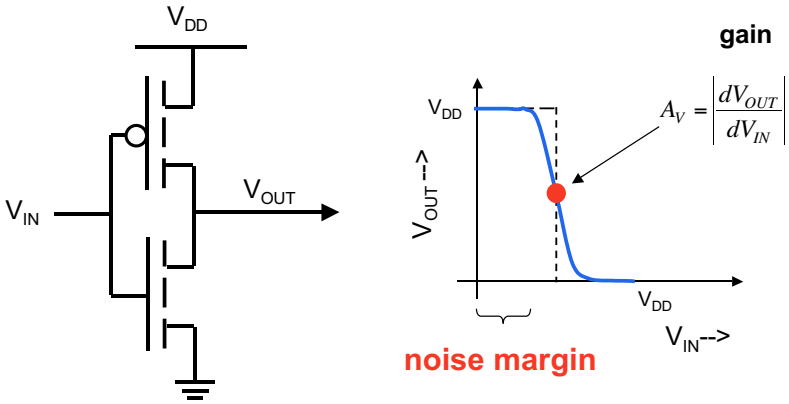




2. CMOS Tutorial: Two input NAND gate

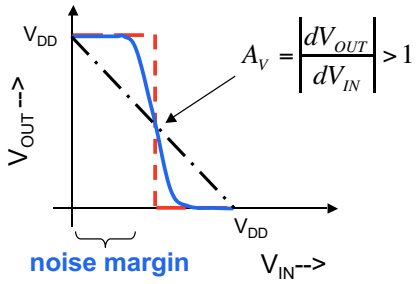


2. CMOS Tutorial: circuits



2. CMOS Tutorial: gain

gain restores signal levels



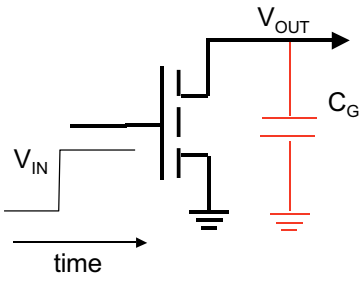
$$V_{DD}\big|_{\min} = 2\ln(2)\left(k_B T/q\right)$$

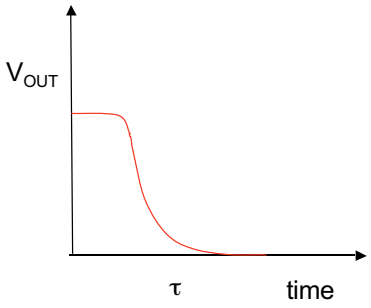
$$E_S = \frac{1}{2}CV_{DD}^2 = Q\frac{V_{DD}}{2}$$

$$E_S\big|_{\min} = k_B T\ln(2) \approx 3\times10^{-21}\,J$$

90 nm CMOS technology operates at ~ 35,000 $k_B T$ ln(2)

2. CMOS Technology: device speed

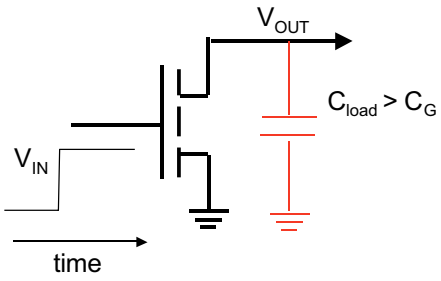


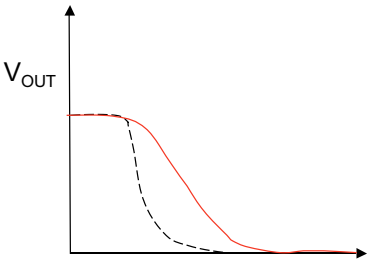


$$\tau = \frac{C_G V_{DD}}{I_D(on)} \approx \frac{L}{\upsilon} \approx 1\,\text{ps}$$

(90 nm technology node)

2. CMOS Tutorial: circuit speed

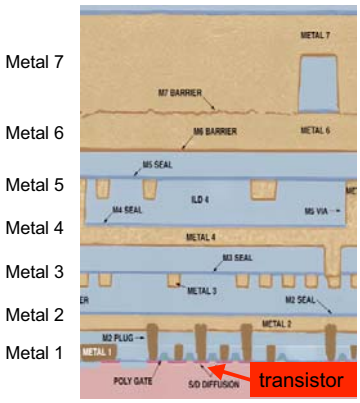




$$\tau = \frac{C_{Load} V_{DD}}{I_D(on)} \approx 10 \text{ ps}$$

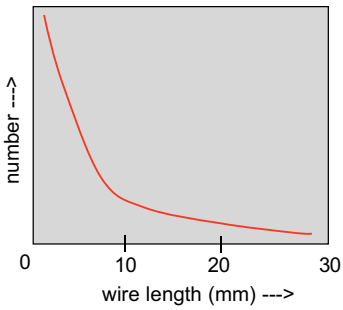
(90 nm technology node)

2. CMOS Tutorial: system speed



Silicon wafer

Rent's Rule



$$\tau_{global} \approx r_{\text{int}} c_{\text{int}} \sim \ell^2 \approx 100 \text{ ps}$$

(90 nm technology node)

2. CMOS Tutorial: system speed

until ~1990:
device delay > interconnect delay

Today (90nm technology):
device delay: ~ 1ps
1 mm interconnect delay: ~ 6 ps

2015 (22 nm technology):
device delay: ~0.1ps
1 mm interconnect: ~30ps

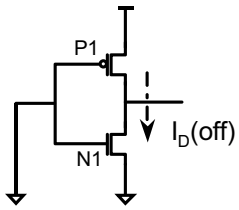
J. Meindl, "Beyond Moore's law: the interconnect era, " *Computing in Science and Engineering*, 2003

2. CMOS Tutorial: system speed

$$\tau = \frac{C_{Load} V_{DD}}{I_D(on)}$$

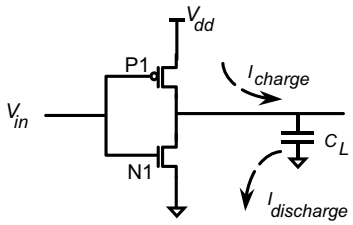
speed is controlled by the DC "on-current"

2. CMOS Tutorial: system power



1) standby power:

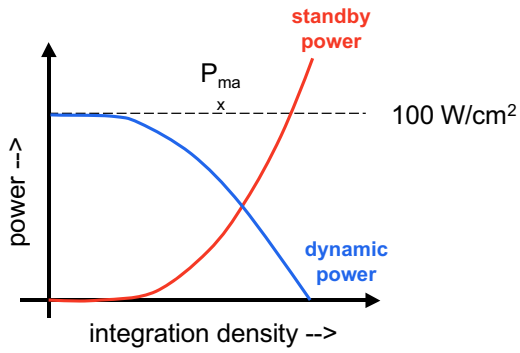
$$P_{off} = N_G I_D(off) V_{DD}$$



2) dynamic power:

$$P_{on} = \alpha f C_{TOT} V_{DD}^2$$

2. CMOS Tutorial: system power



there is an optimum device size!

2. CMOS Tutorial: device requirements for digital systems

- high on-current
- low off-current
- gain
- acceptable power
- well-controlled parameters

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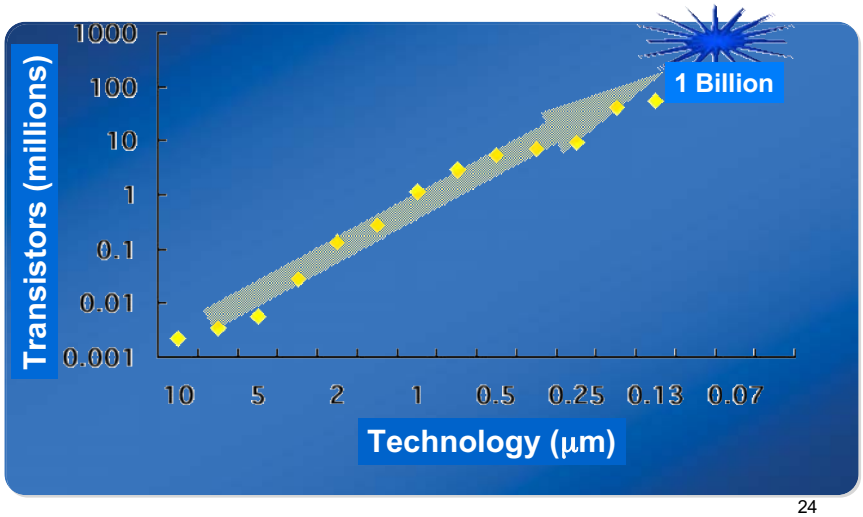
3. CMOS Today

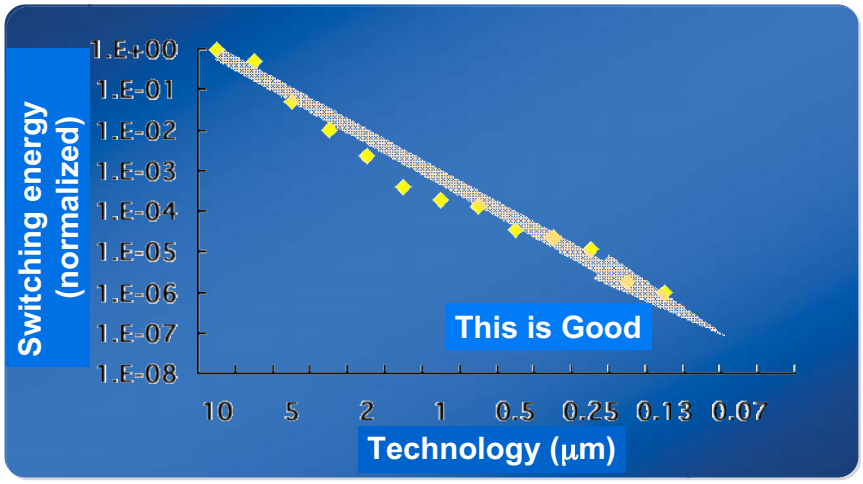
the following slides were provided courtesy of

Dr. Shekhar Borkar
Circuit Research, Intel Labs
Intel Corp.

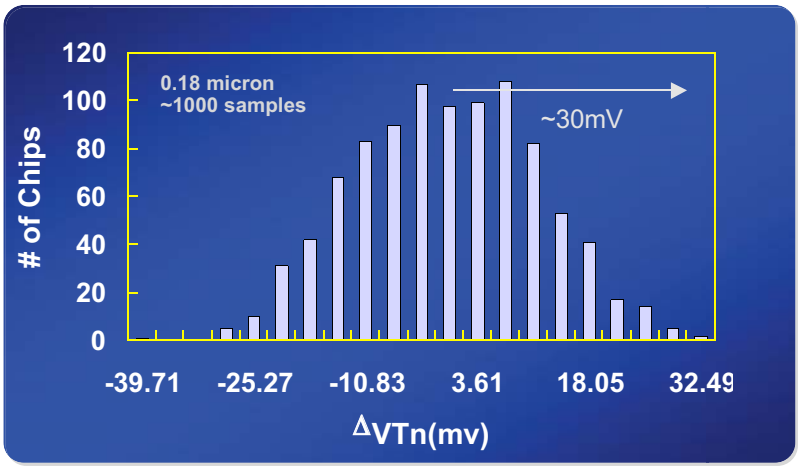
3. CMOS Today: technology scaling



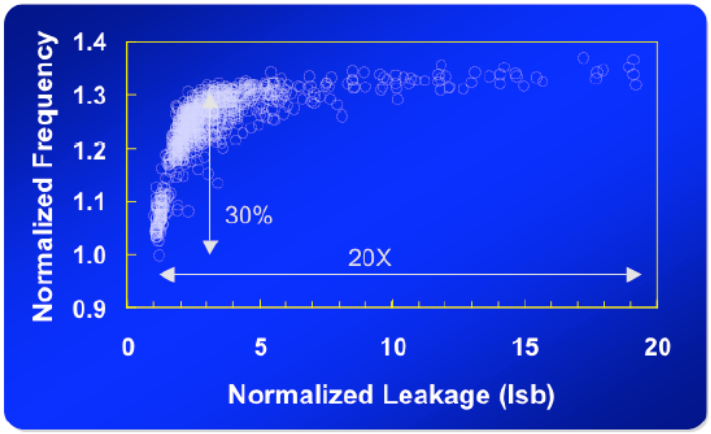
3. CMOS Today: technology scaling



3. CMOS Today: device variations

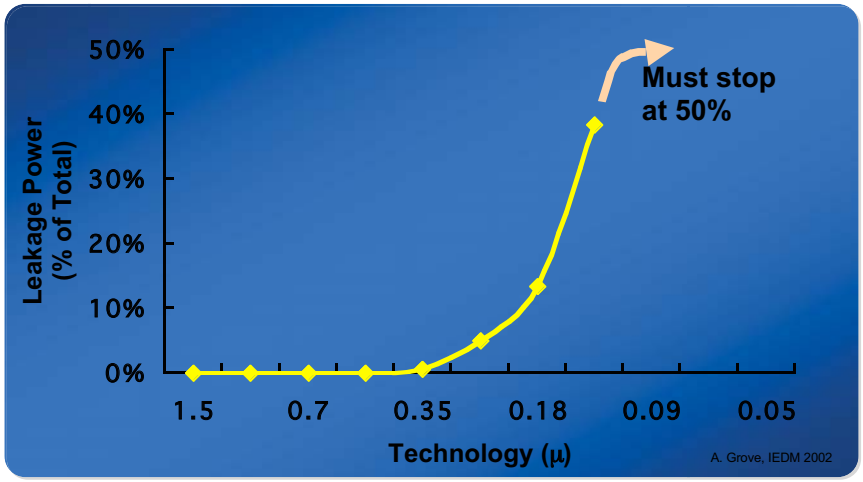


3. CMOS Today: device variations



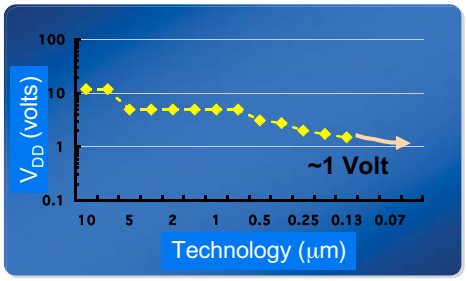
1. 20X variation in SD leakage
2. 30% variation in Frequency

3. CMOS Today: leakage power

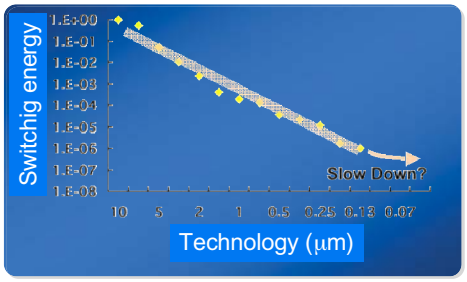


Leakage power limits Vt scaling

3. CMOS Today: technology scaling



- T_{ox} scaling will slow down
- V_{DD} scaling will slow down
- V_T scaling will slow down



- Approaching constant V_{DD} scaling
- **Energy/logic op will not scale**

3. CMOS Today: technology scaling

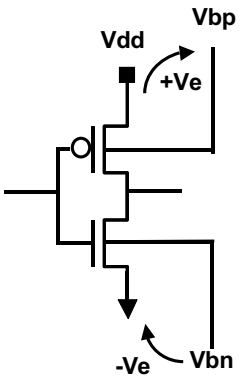
- >1B Transistor integration capacity will be available
- Could be unusable due to power
- Logic Transistor growth will slow down
- Transistor performance will be limited

Solutions:

- Low power design techniques
- Improve design efficiency
- Increased performance by even higher integration (of slower transistors)

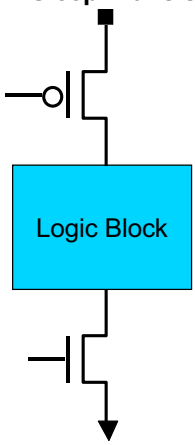
3. CMOS Today: solutions

Body Bias



2-10X reduction

Sleep Transistor



2-1000X reduction

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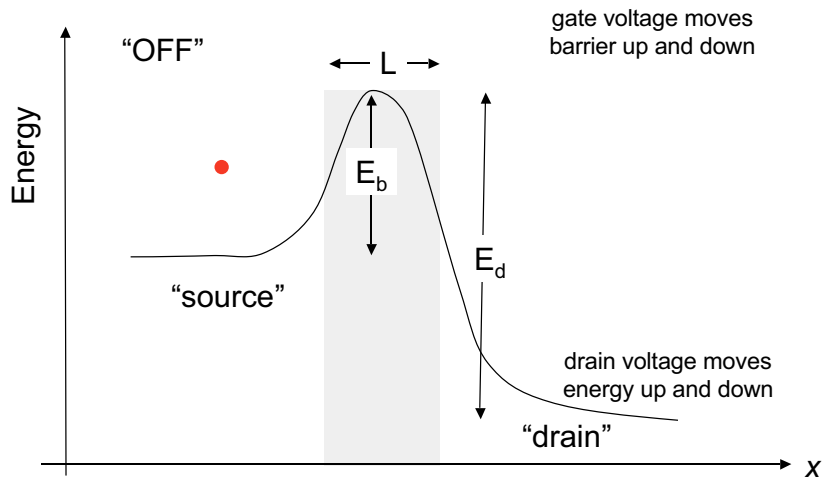
4. CMOS Limits

1) minimum energy dissipation per logic transition, E_{min} (J)
2) minimum size, L / maximum device density, n_{max} (cm^{-2})
3) minimum delay, t_{min} (sec)
4) power density, P (W/cm^2)
5) power-limited device density
6) CMOS vs. the ultimate switch

4. CMOS Limits



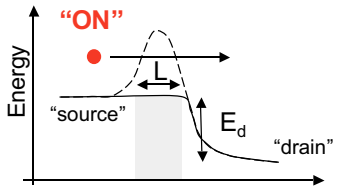
see Zhirnov, Cavin, Hutchby, and Bourianoff, *Proc. IEEE*, Special Issue on Nanoelectronics and Nanoscale Processing, Nov. 2003.

4. CMOS Limits: minimum switching energy

To distinguish 'off' from on, the electron must have less than a 50:50 chance of moving from the source to drain. If 'on', electrons from the drain must have less than a 50:50 chance of moving from drain to source.

$$e^{-E_d / k_B T} < \frac{1}{2}$$

---> $E_S > E_{\min} = \ln(2)\, k_B T$

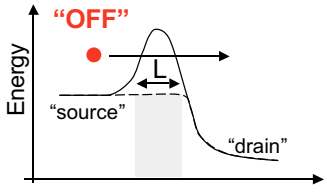


(minimum energy dissipation per logic transition)

4. CMOS Limits: minimum device size

To distinguish 'off' from on, the probability that an electron tunnels through the barrier must be less than a 50:50.

$$P(\mathrm{WKB}) = \exp\left(-\frac{2\sqrt{2mE}}{\hbar} L\right) < \frac{1}{2}$$



$$L > \frac{\ln(2)}{2} \frac{\hbar}{\sqrt{2mE}} \qquad E = k_B T = \frac{E_{\min}}{\ln(2)}$$

--->

$$L_{\min} \approx \frac{\hbar}{\sqrt{2mE_{\min}}} = 1.5\,\mathrm{nm}(300\mathrm{K})$$

$$\Delta p \Delta x = \hbar$$

4. CMOS Limits: minimum device size

Note also that the size of a device, *S*, must be larger than the size of its minimum element, *L*. (For a MOSFET, $S \sim 10\text{-}15L$.)

4. CMOS Limits: maximum device density

$$n_{max} \approx \frac{1}{L_{min}^2} = 4.7 \times 10^{13}\ \text{cm}^{-2}$$

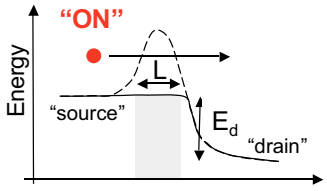
We will show later that device density is limited by the maximum power density that can be dissipated - not by device size.

(This number would be ~ 100X smaller if we account for the fact that a device is larger than its minimum critical feature.)

4. CMOS Limits: maximum speed

The minimum device transit time, t_{min}, sets the maximum speed.

$$t_s \approx \frac{L}{\upsilon} \qquad t_{\min} \approx \frac{L_{\min}}{\upsilon} = \frac{L_{\min}}{\sqrt{2E/m}}$$



Use

$$L_{\min} \approx \frac{\hbar}{\sqrt{2mE}} \qquad E = k_B T = \frac{E_{\min}}{\ln(2)}$$

--->

$$t_{\min} \approx \frac{\hbar}{E_{\min}} = 0.04 \text{ ps} \quad (300\text{K})$$

$$\Delta E \Delta t = \hbar$$

4. CMOS Limits: power dissipation

$$P = \frac{\alpha \, n_{\max} E_S}{t_S}$$

switching activity factor, α ($\alpha < 1$)

$$P_{\max} = \frac{n_{\max} E_{\min}}{t_{\min}} = 3.7 \times 10^6 \text{ W/cm}^2$$

surface of the sun: 6×10^3 W/cm^2

forced water cooling < 800 W/cm^2

2016 ITRS < 100 W/cm^2 (no known solution)

4. CMOS Limits: power-limited density

maximum power dissipation per unit area limits density
- not our ability to make devices small.

$$\hat{n}_{\max} = \frac{\hat{P}_{\max} t_{\min}}{\alpha E_{\min}}$$

for $\hat{P}_{\max} = 100\,\mathrm{W/cm^2}$ and $\alpha = 1$

$$\hat{n}_{\max} \sim 1.5 \times 10^9 \quad \text{devices/cm}^2$$

------> **CMOS technology will produce more devices on a chip than can be used (at once)**

4. CMOS Limits: vs. 2016 CMOS

parameter	2016 ITRS	Limit	2016 ITRS /Limit
τ (fs)	150	40	4
E_s (eV)	12.5 eV	0.017 eV	735
L (nm)	9 nm	1.5 nm	6
n_S (cm^{-2})	2.9 x 10^9	4.7 x 10^{13}	1/6500
$\hat{n}_S$ (cm^{-2})		1.5 x 10^9	2

(numbers from 2002 edition of ITRS)

CMOS at the end of the ITRS will operate close to fundamental limits - except for E_S

4. CMOS Limits: vs. 2016 CMOS

Operation at $k_B T \ln(2)$ is not possible because:

1) Assumes $A_V = 1$ (no noise margin)

2) Assumes C_{LOAD} is charged with 1 electron (no speed)

3) Assumes no device - device variations

We may be near the end of E_S scaling at 35,000 X $k_B T \ln(2)$

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5. Conclusions

1) CMOS devices face serious challenges
(leakage, variations, interconnects, …)
molecular electronics does not address these issues

2) Power dissipation limits device density
not our ability to make devices small

3) CMOS will operate near ultimate limits
no transistor can be fundamentally better

4) CMOS will provide more devices than can be used
design, not technology will drive progress

5. Conclusions

The promise of (bottom-up) nanoelectronics…..

- *understanding devices at the molecular scale*
- *new tools for metrology*
- *new materials*
- *unit processes for directed self-assembly*
- *new devices for new applications*
- *new architectures for ultra-dense systems*
- *terascale electronics*