Outline

- Introduction – *"Is there a limit?"*
- Transistors – *"CMOS building blocks"*
- Parasitics I – *"The [un]desirables"*
- Parasitics II – *"Building a full MOS model"*
- The CMOS inverter – *"A masterpiece"*
- Technology scaling – *"Smaller, Faster and Cooler"*
- Technology – *"Building an inverter"*
- Gates I – *"Just like LEGO"*
- The pass gate – *"An useful complement"*
- Gates II – "A portfolio"
- Sequential circuits – *"Time also counts!"*
- DLLs and PLLs – " A brief introduction"
- Storage elements – *"A bit in memory"*

"Building a full MOS model

- MOS process parasitics
- pn-Junction diodes
- Depletion capacitance
- Source/drain resistance
- MOS Model
- Parasitic bipolars
- Device hazards:
  - Latchup
  - Electrostatic discharge

MOS Parasitics

In a CMOS process the devices are:

- PMOS FETs
- NMOS FETs

+ unwanted (but ubiquitous):

- pn-Junction diodes
- parasitic capacitance
- parasitic resistance

and

- parasitic bipolars
- *parasitic inductance*

Parasitics or useful?

- Resistors
- Capacitors
- Inductors
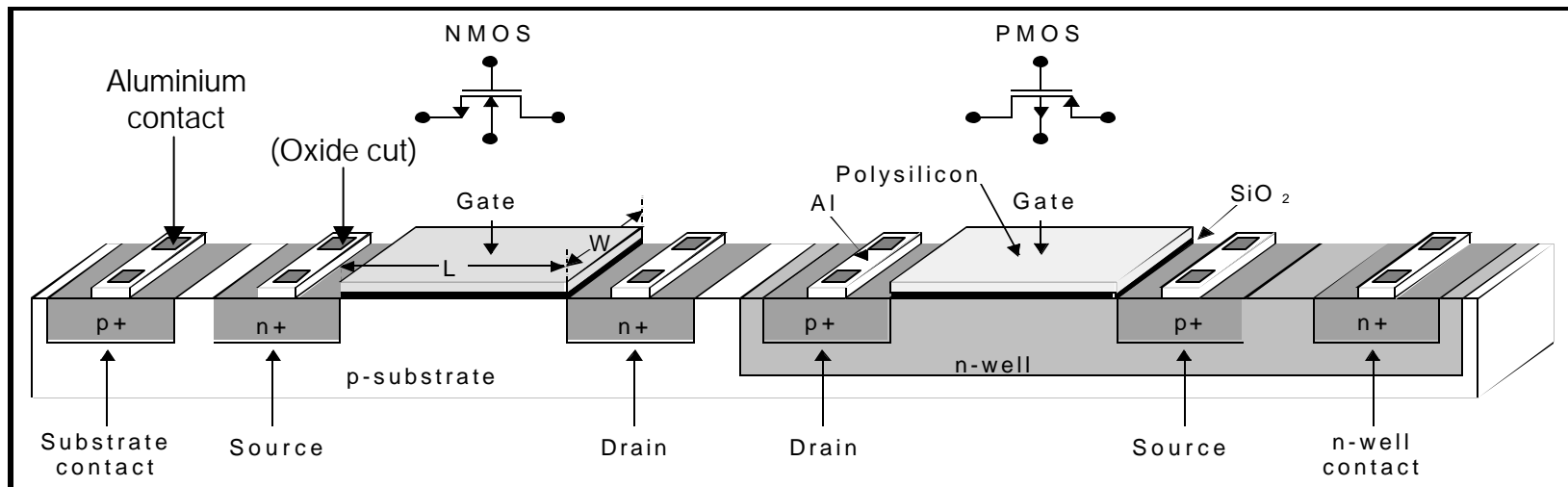- Diodes
- Bipolar transistors

Are useful circuit elements for analogue circuit design. Some technologies offer the possibility of manufacture such devices under controlled conditions.

pn-Junction diodes

- pn – Junction diodes:
  - Provide isolation between devices (if reversed biased)
  - Can be used to implement:
    - band-gap circuits (if forward biased)
    - variable capacitors
    - clamping devices
    - level shifting
  - Are extremely useful as Electro Static Discharge (ESD) protection devices.

CMOS devices

- ## Remember:
  - Every source and drain creates a pn-junction
  - pn-junctions must be reversed biased to provide isolation between devices
  - Reversed biased pn-junctions display parasitic capacitance

pn-Junctions diodes

- Any pn-junction in the IC forms a diode
- Majority carriers diffuse from regions of high to regions of low concentration
- The electric field of the depletion region counteracts diffusion
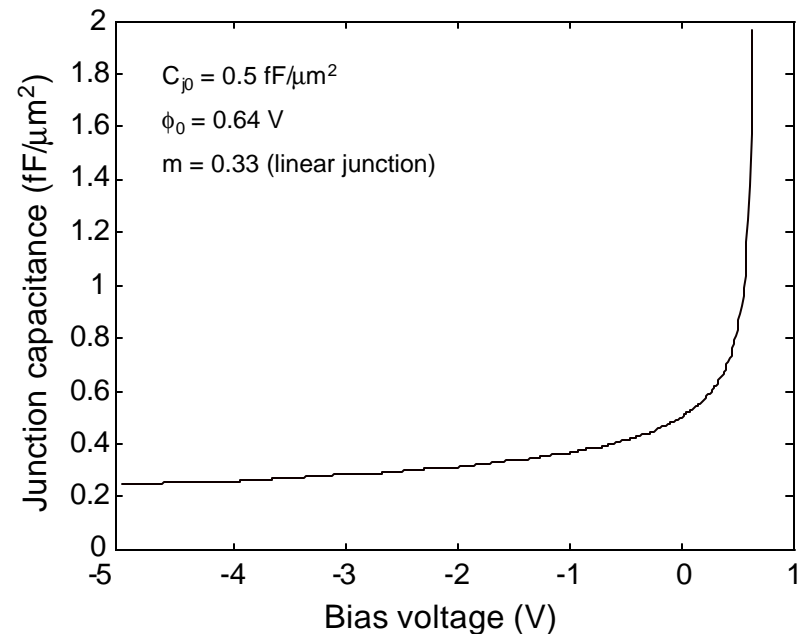- In equilibrium there is no net flow of carriers in the diode
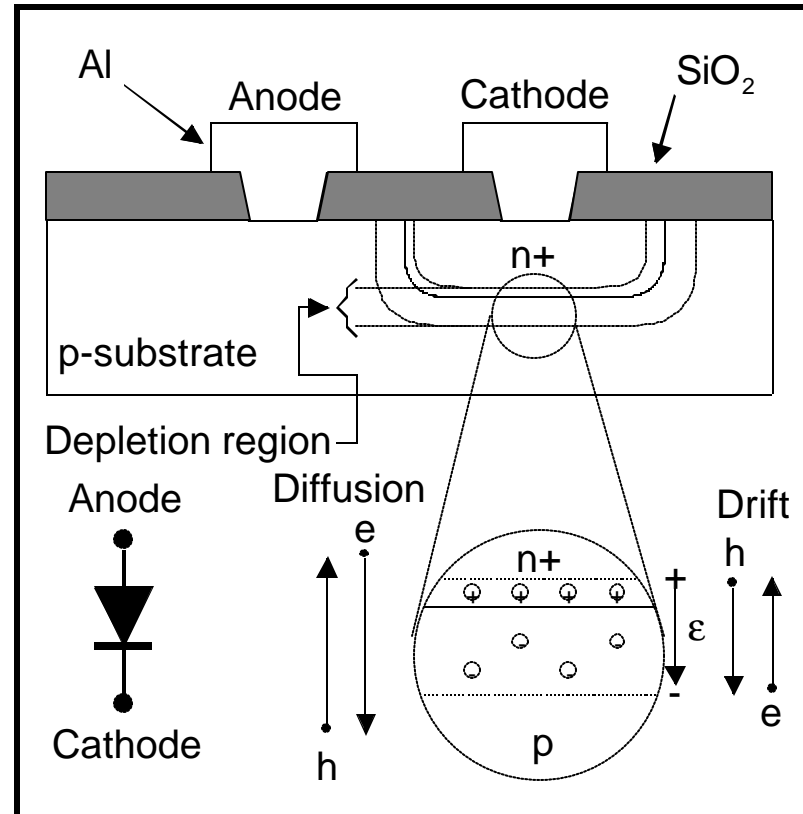
Depletion capacitance

- The depletion, the n- and the p-type regions form a capacitor

- This capacitor is bias dependent:

$$C_j = \frac{C_{j0}}{\left(1 - \dfrac{V}{f_0}\right)^m}$$

- Simplification: for V<0

$$C_j = k \cdot C_{j0}$$

$C_{j0} = 0.5\ \text{fF}/\mu m^2$

$\phi_0 = 0.64\ V$

$m = 0.33\ \text{(linear junction)}$

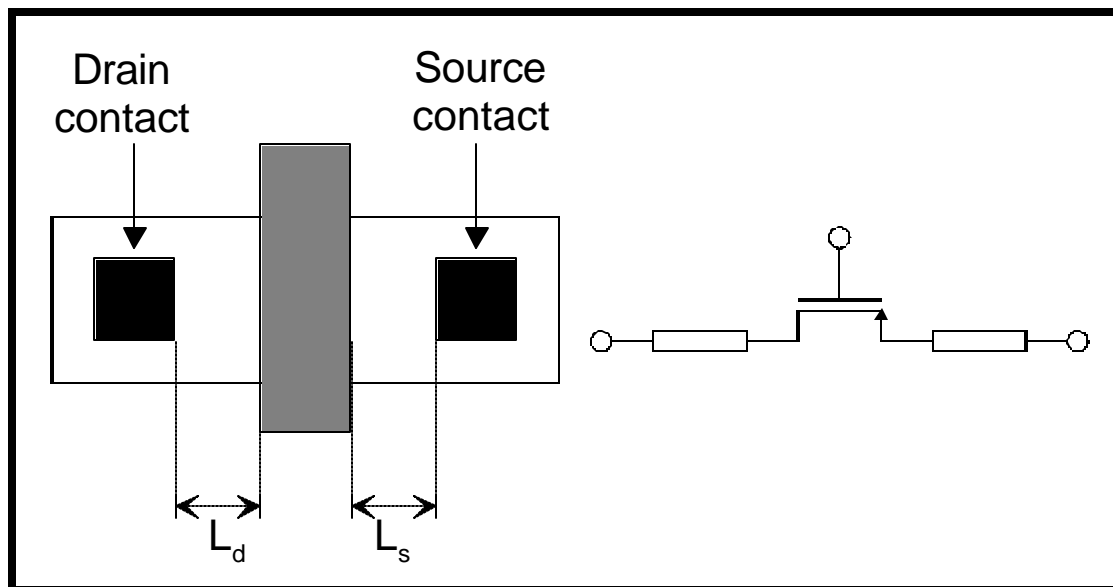Junction capacitance $(\text{fF}/\mu m^2)$

Bias voltage (V)

Source/drain resistance

- Scaled down devices $\Rightarrow$ higher source/drain resistance:

$$R_{s,d} = \frac{L_{s,d}}{W} \cdot R_{sq} + R_c$$

- In sub-μ processes *silicidation* is used to reduce the source, drain and gate parasitic resistance
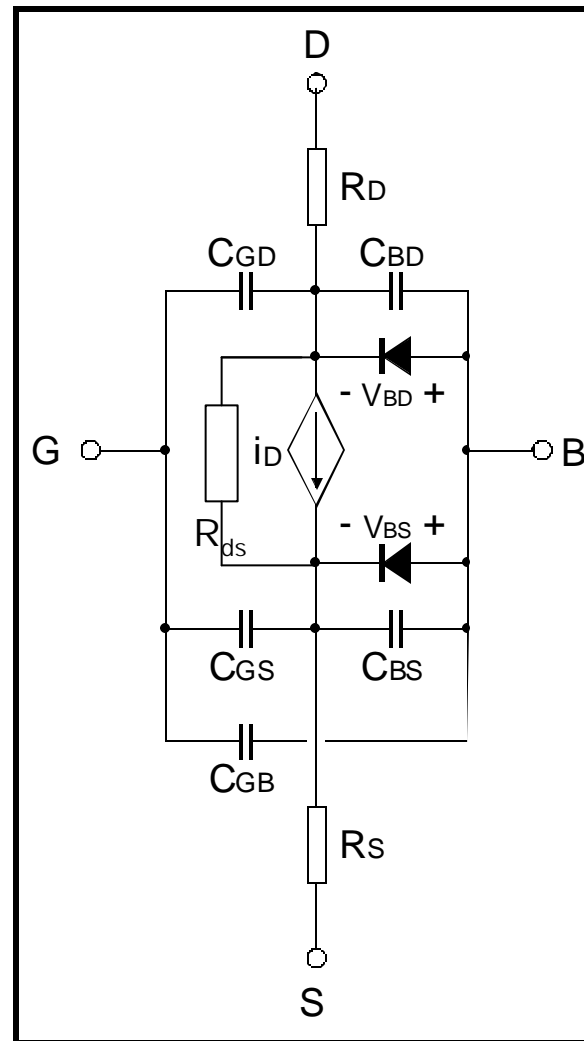

Drain contact

Source contact

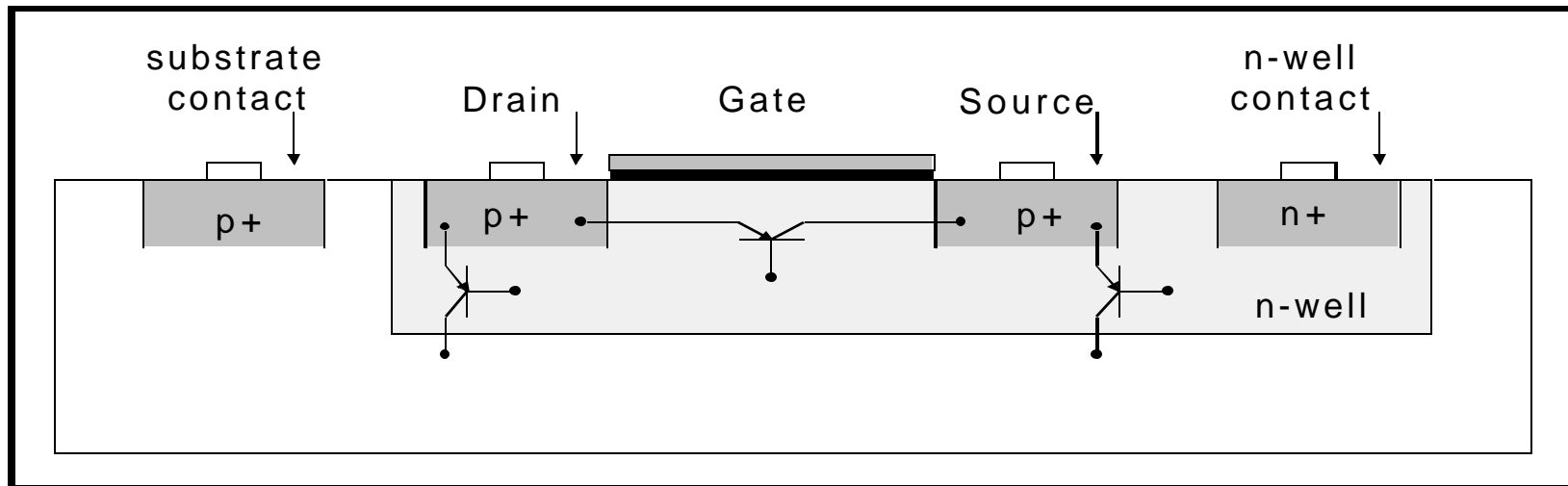L_d

L_s

0.24 μm process

R (P+) = 4 Ω/sq
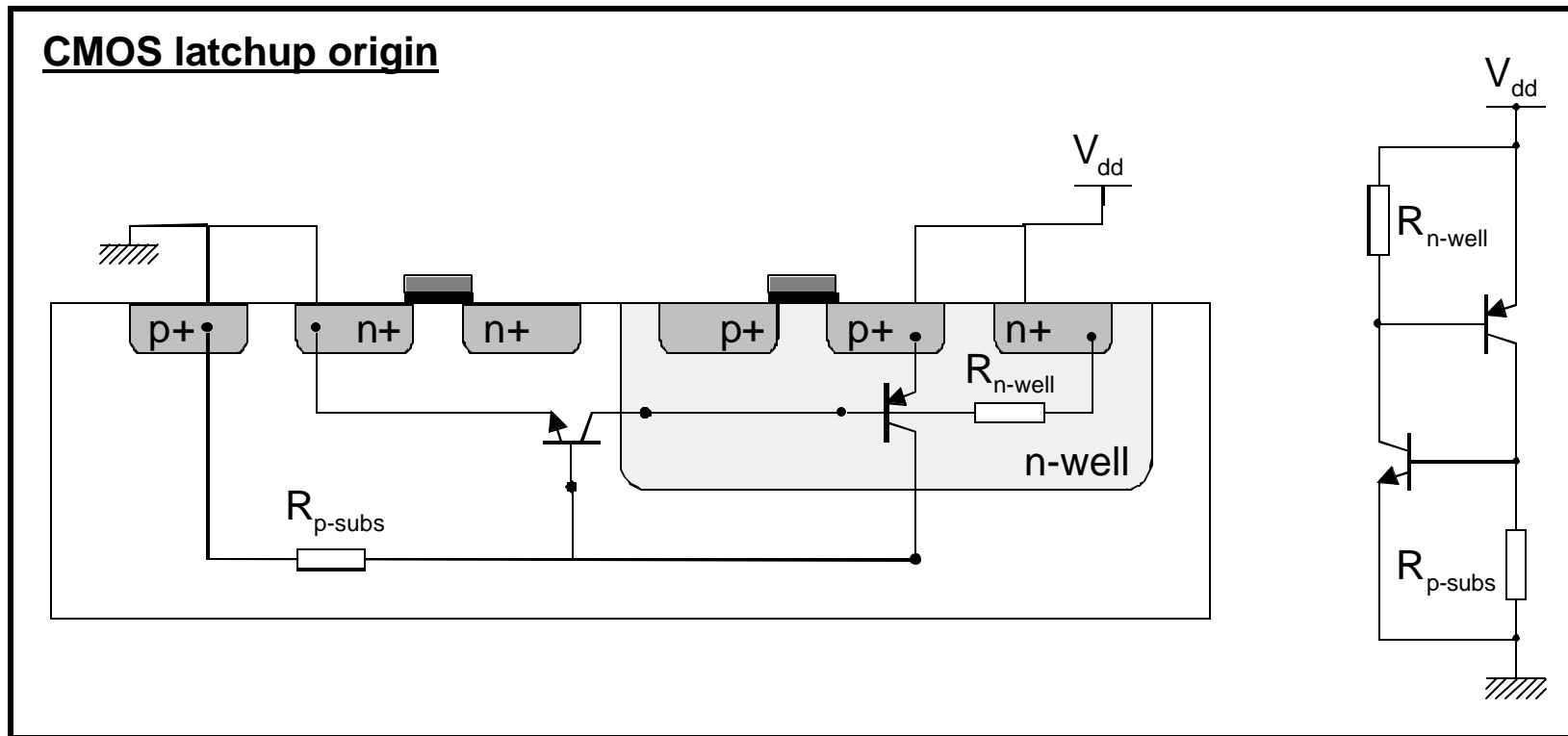R (N-) = 4 Ω/sq

MOSFET model

CMOS parasitic bipolar

- Every p-n-p or n-p-n regions form parasitic bipolar transistors.

- In standard MOS circuits these devices must be turned off.

- For some applications (like bandgap circuits) these devices can be used. But, better know what you are doing…

CMOS device hazards

CMOS latchup origin

CMOS device hazards

- ## Sources of latchup:

  - Electrical disturbance

  - Transient on power and ground buses

  - Improper power sequencing

  - Radiation

  - ESD

- ## How to avoid it:

  - Technological methods (beta reduction, substrate resistance reduction, trench isolation)

  - Layout rules:

    - Spacing rules
    - Contact distribution
    - Guard rings

CMOS device hazards

ESD protection