

Outline

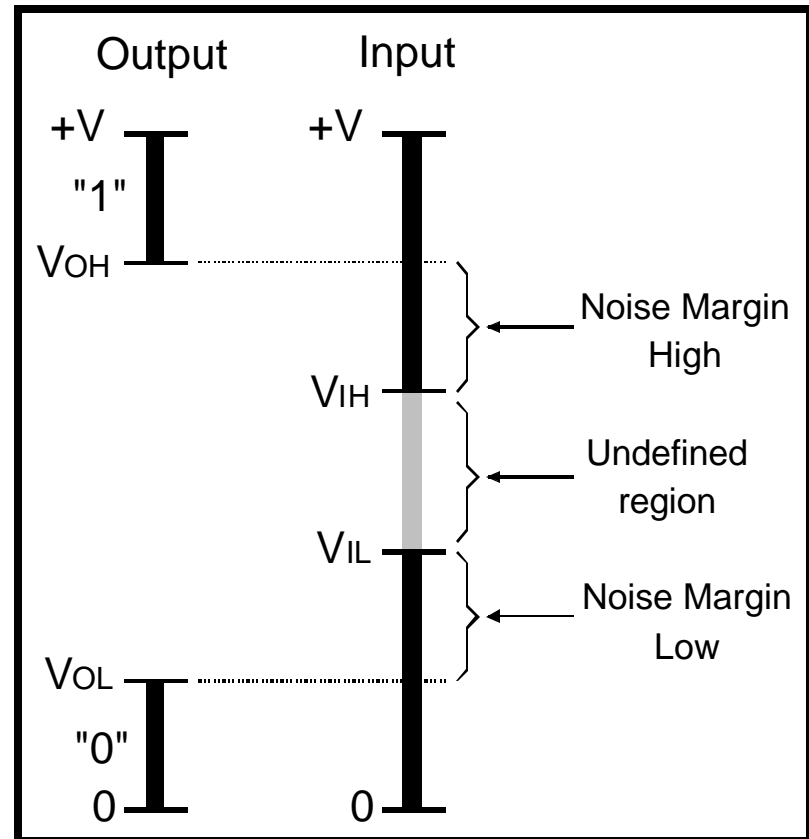
- Introduction – *“Is there a limit?”*
- Transistors – *“CMOS building blocks”*
- Parasitics I – *“The [un]desirables”*
- Parasitics II – *“Building a full MOS model”*
- **The CMOS inverter – *“A masterpiece”***
- Technology scaling – *“Smaller, Faster and Cooler”*
- Technology – *“Building an inverter”*
- Gates I – *“Just like LEGO”*
- The pass gate – *“An useful complement”*
- Gates II – *“A portfolio”*
- Sequential circuits – *“Time also counts!”*
- DLLs and PLLs – *“A brief introduction”*
- Storage elements – *“A bit in memory”*

“A masterpiece”

- Logic levels
- MOST – a simple switch
- The CMOS inverter:
 - DC operation
 - Dynamic operation
 - Propagation delay
 - Power consumption
 - Layout

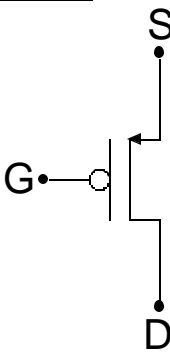
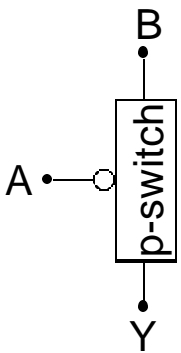
CMOS logic: “0” and “1”

- Logic circuits process Boolean variables
- Logic values are associated with voltage levels:
 - $V_{IN} > V_{IH} \Rightarrow \text{“1”}$
 - $V_{IN} < V_{IL} \Rightarrow \text{“0”}$
- Noise margin:
 - $NM_H = V_{OH} - V_{IH}$
 - $NM_L = V_{IL} - V_{OL}$



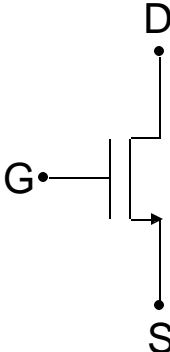
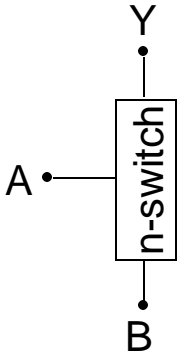
The MOST - a simple switch

p-switch

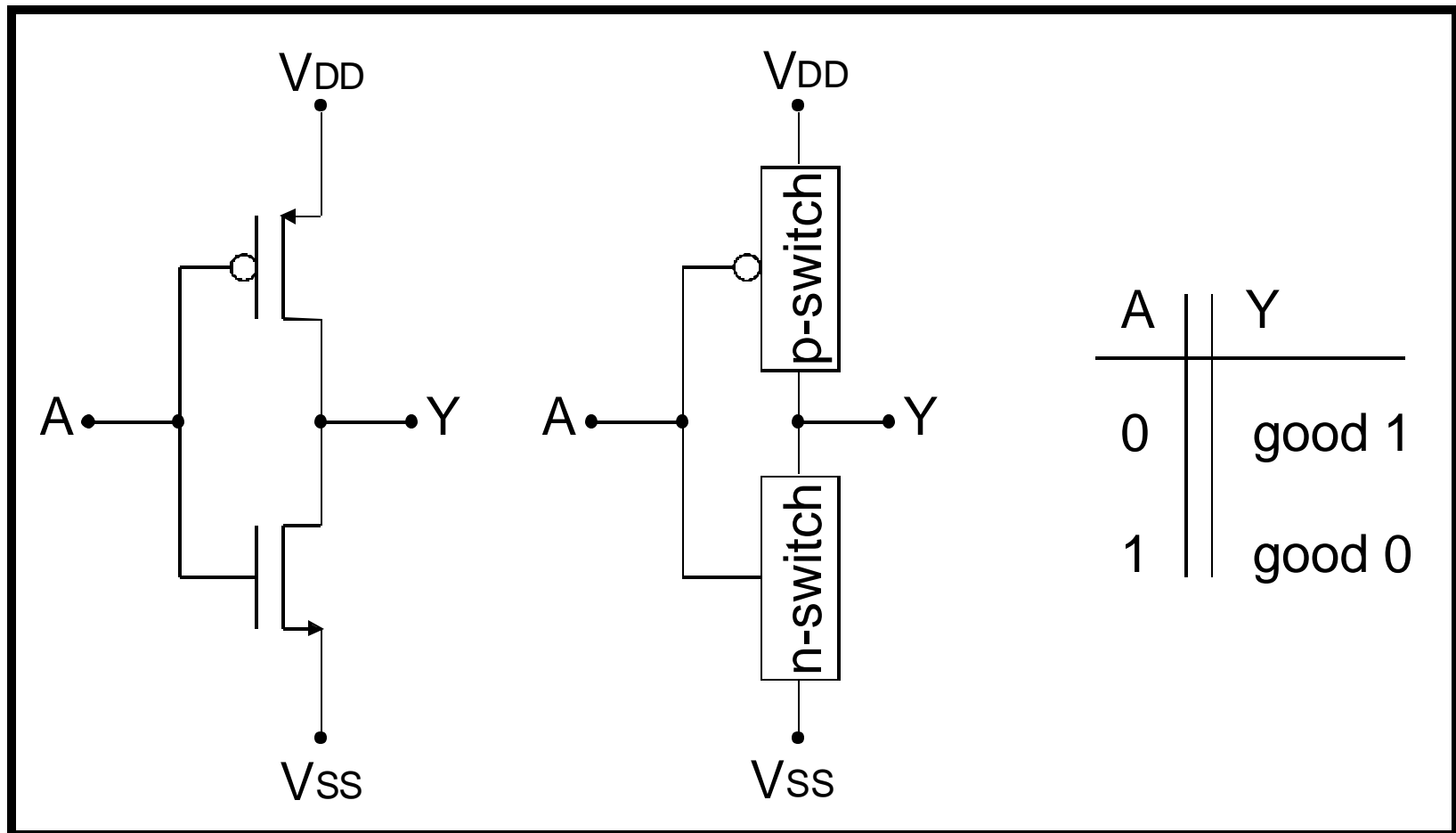
A	B	Y	
0	0	bad 0	(source follower)
0	1	good 1	
1	0	?	(high Z)
1	1	?	(high Z)

n-switch

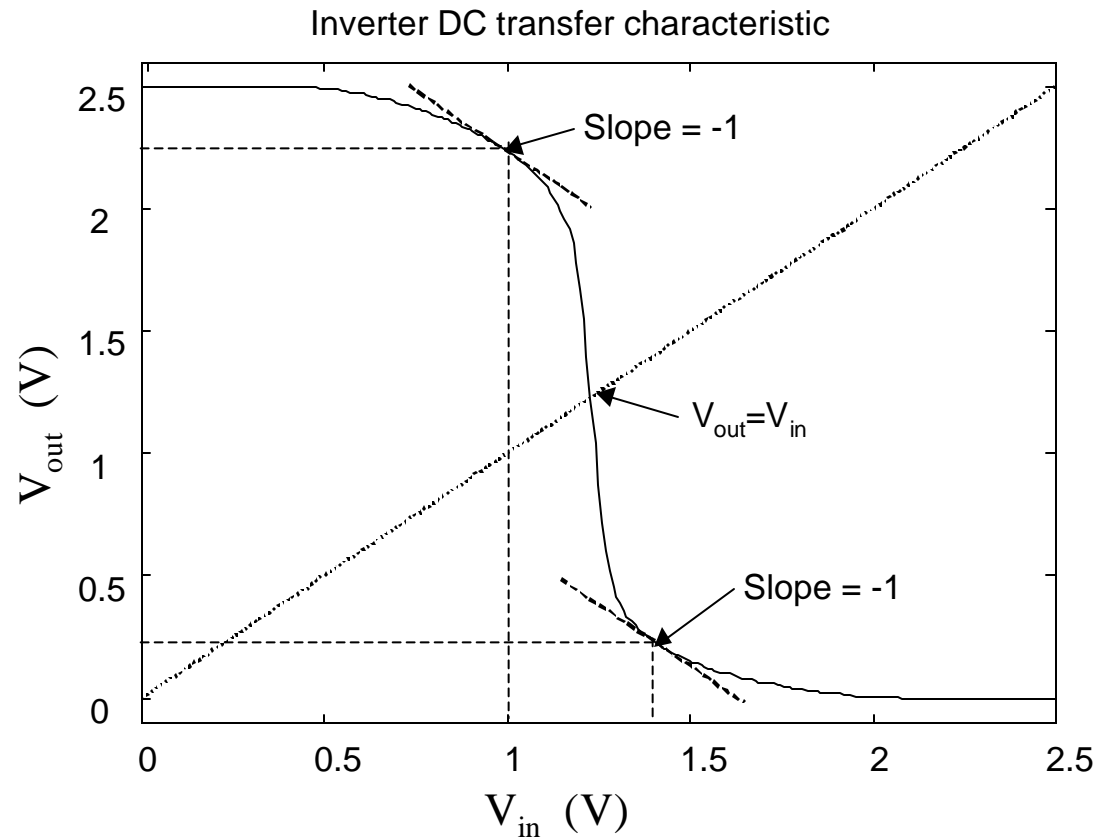
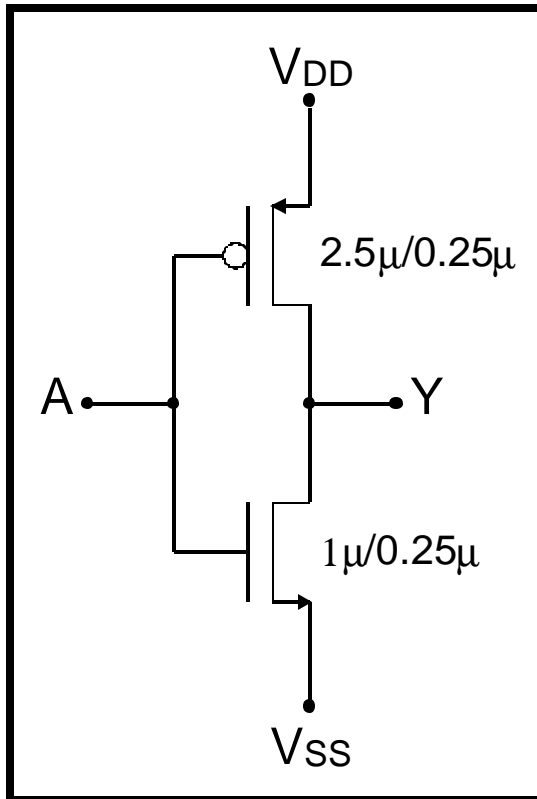



A	B	Y	
0	0	?	(high Z)
0	1	?	(high Z)
1	0	good 0	
1	1	bad 1	(source follower)

The CMOS inverter



The CMOS inverter

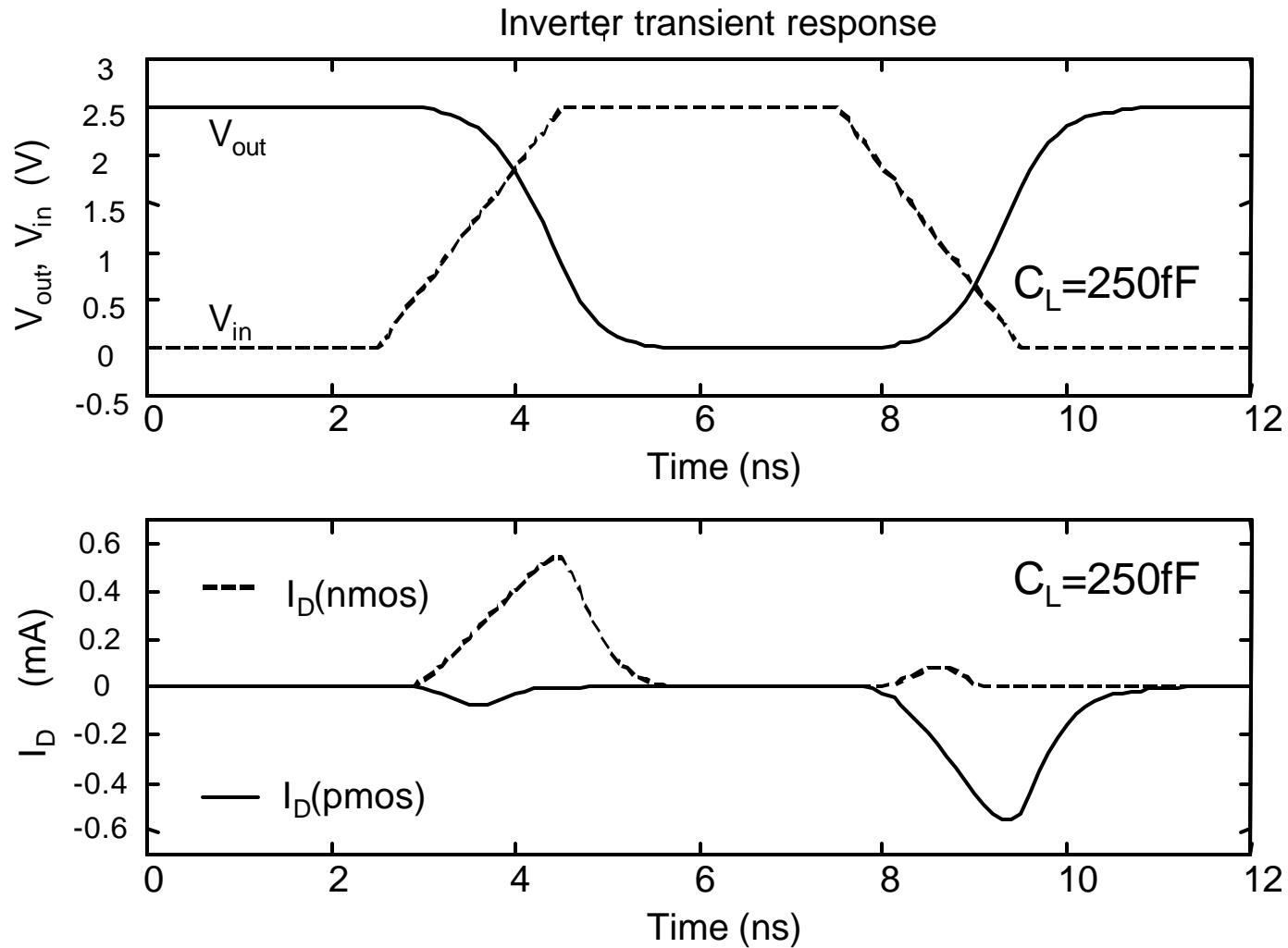


The CMOS inverter

Regions of operation (balanced inverter):

V_{in}	n-MOS	p-MOS	V_{out}
0	cut-off	linear	V_{dd}
$V_{TN} < V_{in} < V_{dd}/2$	saturation	linear	$\sim V_{dd}$
$V_{dd}/2$	saturation	saturation	$V_{dd}/2$
$V_{dd} - V_{TP} > V_{in} > V_{dd}/2$	linear	saturation	~ 0
V_{dd}	linear	cut-off	0

The CMOS inverter



The CMOS inverter

- Propagation delay
 - Main origin: load capacitance

$$t_{pLH} = \frac{C_L \cdot V_{dd}}{k_p (V_{dd} - |V_{TP}|)^2} \approx \frac{C_L}{k_p \cdot V_{dd}}$$

$$t_{pHL} = \frac{C_L \cdot V_{dd}}{k_n (V_{dd} - |V_{TN}|)^2} \approx \frac{C_L}{k_n \cdot V_{dd}}$$

$$t_p \approx \frac{1}{2} (t_{pLH} + t_{pHL}) = \frac{C_L}{2 \cdot V_{dd}} \left(\frac{1}{k_n} + \frac{1}{k_p} \right)$$

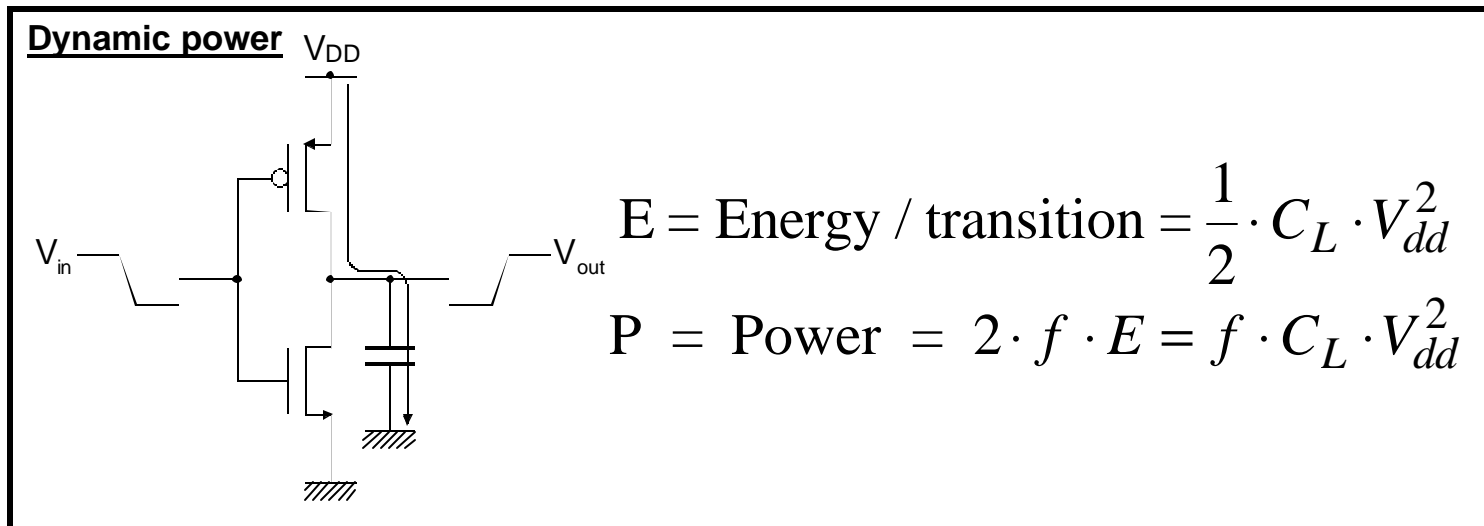
- To reduce the delay:
 - Reduce C_L
 - Increase k_n and k_p . That is, increase W/L

The CMOS inverter

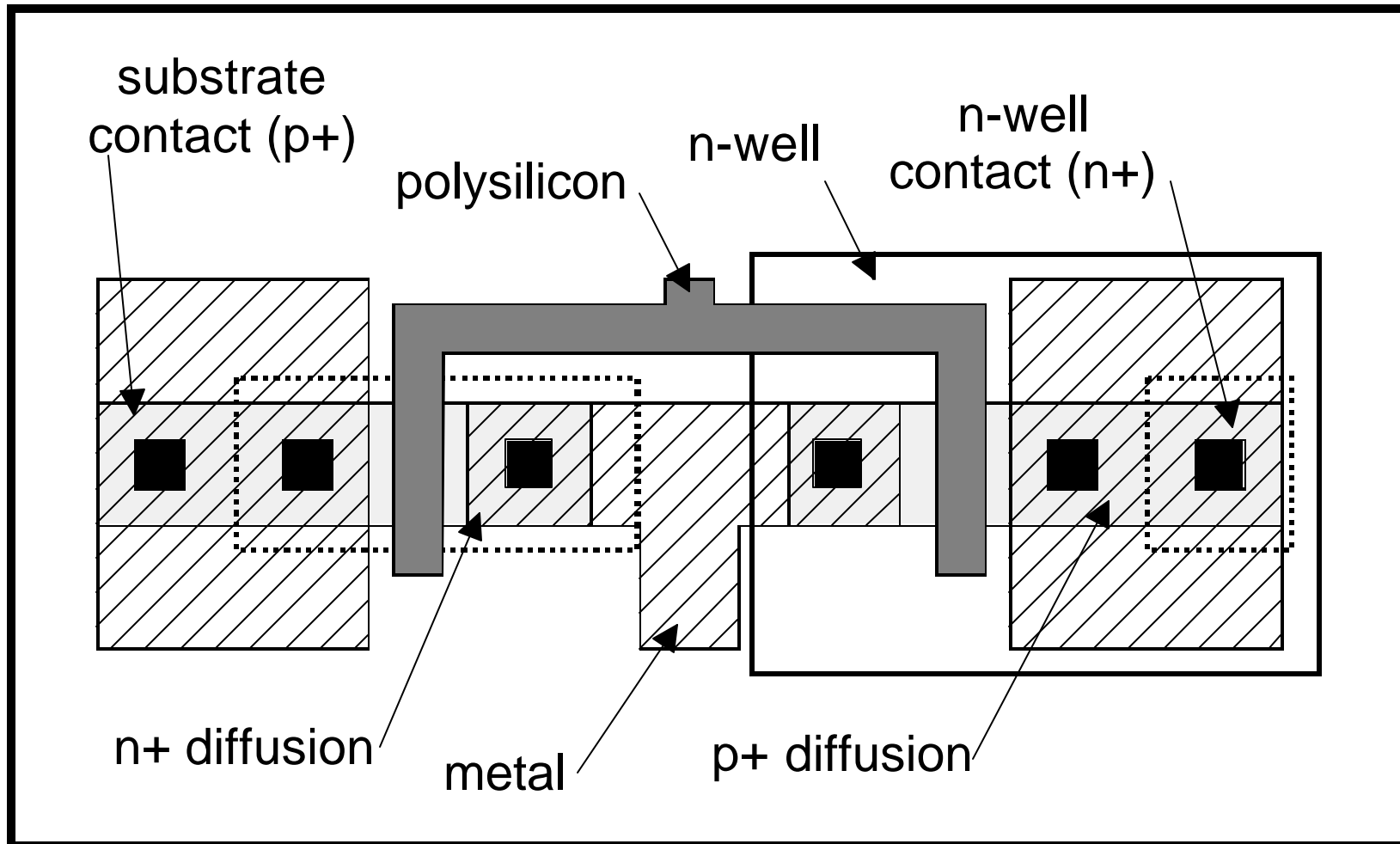
- CMOS power budget:
 - Dynamic power consumption:
 - Charging and discharging of capacitors
 - Short circuit currents:
 - Short circuit path between power rails during switching
 - Leakage
 - Leaking diodes and transistors

The CMOS inverter

- The dynamic power dissipation is a function of:
 - Frequency
 - Capacitive loading
 - Voltage swing
- To reduce dynamic power dissipation
 - Reduce: C_L
 - Reduce: f
 - Reduce: $V_{dd} \Leftarrow$ The most effective action



The CMOS inverter



The CMOS inverter

