OUTLINE

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VHDL: THE ALLIANCE SUBSET
VLSI Design Techniques

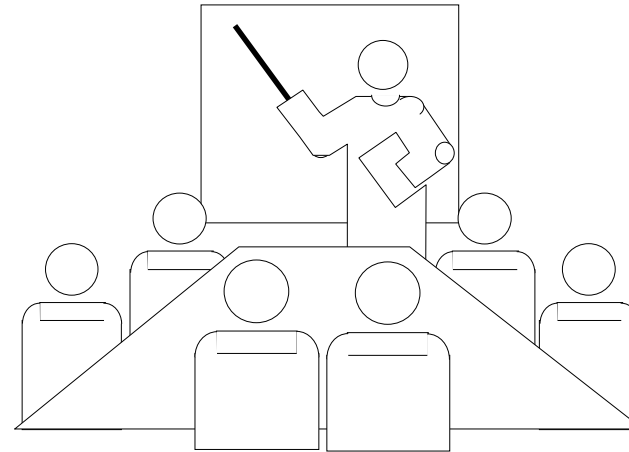# Why a Subset ? (1)

1 - Complex Language

Developing a compiler is
hard and time consuming

Why a Subset ? (2)

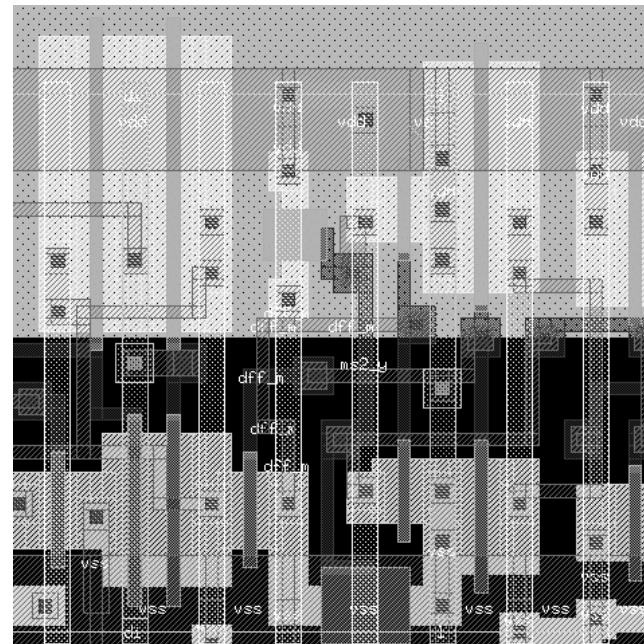## 2 - Educational Needs

➢ Understanding Time

➢ Univocal (Ex: One way in describing a register)

Why a Subset ? (3)

3 - Our Environment

➢ V L S I

Criterions

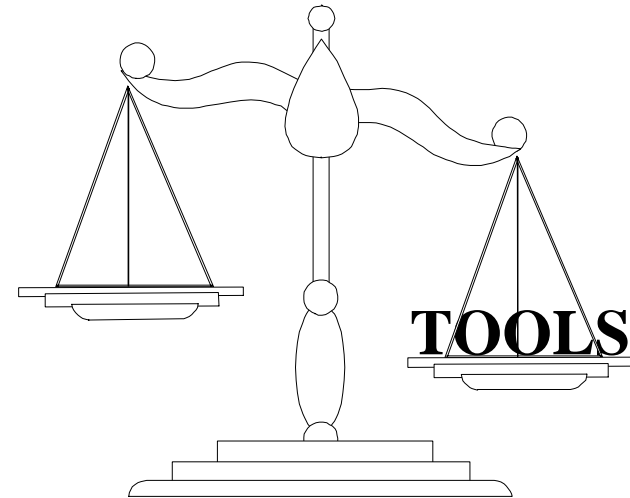## Users versus Tools Requirements

➢ Finding the Good Balance   **USERS   TOOLS**
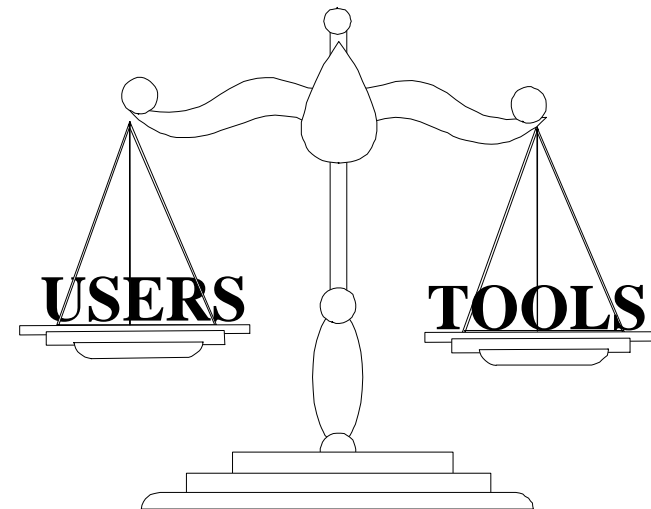
Tools' Requirements (1)

Which Tools use VHDL ?

➢ Simulator

➢ Synthesis Tools

➢ Placer & Router

➢ Functional Abstractor

➢ Formal Proover

TOOLS

Tools' Requirements (2)

➢ **SYNTHESIS TOOLS**

    ✗ A register must be identified in a syntactical way

    ✗ A bus must be identified in a syntactical way

    ✗ Signals must have the BIT type ('0' , '1')

    ✗ No timing

➢ **FORMAL PROOVER**

    ✗ A register must be identified in a syntactical way

    ✗ A bus must be identified in a syntactical way

Tools' Requirements (3)

➤ **PLACER & ROUTER**

    ✘ No mixing between structural and behavioral views
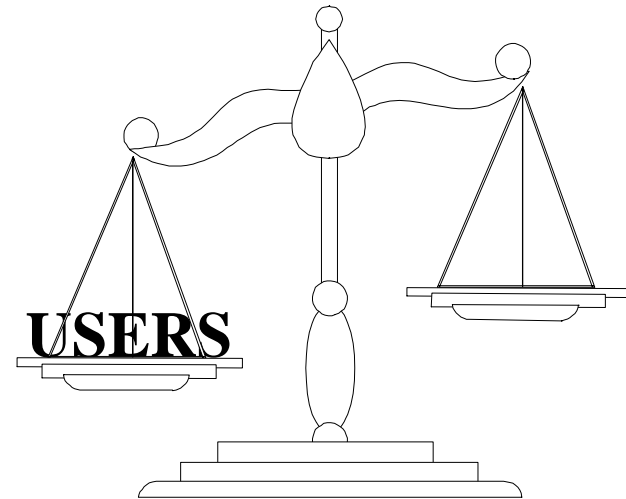
➤ **FUNCTIONAL ABSTRACTOR**

    ✘ VHDL subset as close as possible to the hardware

➤ **SIMULATOR**

    ✘ No abstract types

    ✘ No timing

Users' Requirements

Looking for the Largest
Subset ...

USERS

The Good Subset

✔ Lets the user describe his circuit easily

✔ Do not deteriorate the tool with a complex language

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Alliance Internal & External Aspects

External Aspect

- ✔ Name
- ✔ Interface
- ✘ Color
- ✘ Temperature
- ✘ ------

What is visible

Internal Aspect

- ✔ Structural
- ✔ Behavioral

- ✔ Signal
- ✔ Component
- ✔ Instance

How it works

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Alliance External Aspect (1)

Example

CIRCUIT NAME

PORT NAME

```
entity PARITY is
    port ( A, B, C, D : in BIT;
           P              : out BIT
    );
end PARITY;
```
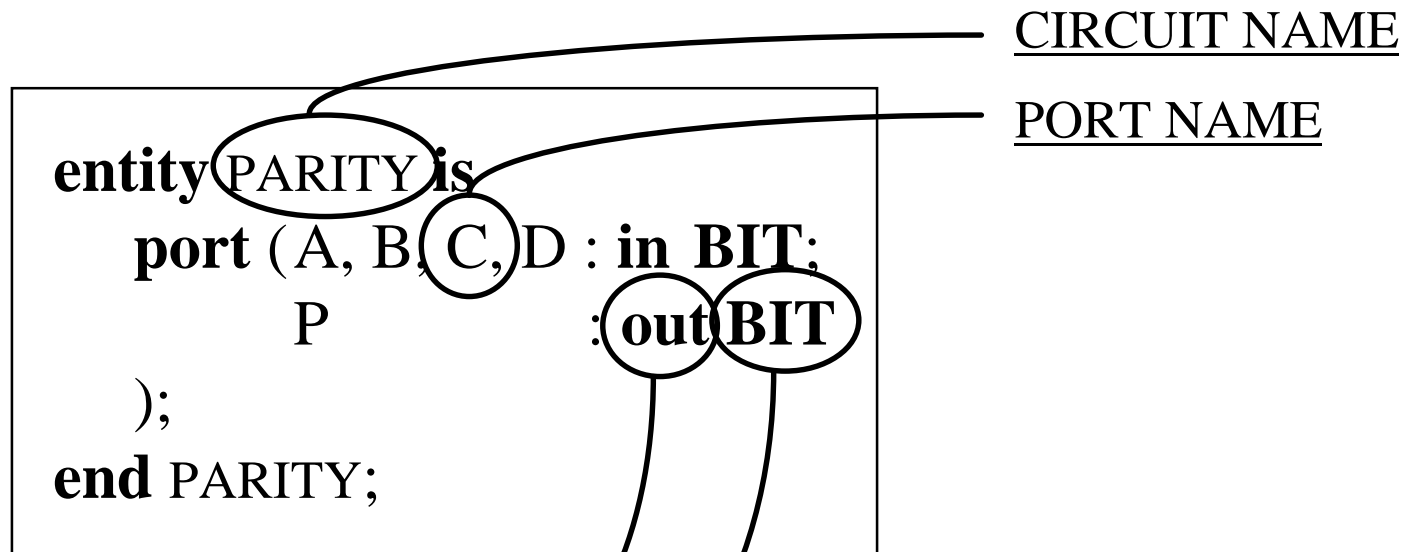
MODE: **in**, **out**, **inout**...

DATA TYPE

Alliance External Aspect (2)

Example

```
entity ADDER_32 is
    port (
            A : IN BIT_VECTOR (0 TO 31);
            B : IN BIT_VECTOR (0 TO 31);
            CIN : IN BIT;

            SUM : OUT BIT_VECTOR (31 DOWNTO 0);

            COUT : OUT BIT

    );
end ADDER_32 ;
```

Alliance Internal Aspect (1)

Structural

ARCHITECTURE Pstruct **OF** Parity **IS**
   COMPONENT XOR_Y
     PORT (

         I0 : **IN BIT** ;

         I1 : **IN BIT**;

         T : **OUT BIT**

       );

END COMPONENT;
SIGNAL Parity_AB : **BIT**;
SIGNAL Parity_CD : **BIT**;

DECLARATIVE
PART

Alliance Internal Aspect (2)

Structural

BEGIN

    Instance_AB : XOR_Y

        PORT MAP (

                I0 => A,

                I1 => B,

                T => Parity_AB

            );

    Instance_CD : XOR_Y

        PORT MAP (

                I0 => C,

                I1 => D,
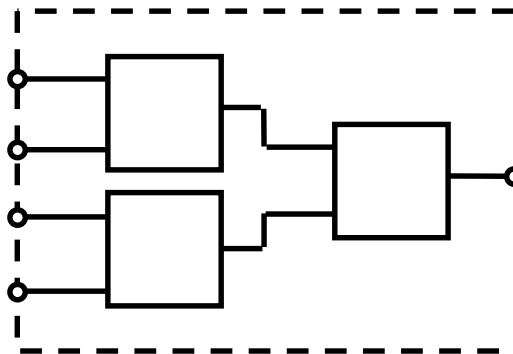
                T => Parity_CD

            );

DESCRIPTION PART

Alliance Internal Aspect (3)

Structural

Instance_AB : XOR_Y
      PORT MAP (
                I0 => Parity_AB,
                I1 => Parity_CD,
                T => P
         );
END;

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Alliance Internal Aspect (1)

Behavioral

BOOLEAN FUNCTIONS:

- ♦ **AND**
- ♦ **OR**
- ♦ **XOR**
- ♦ **NAND**
- ♦ **NOR**
- ♦ **NOT**

Always use brackets.

Alliance Internal Aspect (2)

Behavioral

- **ASSERT** (Condition)
  - **REPORT** "Message"
    - **SEVERITY** Level;

Very useful in large-scale design.
- Allows encoding specific constraints and error conditions
- Provide useful messages.
- Stop the simulation when constraints are not met.

Alliance Internal Aspect (3)

Behavioral

Three Kinds of Assignment

Simple Assignment

S <= A **AND** B;

Always

Conditional Assignment

S <= A **AND** B **WHEN** (C = '0') **ELSE**
D **OR** E;

Alliance Internal Aspect (4)

Behavioral

Selective Assignment

```
WITH Address(3 downto 0) SELECT
    Out <= "000100" WHEN "0000",
           "000101" WHEN "0001",
           ---------
           "000000" WHEN Others;
```

Alliance Internal Aspect (5)

Behavioral

REGISTERS

    SIGNAL myregister : **REG_BIT REGISTER**;

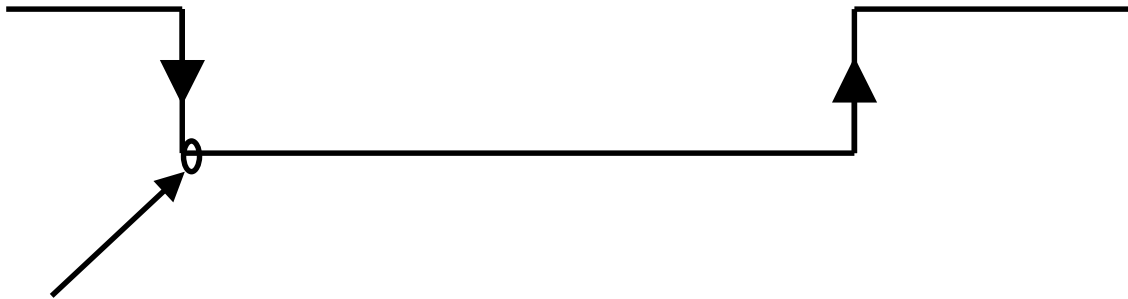   store : **BLOCK** (CK = '0' **AND NOT CK'STABLE**)
    BEGIN
    myregister <= **GUARDED** I0;
    END BLOCK store;

Alliance Internal Aspect (6)

Behavioral

(CK = '0' **AND NOT CK'STABLE**)

Alliance Internal Aspect (7)

Behavioral

BUS

SIGNAL my_bus1 : **MUX_BIT BUS**;

Only <u>one</u> driver active at the same time.

SIGNAL my_bus2 : **WOR_BIT BUS**;

Many drivers drive the same value.