ICTP Microprocessor Laboratory
Second Central American Regional Course on Advanced VLSI Design Techniques
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Scaling Impact on Analog Circuit Performance

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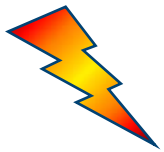
Outline

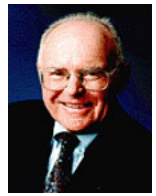
- Scaling down of CMOS technologies
- How scaling works for devices and interconnections
- Scaling impact on noise
- Scaling impact on matching
- Analog performance of submicron processes
- Substrate noise in mixed-mode integrated circuits

Outline



- Scaling down of CMOS technologies
  - Moore's law
  - An example: Intel Microprocessors
  - The International Technology Roadmap for Semiconductors: what will happen in the next 15 years?
- How scaling works for devices and interconnections
- Scaling impact on noise
- Scaling impact on matching
- Analog performance of submicron processes
- Substrate noise in mixed-mode integrated circuits

Moore's law



1965: Number of Integrated Circuit components will double every year

G. E. Moore, "Cramming More Components onto Integrated Circuits", *Electronics*, vol. 38, no. 8, 1965.

1975: Number of Integrated Circuit components will double every 18 months

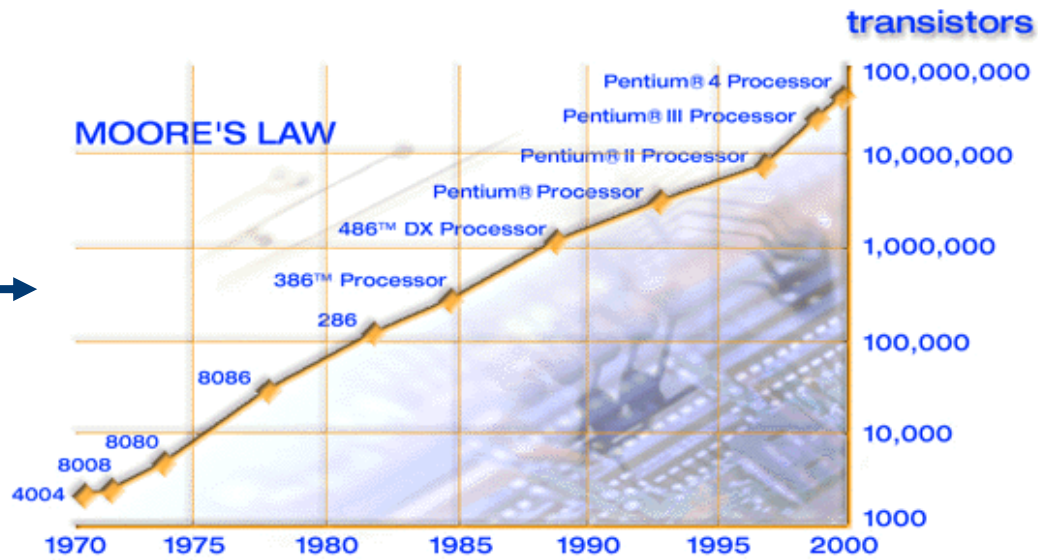
G. E. Moore, "Progress in Digital Integrated Electronics", *Technical Digest of the IEEE IEDM 1975*.

1996: The definition of "Moore's Law" has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line. I don't want to do anything to restrict this definition. - G. E. Moore, 8/7/1996

P. K. Bondyopadhyay, "Moore's Law Governs the Silicon Revolution", *Proc. of the IEEE*, vol. 86, no. 1, Jan. 1998, pp. 78-81.

An example:

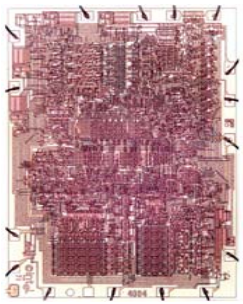
Intel's Microprocessors



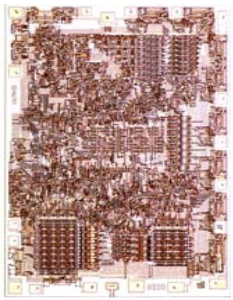
http://www.intel.com/

The intel Microprocessors

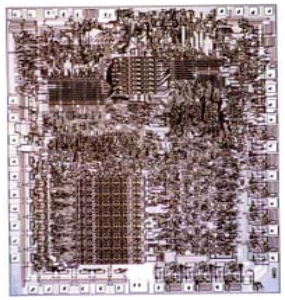
4004
11 / 1971
2300
10 μm
108 KHz



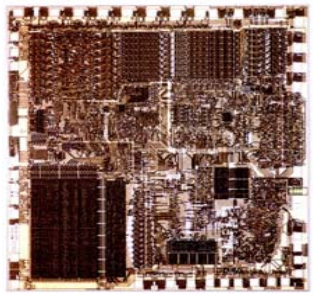
8008
04 / 1972
3500
10 μm
200 KHz



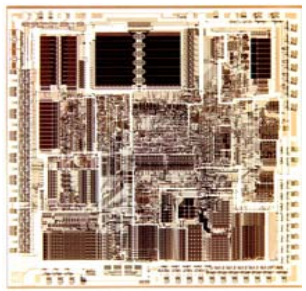
8080
04 / 1974
4500
6 μm
2 MHz



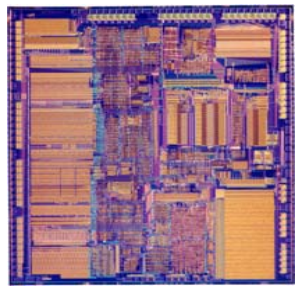
8088
06 / 1979
29000
3 μm
8 MHz



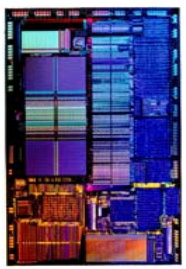
80286
02 / 1982
134000
1.5 μm
12 MHz



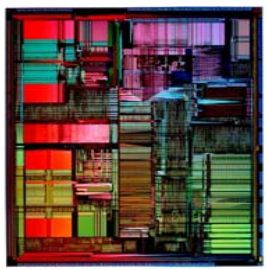
Intel386™
10 / 1985
275000
1 μm
16 MHz



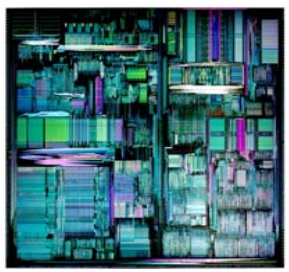
Intel486™ DX
04 / 1989
1.2 M
1 μm
25 MHz



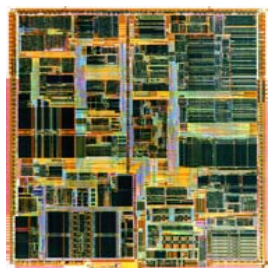
Pentium®
03 / 1993
3.1 M
0.8 μm
66 MHz



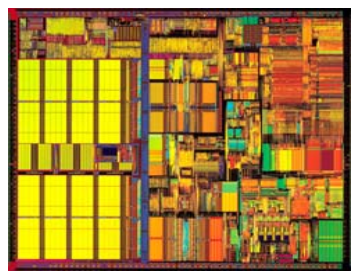
Pentium® Pro
11 / 1995
5.5 M
0.6 μm
150 MHz



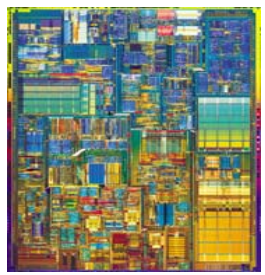
Pentium® II
05 / 1997
7.5 M
0.35 μm
233 MHz



Pentium® III
02 / 1999
9.5 M
0.25 μm
500 MHz



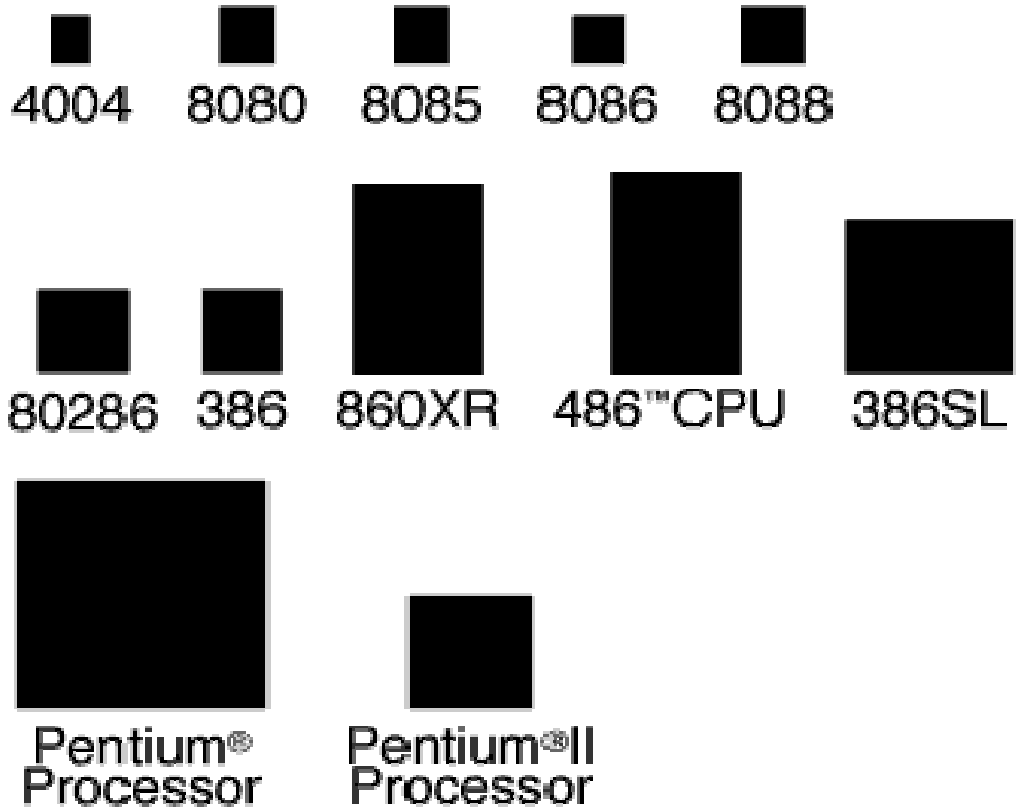
Pentium® 4
11 / 2000
42 M
0.18 μm
1.5 GHz



http://www.intel.com/

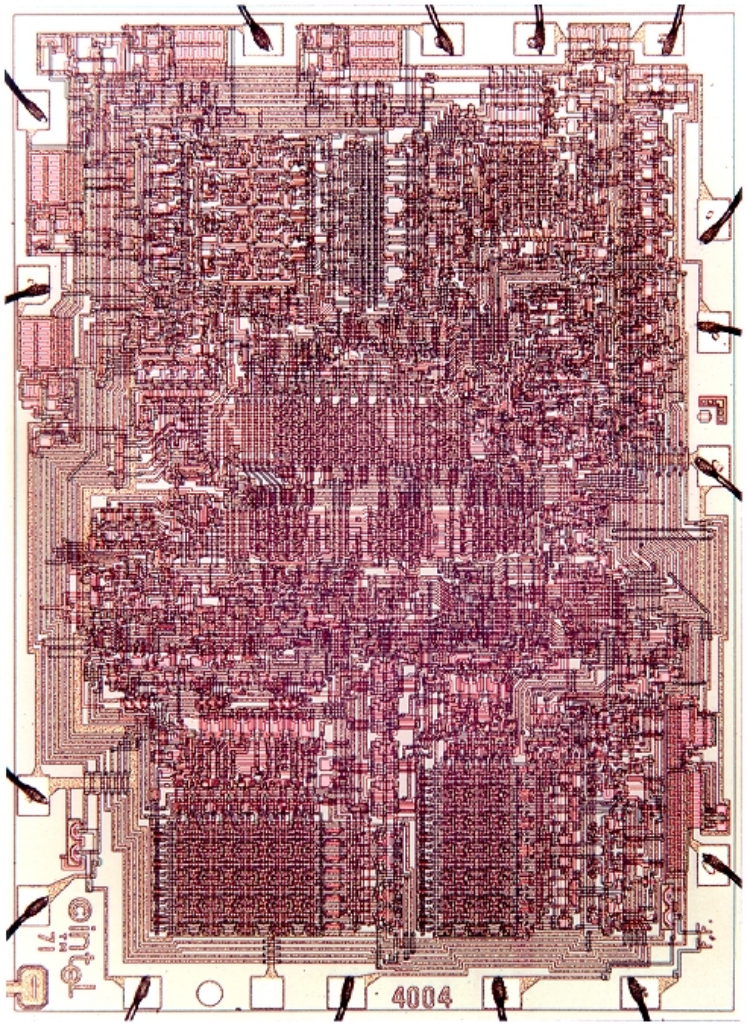
The intel Microprocessors

The correct size relationship.



http://www.intel.com/

The intel 4004 processor



http://www.intel.com/

- **Introduced: 15/11/1971**
- **Clock: 108 KHz**
- **2300 Transistors**
- **10 μm technology (NMOS)**

The Pentium® 4

http://www.intel.com/

The first Pentium® 4

- Introduced: 20/11/2000
- Clock: 1.5 GHz
- 42 Million Transistors
- 0.18 μm technology

A more recent one

- Introduced: 21/06/2004
- Clock: 3.6 GHz
- 125 Million Transistors
- 0.09 μm technology

The Roadmap History

- **The National Technology Roadmap for Semiconductors (NTRS):**

  Sponsored by the Semiconductor Industry Association (SIA)

  Edited in 1992, 1994 and 1997

- **The International Technology Roadmap for Semiconductors (ITRS):**

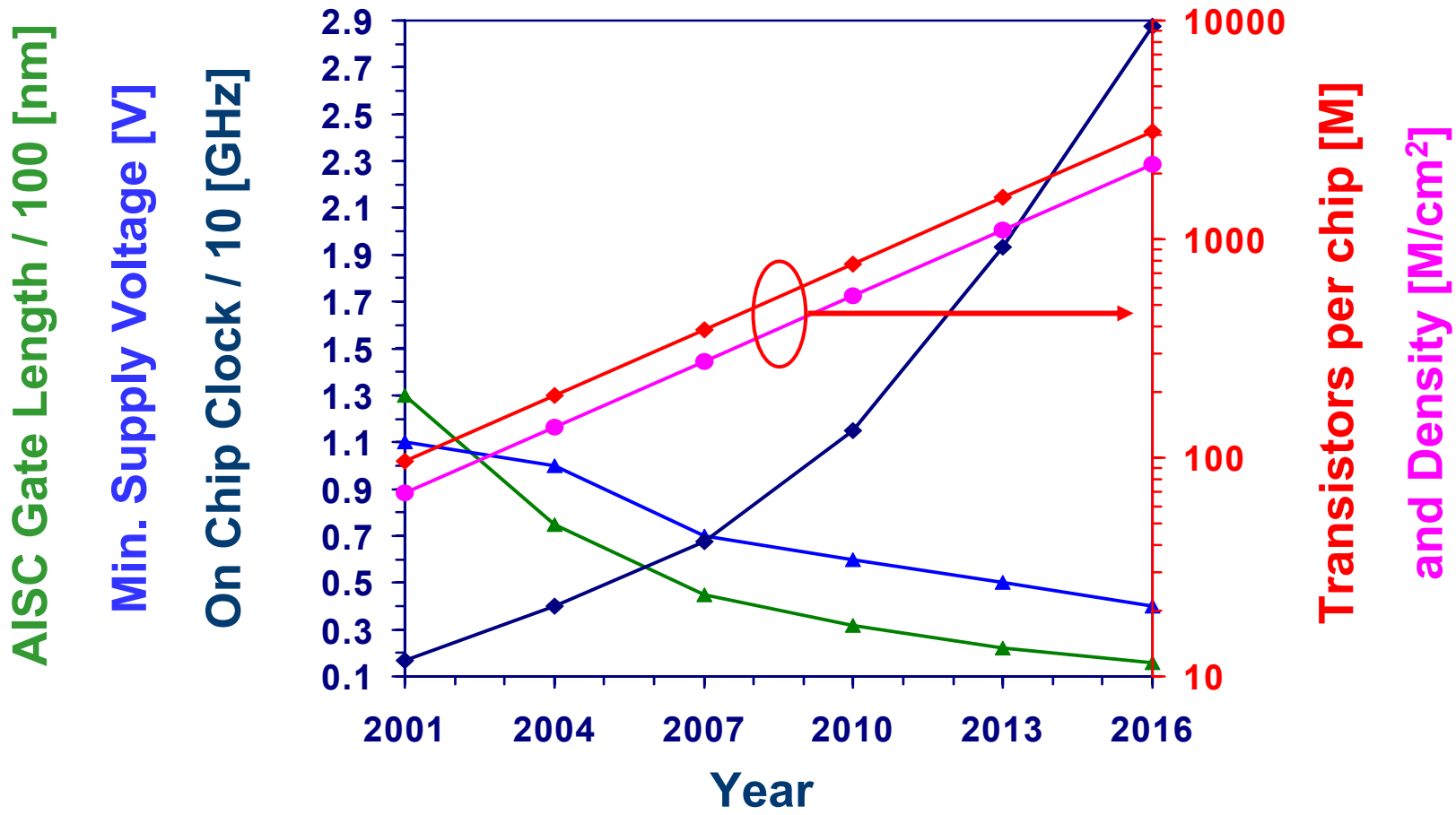
  Sponsored by:

  - **Semiconductor Industry Association (SIA)**
  - **European Electronics Component Manufacturers Association (EECA)**
  - **Korea Semiconductor Industry Association (KSIA)**
  - **Japan Electronics and Information Technology Industries Association (JEITA)**
  - **Taiwan Semiconductor Industry Association (TSIA)**

  Edited in 1998 (Update), 1999, 2000 (Update), 2001, 2002 (Update), 2003

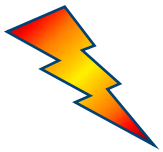
These documents always contained a 15-year outlook of the major trends of the semiconductor industry

Future perspectives



Data taken from the Executive Summary of
The International Technology Roadmap for Semiconductors (2001 Edition)

Outline

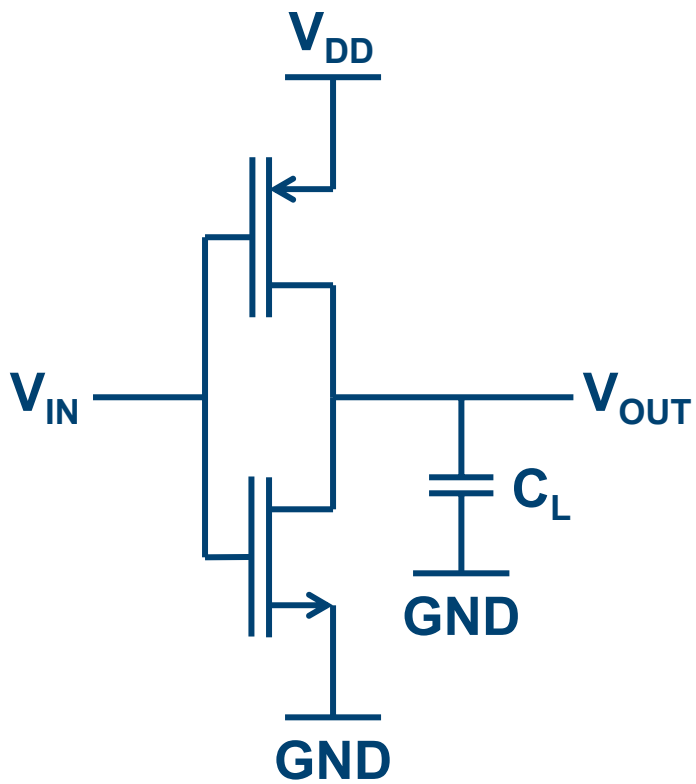


- Scaling down of CMOS technologies
- How scaling works for devices and interconnections
  - Constant field scaling
  - Generalized scaling
  - Scaling of interconnections
- Scaling impact on noise
- Scaling impact on matching
- Analog performance of submicron processes
- Substrate noise in mixed-mode integrated circuits

Why scaling ???

Scaling improves density, speed and power consumption of digital circuits

Example: CMOS inverter



$$P_{static} = I_{leakage} \cdot V_{DD}$$

$$P_{dynamic} = C_L \cdot V_{DD}^2 \cdot f$$

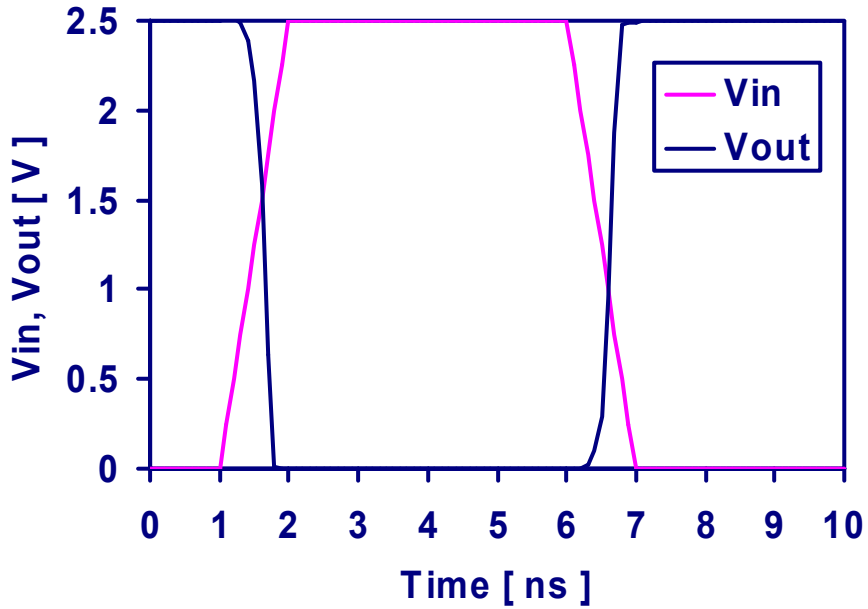
$$PDP = C_L \cdot V_{DD}^2$$

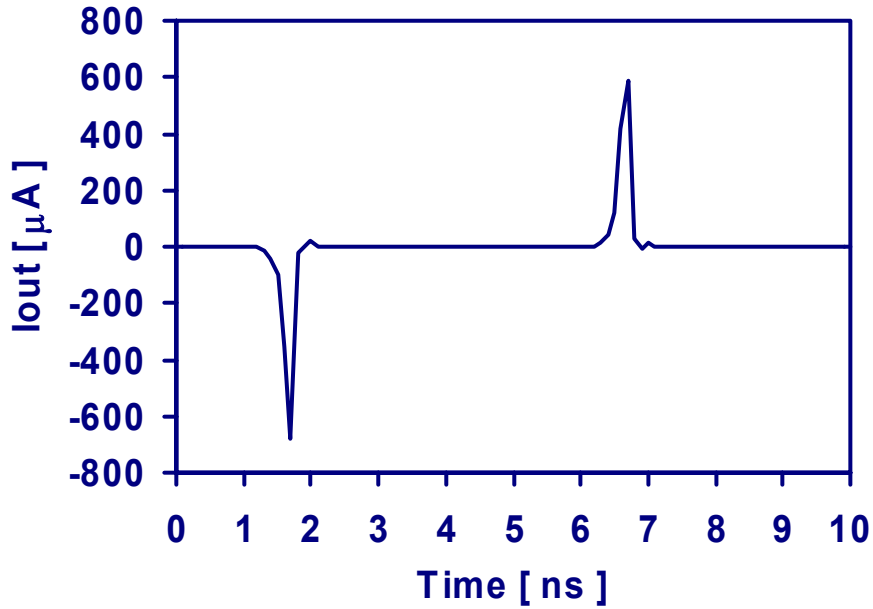
Power-delay product

t_{ox} ↓ V_{DD} ↓ C_L ↓

Dynamic current in an inverter

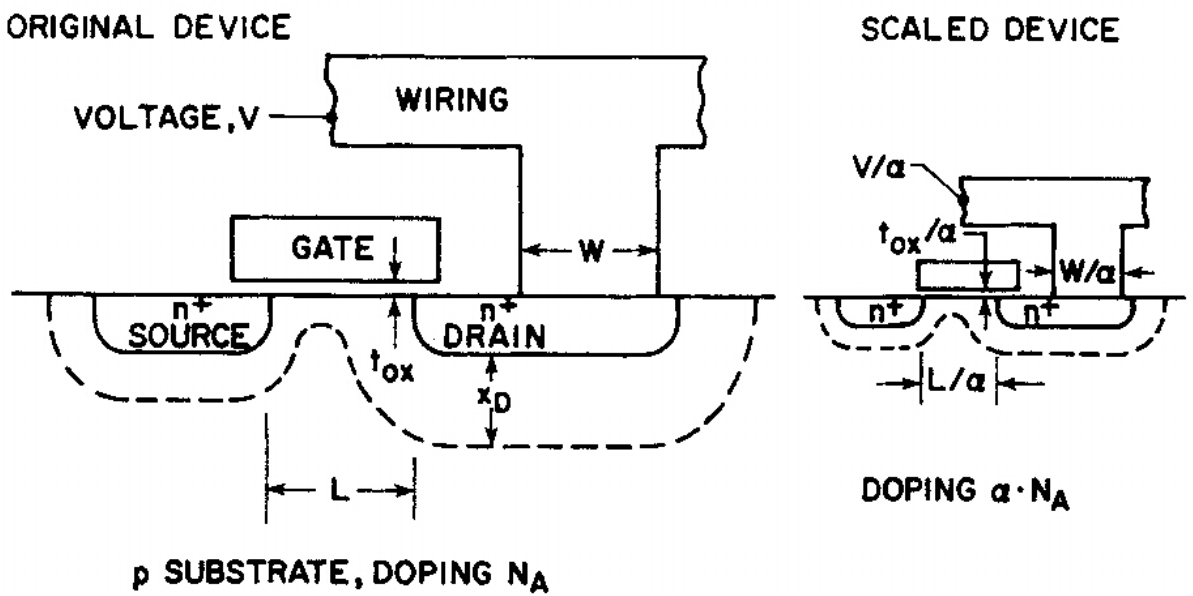
Simulation of a chain of two inverters in a 0.25 μm CMOS technology





Constant field scaling

The aim of scaling is to reduce the device dimensions (to improve the circuit performance) without introducing effects which could disturb the good operation of the device.



$$x_d = \sqrt{\frac{2\varepsilon_{Si}}{qN_A}}\sqrt{\phi_{bi} + V}$$

B. Davari et al., "CMOS Scaling for High Performance and Low Power - The Next Ten Years", *Proc. of the IEEE*, vol. 87, no. 4, Apr. 1999, pp. 659-667.

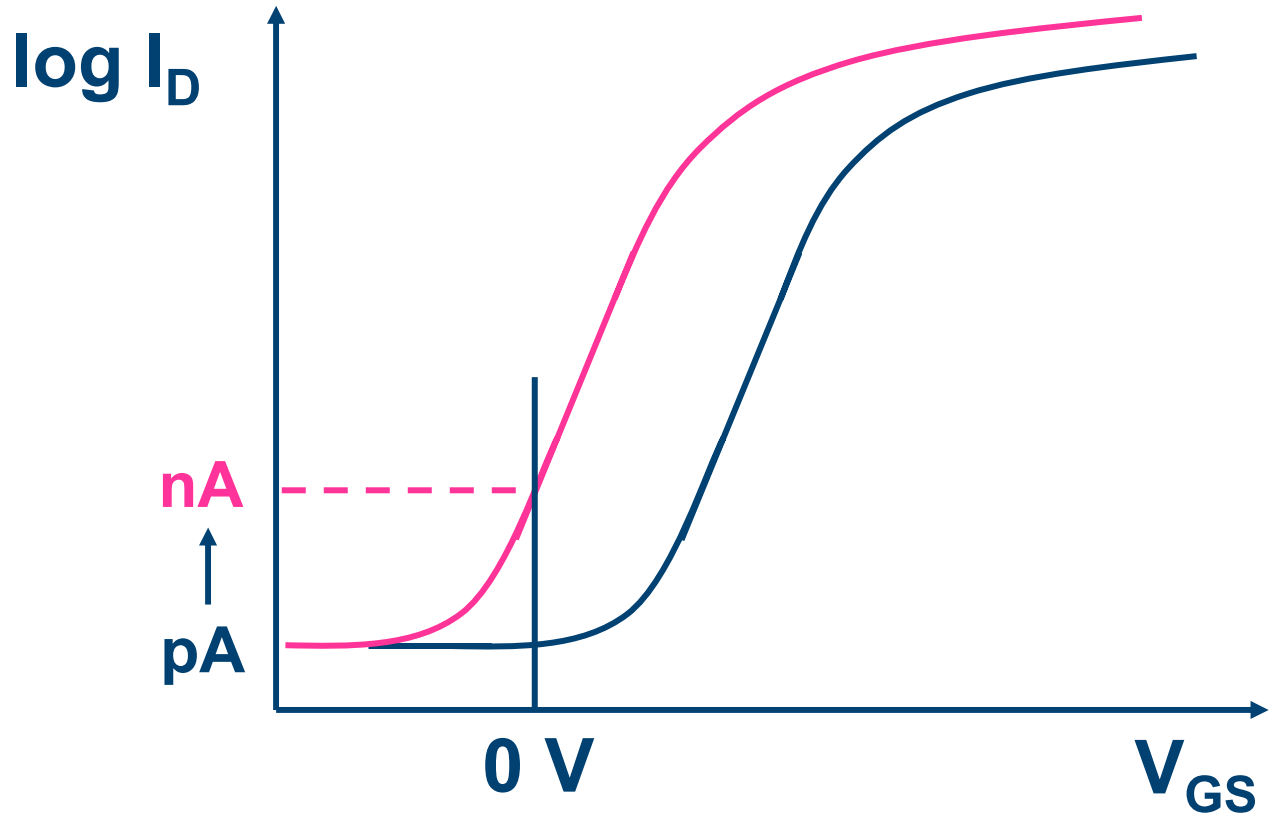
Constant field scaling

Summary of the scaling factors for several quantities

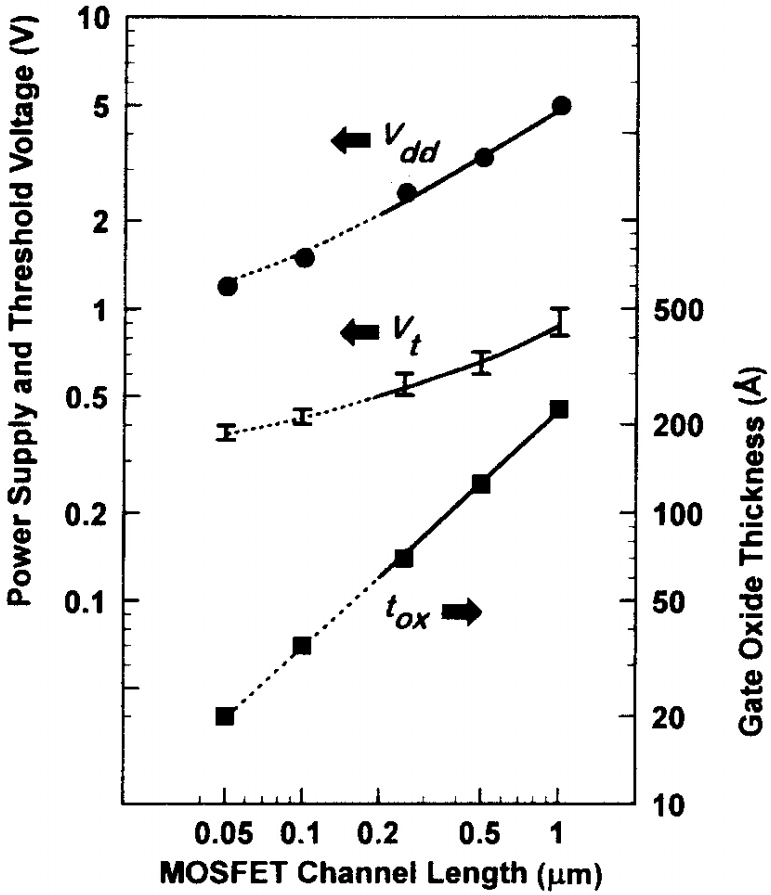
Quantity	Scaling Factor	Quantity	Scaling factor
Device dimensions (L, W, t_{ox}, x_D)	$1/\alpha$	Capacitances	$1/\alpha$
Area	$1/\alpha^2$	Capacitances per unit area	α
Devices per unit of chip area (density)	α^2	Charges	$1/\alpha^2$
Doping concentration (N_A)	α	Charges per unit area	1
Bias voltages and V_T	$1/\alpha$	Electric field intensity	1
Bias currents	$1/\alpha$	Body effect coefficient (γ)	$1/\sqrt{\alpha}$
Power dissipation for a given circuit	$1/\alpha^2$	Transistor transit time (τ)	$1/\alpha$
Power dissipation per unit of chip area	1	Transistor power-delay product	$1/\alpha^3$

Constant field scaling problem

Subthreshold slope and width of the moderate inversion region do not scale. This can have a devastating impact on the static power consumption of a digital circuit.



Generalized scaling

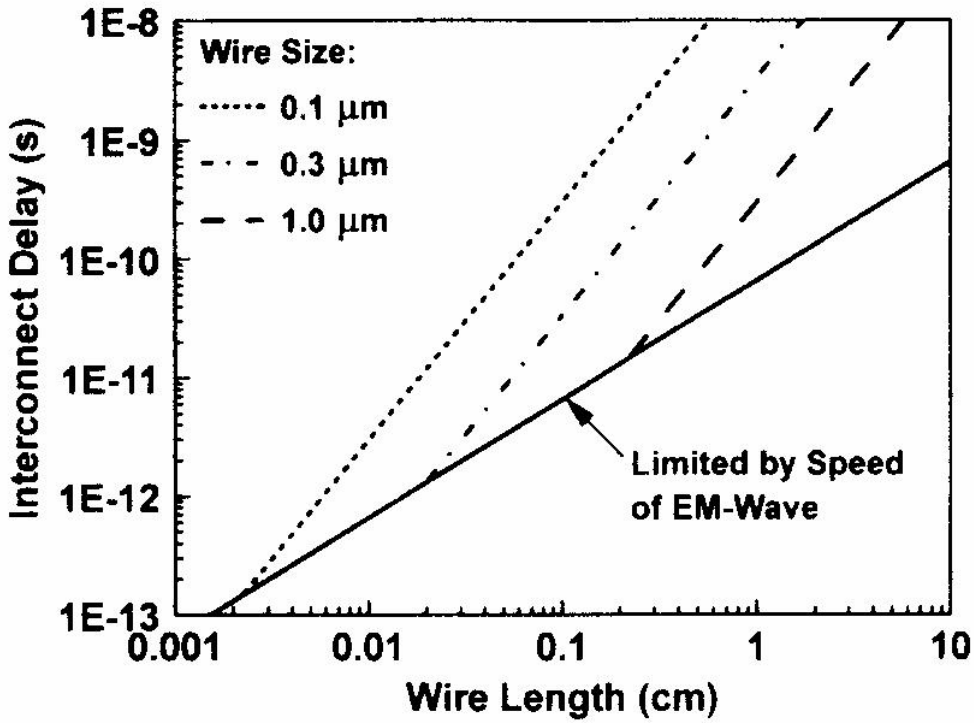


- The dimensions in the device scale as in the *constant field* scaling
- V_{dd} scales to have reasonable electric fields in the device, but slower than t_{ox}, to have an useful voltage swing for the signals
- The doping levels are adjusted to have the correct depletion region widths
- To limit the subthreshold currents, V_T scales more slowly than V_{dd}

Y. Taur et al., "CMOS Scaling into the Nanometer Regime", *Proc. of the IEEE*, vol. 85, no. 4, Apr. 1997, pp. 486-504.
Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998, p. 186.

Scaling of interconnections

An accurate scaling of the interconnections is needed as well, so that we can profit at the circuit level of the improvements made at the device level. Interconnections are becoming more and more important in modern technologies because the delay they introduce is becoming comparable with the switching time of the digital circuits.

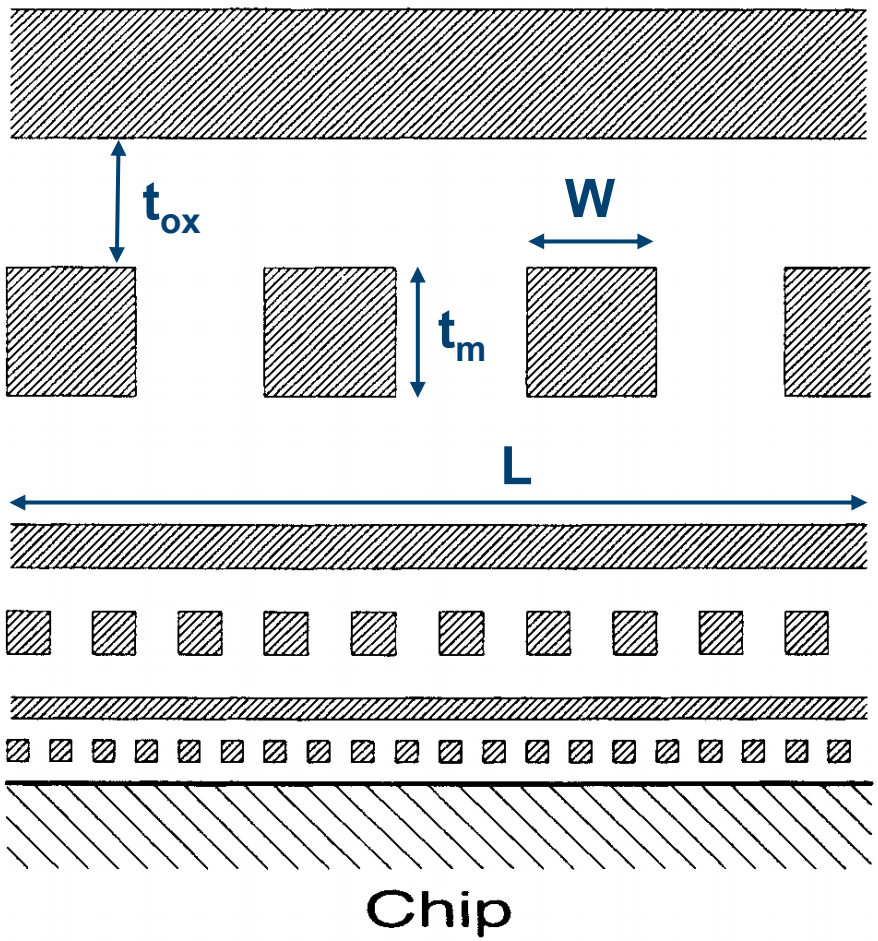


Y. Taur et al., "CMOS Scaling into the Nanometer Regime", *Proceedings of the IEEE*, vol. 85, no. 4, Apr. 1997, pp. 486-504.

T. N. Theis, "The future of interconnection technology", *IBM Journal of Research and Development*, vol. 44, no. 3, May 2000, pp. 379-390.

“Reverse” scaling

The scaling method is different from the one applied to devices



If W, L, t_m and t_{ox} are scaled by $1/\alpha$

- **Current density scales by α**
- **R scales by α, C scales by $1/\alpha$**
- **RC (delay) does not scale!!!**

In practice, wires dimensions are reduced only for local interconnections (but not t_m). At the chip scale, t_m and t_{ox} are increased (reverse scaling).

G. A. Sai-Halasz, "Performance trends in high-end processors", *Proceedings of the IEEE*, vol. 83, no. 1, January 1995, pp. 20-36.

Hierarchical scaling

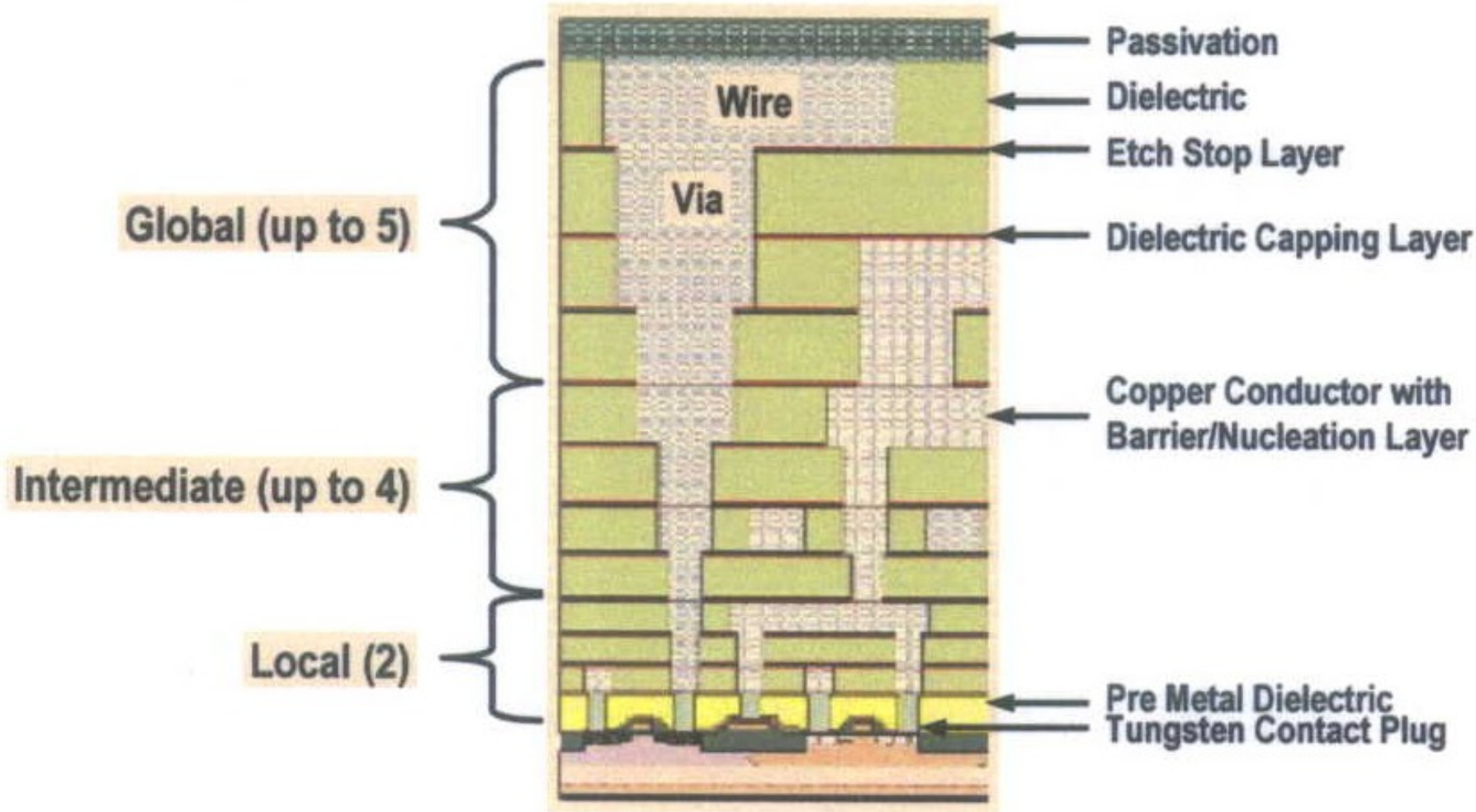


Figure 36 Cross-section of Hierarchical Scaling

The International Technology Roadmap for Semiconductors (2001 Edition)

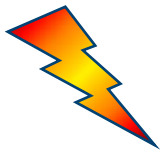
Generalized selective scaling

Physical parameter	Constant-Electric Field Scaling Factor	Generalized Scaling Factor	Generalized Selective Scaling Factor
Channel length, Insulator thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Wiring width, channel width	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric field in device	1	ε	ε
Voltage	$1/\alpha$	ε/α	ε/α_d
On-current per device	$1/\alpha$	ε/α	ε/α_w
Doping	α	$\varepsilon\alpha$	$\varepsilon\alpha_d$
Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w^2$
Capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Gate delay	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Power dissipation	$1/\alpha^2$	ε^2/α^2	$\varepsilon^2/\alpha_w\alpha_d$
Power density	1	ε^2	$\varepsilon^2\alpha_w/\alpha_d$

α is the dimensional scaling parameter, ε is the electric field scaling parameter, and α_D and α_W are separate dimensional scaling parameters for the selective scaling case. α_D is applied to the device vertical dimensions and gate length, while α_W applies to the device width and the wiring.

D. J. Frank et al., "Device Scaling Limits of Si MOSFETs and Their Application Dependencies", *Proc. IEEE*, vol. 89, no. 3, March 2001, pp. 259-288.

Outline



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Scaling impact on noise

$$\frac{\overline{v_{in}^2}}{\Delta f} = 4kTn\gamma\frac{1}{g_m} + \frac{K_a}{C_{ox}^2 WL}\frac{1}{f^{\alpha}}$$

$$g_m = \sqrt{\frac{2}{n}\mu C_{ox}\frac{W}{L}I_{DS}} \qquad C_{ox} = \frac{\varepsilon_{SiO_2}}{t_{ox}}$$

$t_{ox} \downarrow \quad C_{ox} \uparrow \quad g_m \uparrow$

White noise: keeping the same W/L ratio and the same current, we have an improvement in the noise since C_{ox} (and therefore g_m) increases with scaling.

1/f noise: we suppose that the constant K_a does not change with scaling. In this case, we have an improvement in the noise if we keep the same device area (WL), or we have the same noise if we scale both W and L. Data taken from the Roadmap foresee that K_a will remain more or less constant even for the most advanced CMOS processes. This must, of course, be verified…

Scaling impact on noise

For the same device dimensions and current, both the channel thermal noise and the flicker (1/f) noise should decrease

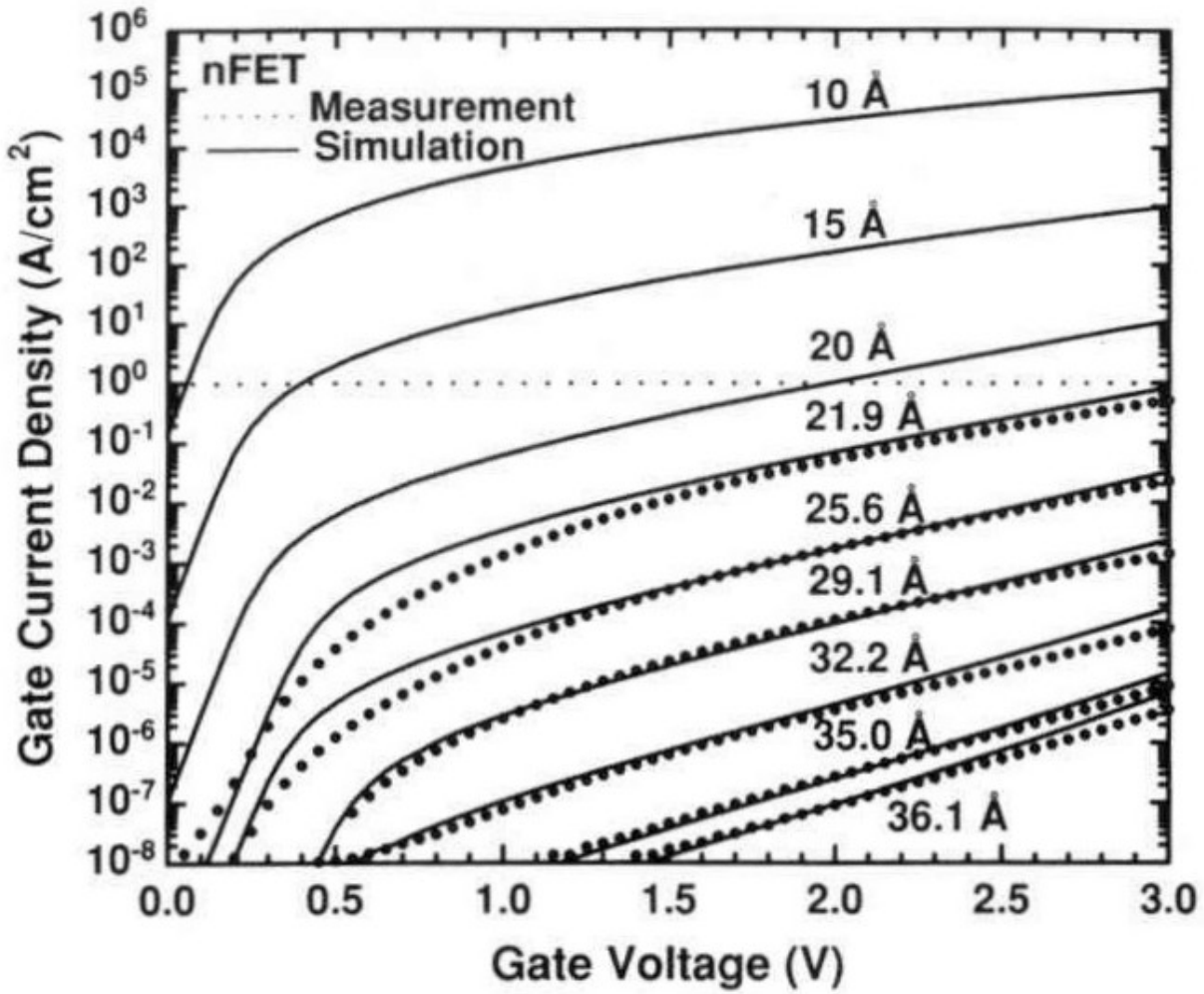
BUT

there can be other effects in submicron MOSFETs that tend to increase the noise, such as, for example, carriers heating and parasitic resistances.

The constant K_a is HIGHLY technology dependent. It might be difficult to keep it under control in new advanced processes. Moreover, the effect on 1/f noise on new dielectric materials in not yet known.

Another (possibly serious) source of problems in the future will be the leakage current through the gate oxide. Thinner gate oxides will have a much higher leakage current, which will have a higher shot noise.

Gate leakage current shot noise



$$\sqrt{\frac{\overline{i_n^2}}{\Delta f}} = 2qI$$

In the hypothesis:

- **current density = 1 A/cm²**
- **W = 1000 μm**
- **L = 0.1 μm**

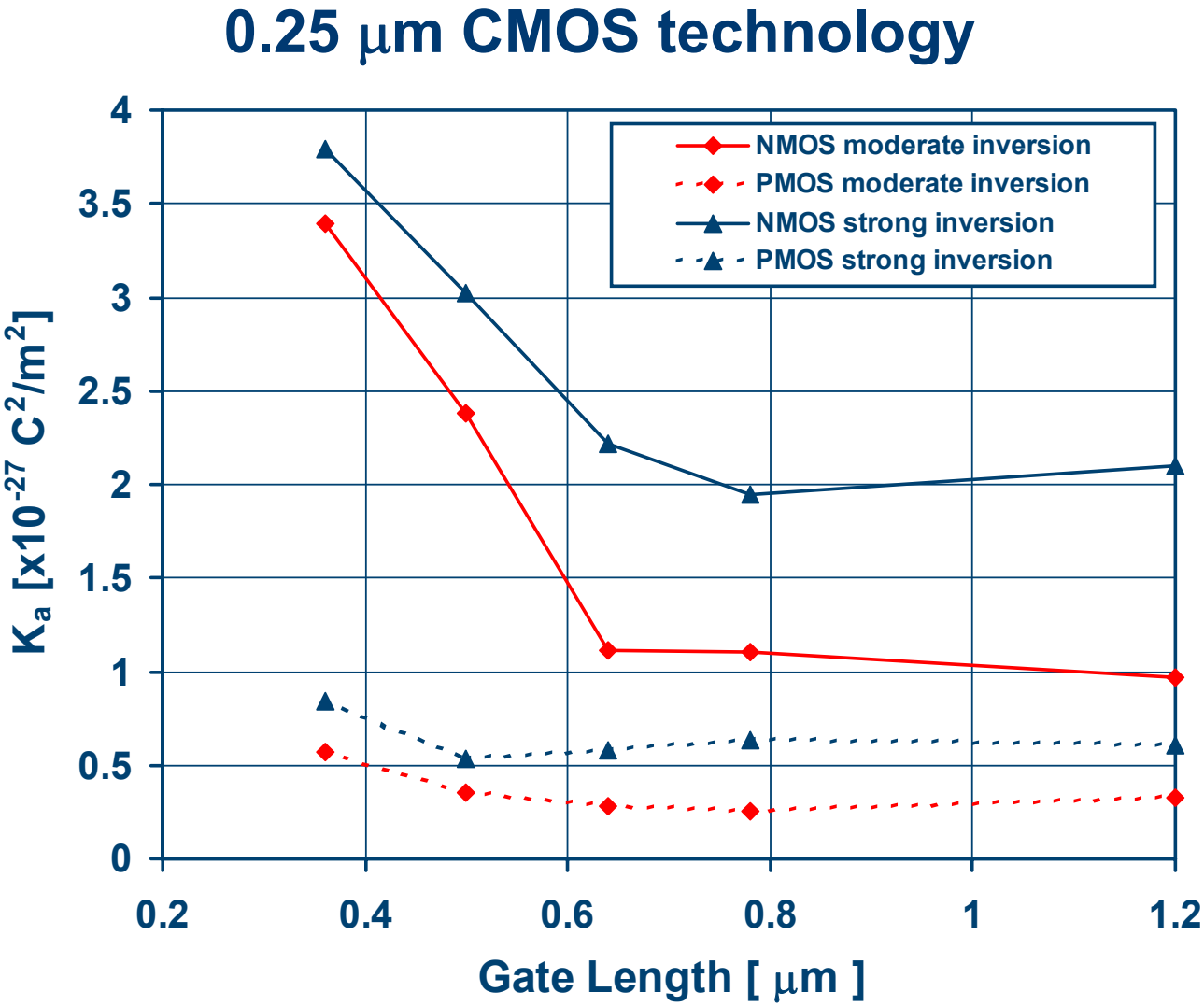
We have

- **I = 1 μA**
- **2qI = 0.56 pA/√Hz**

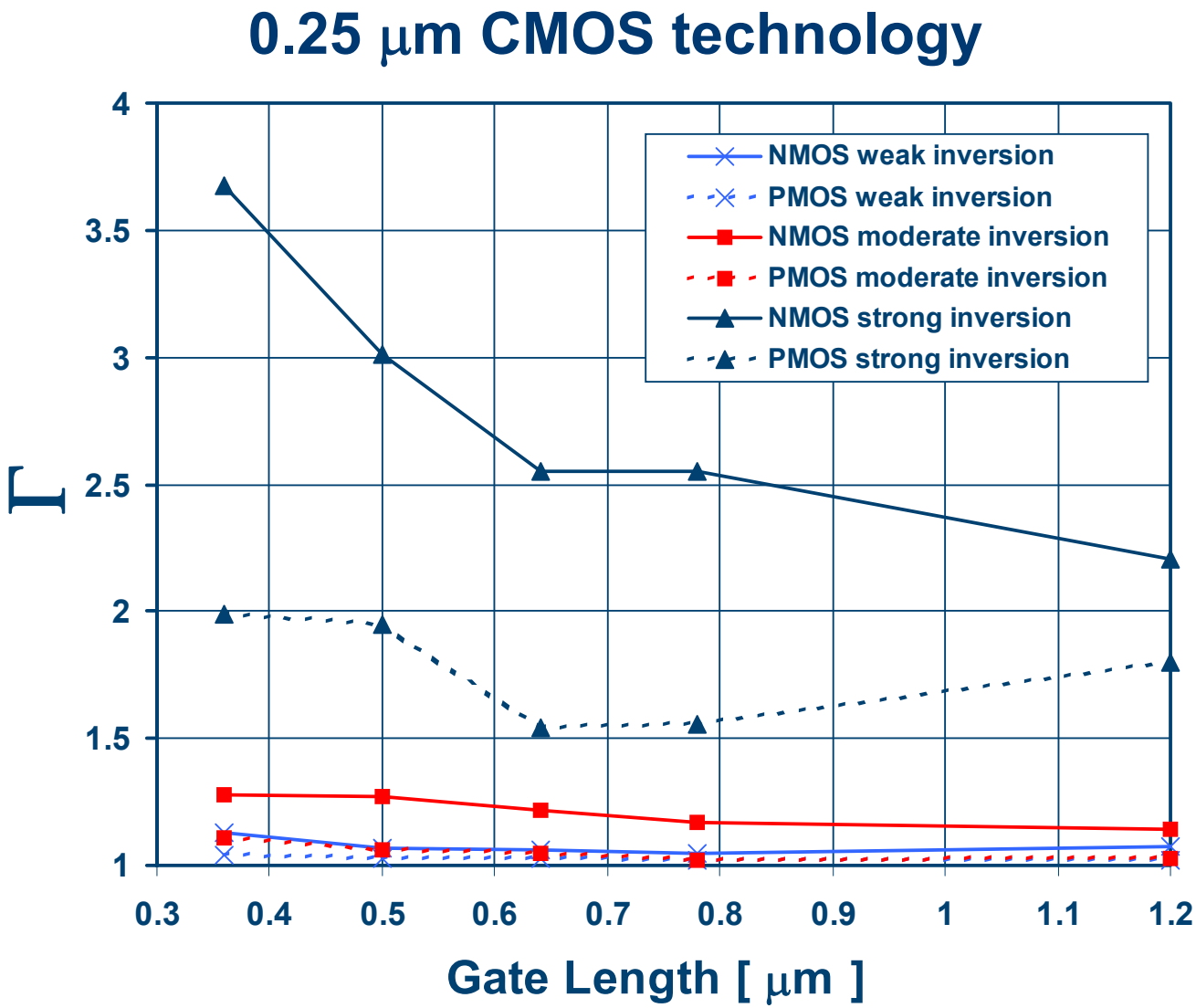
which are NOT negligible values!

D. J. Frank et al., "Device Scaling Limits of Si MOSFETs and Their Application Dependencies", *Proc. IEEE*, vol. 89, no. 3, March 2001, pp. 259-288.

1/f Noise parameter K_a



Excess noise factor Γ



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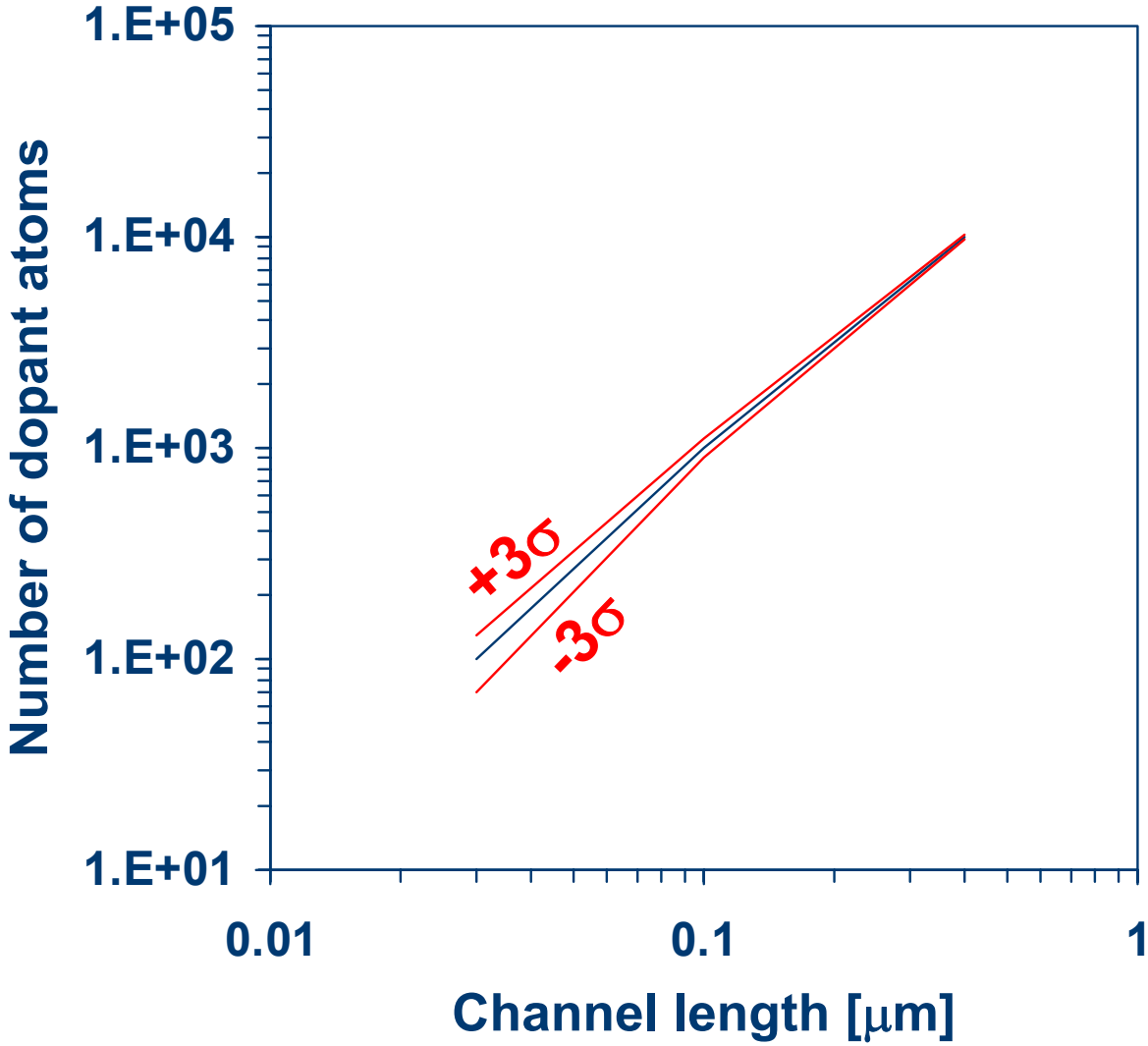
Channel dopant fluctuation



The ion implantation process follows Poisson statistics. Therefore, the uncertainty in the number of dopant implanted is given by the square root of the number.

The error becomes proportionally more important for smaller devices! (=1/√N)

Scaling & dopant fluctuations

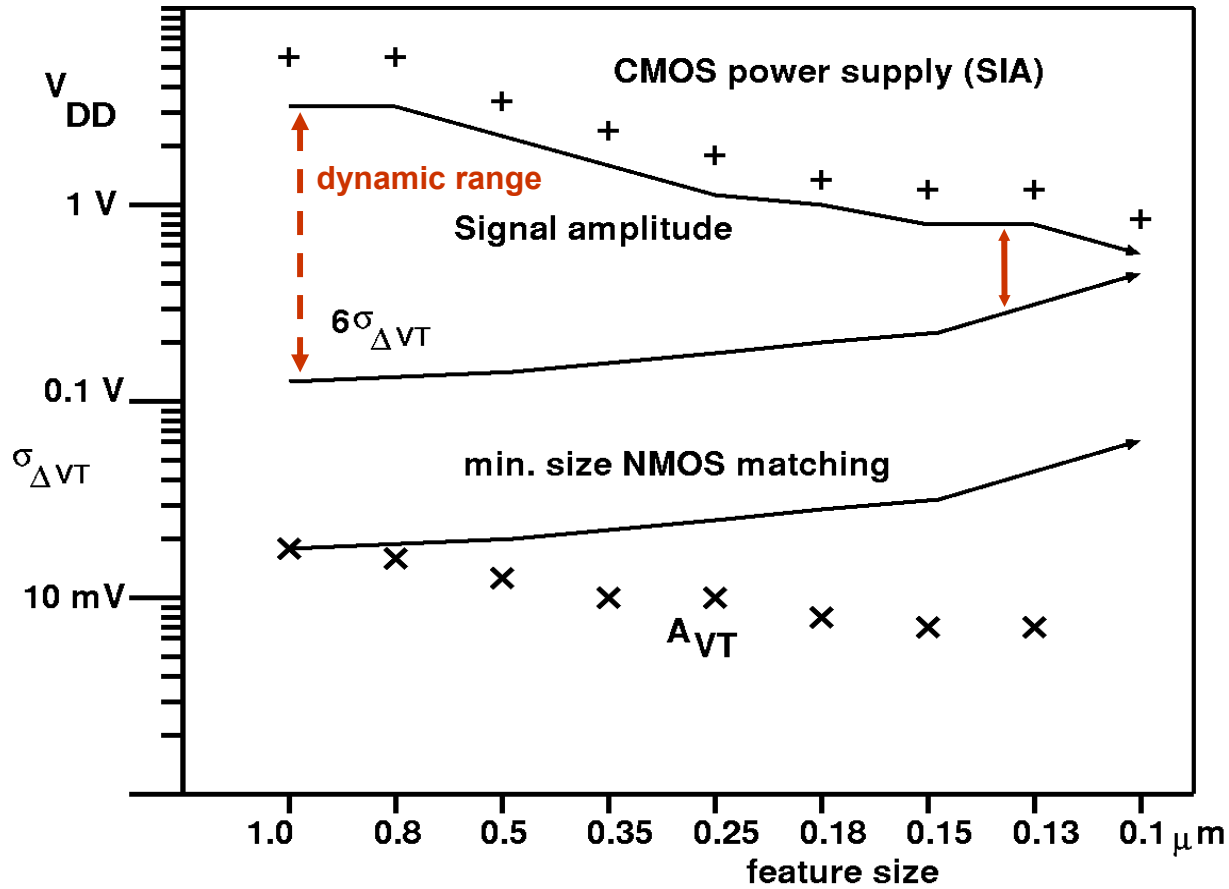
$$\sigma_{\Delta V_{th}} = C \cdot \frac{t_{ox} \cdot \sqrt[4]{N}}{\sqrt{W\,L}}$$

- For the same device dimensions, matching improves
- For minimum size devices, matching might be worse

L_{min} [μm]	t_{ox} [nm]	N_a [cm^{-3}]	A_N / t_{ox} [mV·μm / nm]	A_N [mV·μm]	$\sigma_{\Delta Vth}$ [mV]	$6 \cdot \sigma_{Vth}$ [mV]
1.2	25	$5 \cdot 10^{16}$	0.328	8.2	6.84	29
1	20	$6 \cdot 10^{16}$	0.344	6.9	6.89	29.2
0.8	15	$7.5 \cdot 10^{16}$	0.365	5.5	6.84	29
0.5	10	$1.2 \cdot 10^{17}$	0.414	4.1	8.28	35.1
0.25	5.5	$2.4 \cdot 10^{17}$	0.498	2.7	11	46.5
0.18	4	$3.3 \cdot 10^{17}$	0.542	2.2	12	51.1

P.A. Stolk et al., "Modeling Statistical Dopant Fluctuations in MOS Transistors", *IEEE Trans. Elect. Dev.*, vol. 45, no. 9, Sept. 1998 , pp. 1960-1971.

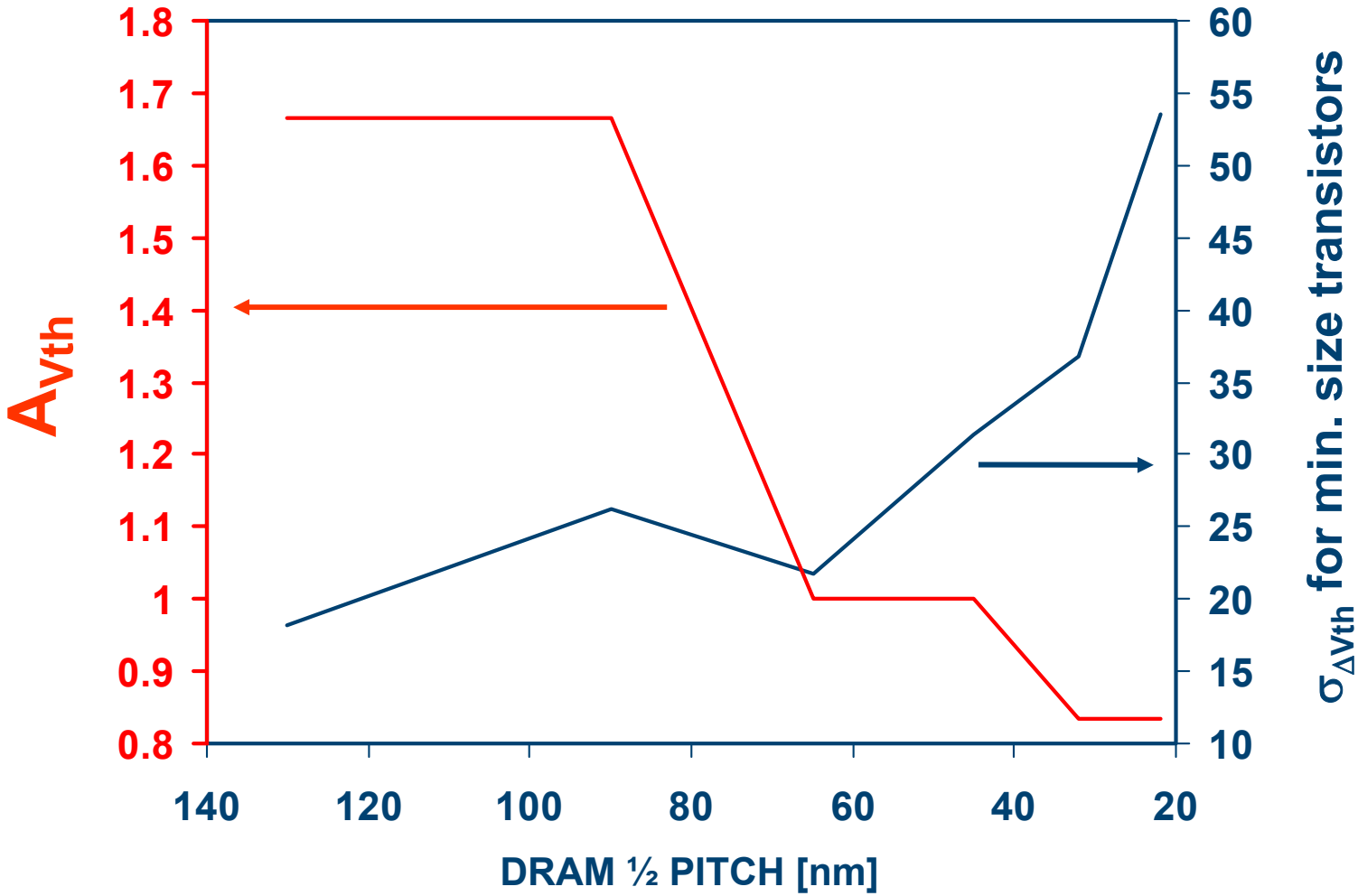
Scaling impact on matching



Matching will have a very important impact on the performance of deep submicron CMOS circuits

M.J.M. Pelgrom et al., "Transistor matching in analog CMOS applications", *Technical Digest of the International Devices Meeting 1998*, pp. 915-918.

Matching data from the Roadmap



Data taken from The International Technology Roadmap for Semiconductors (2001 Edition)

Outline

- Scaling down of CMOS technologies
- How scaling works for devices and interconnections
- Scaling impact on noise
- Scaling impact on matching
- Analog performance of submicron processes
  - Scaling impact on analog performance
  - Analog design in “digital” processes
  - Integrated capacitors
- Substrate noise in mixed-mode integrated circuits

Scaling impact on μC_{ox}

Due to the scaling of the gate oxide thickness, the gate capacitance C_{ox} increases with scaling. This increases the driving capability of the transistor. For a given W/L ratio and a fixed bias current, the transconductance also increases with scaling.

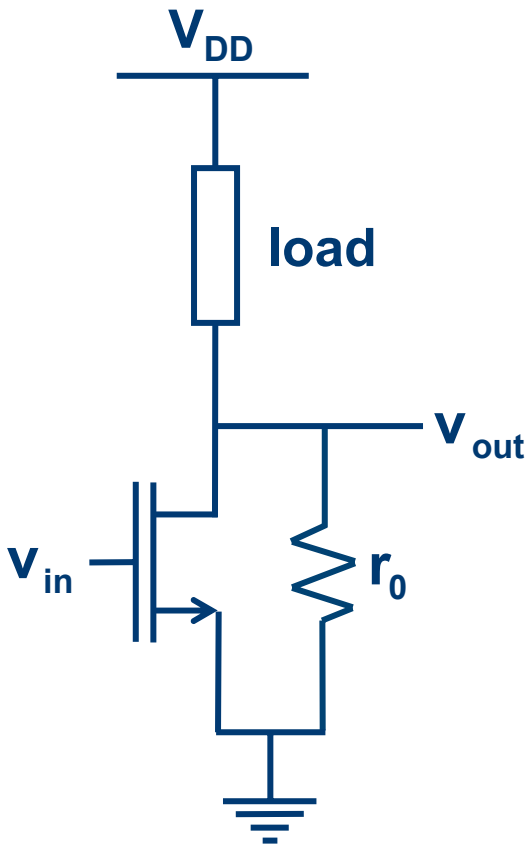
$$g_m = \sqrt{2\frac{\beta}{n} I_{DS}} = \frac{\beta}{n}(V_{GS} - V_T) \qquad \beta = \mu\, C_{ox} \frac{W}{L}$$

The following data are taken from the design manuals of different CMOS technologies

L_{min} [μm]	$t_{ox\_physical}$ [nm]	$t_{ox\_effective}$ [nm]	C_{ox} [fF/μm^2]	μC_{ox} [μA/V^2]
1.2	24	---	1.44	68
0.8	17	---	2.03	90
0.5	10	---	3.45	134
0.25	5.5	6.2	5.5	280
0.13	2.2	3.15	10.9	555

N. D. Arora et al., "Modeling the Polysilicon Depletion Effect and Its Impact on Submicrometer CMOS Circuit Performance", *IEEE Transactions on Electron Devices*, vol. 42, no. 5, May 1995, pp. 935-943.

Intrinsic gain



$$v_{out} = v_{in} \cdot g_m \cdot \frac{r_0 r_{load}}{r_0 + r_{load}}$$

$$\text{Gain} = \frac{v_{out}}{v_{in}} = g_m \cdot \frac{r_0 r_{load}}{r_0 + r_{load}}$$

The quantity $g_m r_0$ is called intrinsic gain of the transistor. It represents the maximum gain obtainable from a single transistor, and it is a very useful figure of merit in analog design.

Scaling impact on the intrinsic gain

$$g_m = \frac{\beta}{n}(V_{GS} - V_T) \qquad \beta = \mu C_{ox} \frac{W}{L} \qquad I_{DS\_SAT} = \frac{\beta}{2n}(V_{GS} - V_T)^2$$

$$\lambda = \frac{1}{V_{DS}} \cdot \frac{\Delta L}{L - \Delta L} \approx \frac{1}{V_{DS}} \cdot \frac{\Delta L}{L} \qquad \Delta L \approx \sqrt{\frac{2\varepsilon_{Si}}{qN_a}} \sqrt{V_{DS}} \qquad g_{out} = \lambda \cdot I_{DS\_SAT}$$

$$r_0 = \frac{1}{g_{out}} = \frac{1}{\lambda \cdot I_{DS\_SAT}} \qquad \text{Intrinsic Gain} = g_m \cdot r_0$$

Supposing to have constant field scaling for the technology, we obtain:

L	W	β	V_{GS}-V_T	g_m	V_{DS}	ΔL	λ	I_{DS_SAT}	g_{out}	r_o	$g_m r_0$
1/α	1/α	α	1/α	1	1/α	1/α	α	1/α	1	1	1
1	1/α	1	1/α	1/α	1/α	1/α	1	$1/\alpha^2$	$1/\alpha^2$	α^2	α
1	1	α	1/α	1	1/α	1/α	1	1/α	1/α	α	α
1/α	α	α^3	1/α	α^2	1/α	1/α	α	α	α^2	$1/\alpha^2$	1

Analog power consumption

t_{ox} scales $\longrightarrow$ V_{DD} must be scaled as well

Min. power consumption for class A analog circuits:

$$P_{min} = 8\,\pi\,kT \cdot SNR \cdot f_{sig} \cdot \frac{V_{DD}}{V_{DD} - \Delta V}$$

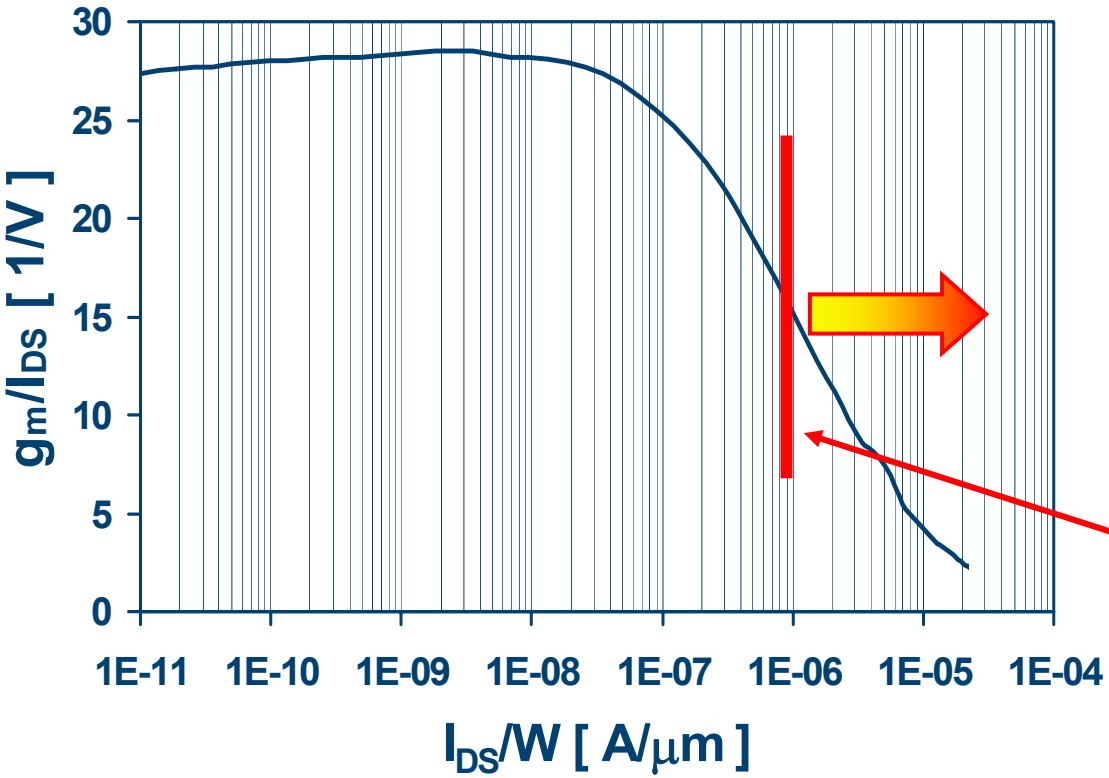
ΔV is the fraction of the V_{DD} not used for signal swing

Optimal analog power/performance trade-off for 0.35 - 0.25 μm technologies

A.-J. Annema, "Analog Circuit Performance and Process Scaling", *IEEE Transactions on Circuit and System II*, vol. 46, no. 6, June 1999, pp. 711-725.

Weak inversion region

t_{ox} scales ⟶ for the same device dimensions the boundary between weak inversion and strong inversion moves towards higher currents



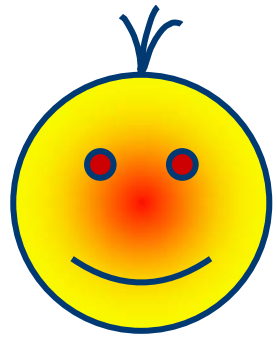
Strong inversion $g_m = \sqrt{2\frac{\beta}{n} I_{DS}}$

Weak inversion $g_m = \frac{I_{DS}}{n\phi_t}$

$I_{DS\_W\_to\_S} = 2\beta n\phi_t^2$

Scaling impact on analog circuits

t_{ox} scales ⟶ for the same device dimensions



- Threshold voltage matching improves $\sigma_{\Delta V_{th}} = \frac{Const \cdot t_{ox}}{\sqrt{W\,L}}$
- 1/f noise decreases $\frac{\overline{v_{in\_1/f}^2}}{\Delta f} = \frac{K_a}{C_{ox}^2\,WL}\frac{1}{f^{\alpha}}$
- Transconductance increases (same current) $g_m = \sqrt{\frac{2}{n}\mu C_{ox}\frac{W}{L}I_{DS}}$
- White noise decreases

Scaling impact on analog circuits

- **New noise mechanisms**
- **Modeling difficulties**
- **Lack of devices for analog design**
- **Reduced signal swing (new architectures needed)**
- **Substrate noise in mixed-signal circuits**
- **Velocity saturation. Critical field: 3 V/μm for electrons, 10 V/μm for holes**

$$g_{m\_vel.sat.} = WC_{ox}v_{sat}$$

Analog design in digital processes

The integrated circuits market is driven by digital circuits, such as memories and microprocessors. This led to an increasing interest in integrating analog circuits together with digital functions in processes optimized for digital circuits, making what it is called a System on a Chip (SoC). This approach has several advantages and disadvantages.

ADVANTAGES:

- Lower wafer cost
- Higher yield
- Higher speed
- Lower power consumption (not always)
- Complex digital functions on chip (DSP)

DISADVANTAGES:

- Low power supplies
- Lack of "analog" components
- Inadequate modeling
  - Output conductance
  - Different inversion regions
- "Digital" noise

• E. A. Vittoz, "The Design of High-Performance Analog Circuits on Digital CMOS Chips", *IEEE JSSC*, vol. 20, no. 3, June 1985, pp. 657-665.
• W. Sansen, "Challenges in Analog IC Design in Submicron CMOS Technologies", *Proceedings of the 1996 IEEE-CAS Region 8 Workshop on Analog and Mixed IC Design*, Pavia, Italy, 13-14 September 1996, pp. 72-78.
• C. Azaredo Leme and J. E. Franca, "Analog-Digital Design in Submicrometric Digital CMOS Technologies", *Proceedings of the 1997 IEEE International Symposium on Circuits and Systems*, Hong Kong, 9-12 June 1997, vol. 1, pp. 453-456.

Analog components availability

Analog design needs high-quality passive components. These are not present in processes optimized for digital design, or at least not in the first stages of the process development. These analog "options" are:

- **High-resistivity poly for resistors**
- **Diffusion resistors**
- **Trimming options**
- **Linear and dense capacitors**
  - **Metal to metal (at least one special metal layer required)**
  - **Metal to poly**
  - **Poly to poly**

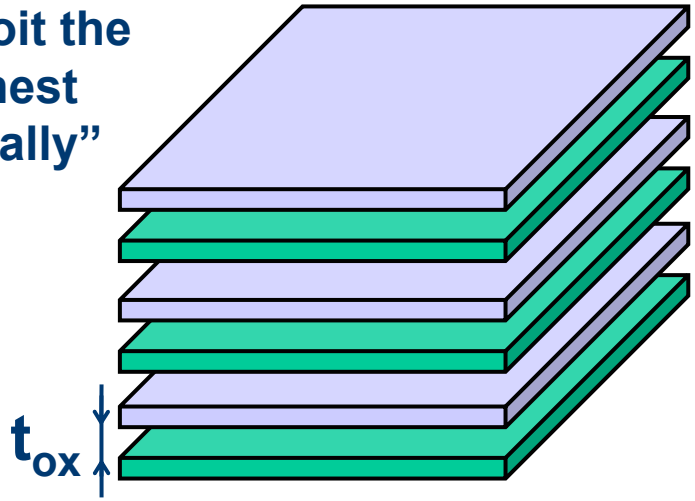
Integrated capacitors

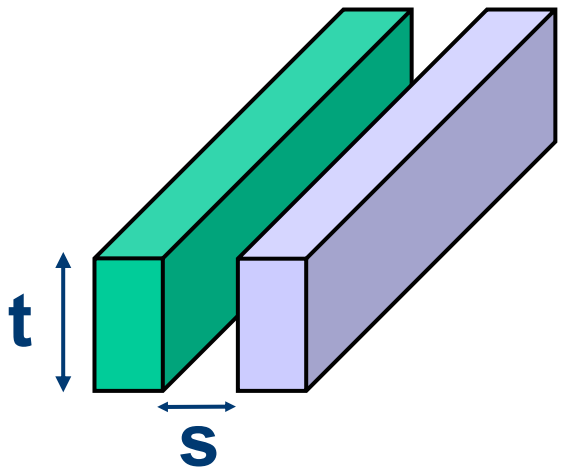
- **High-linearity capacitors can be obtained with metal-to-metal structures. This generally requires adding a special metal layer to the technology, in order to reduce the dielectric thickness between the metal plates. The density reached is generally below 1 fF/μm^2 (not very high…).**
- **Dense capacitors can be obtained exploiting the high capacitance density of the thin gate oxide. This allows having dense and precise capacitors, good matching but very poor linearity. This solution can be adopted in any process.**
- **A third possible solution is suggested by the availability of many interconnection layers. Exploiting the parasitic capacitance between metal wires in a clever way, one can obtain linear capacitors with good matching and linearity and densities up to 1.5 fF/μm^2. These capacitors can be integrated in any process!!**

- A. T. Behr et al., "Harmonic Distortion Caused by Capacitors Implemented with MOSFET Gates", *IEEE JSSC*, vol. 27, no. 10, Oct. 1992, pp. 1470-1475.
- D. B. Slater, Jr. and J. J. Paulos, "Low-Voltage Coefficient Capacitors for VLSI Processes", *IEEE JSSC*, vol. 24, no. 1, February 1989, pp. 165-173.
- J. L. McCreary, "Matching Properties, and Voltage and Temperature Dependence of MOS Capacitors", *IEEE JSSC*, vol. 16, no. 6, Dec. 1981, pp. 608.
- S. Pavan, Y. Tsividis and K. Nagaraj, "Modeling of accumulation MOS capacitors for analog design in digital VLSI processes", *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems*, Orlando, Florida, USA, 30 May – 2 June 1999, vol. 6, pp. 202-205.

Multi-metal-layer capacitors

This solution is a possibility, but it does not exploit the fact that in deep submicron processes the highest parasitic capacitance can be obtained "horizontally" rather than vertically, i.e. $t_{ox} > s$





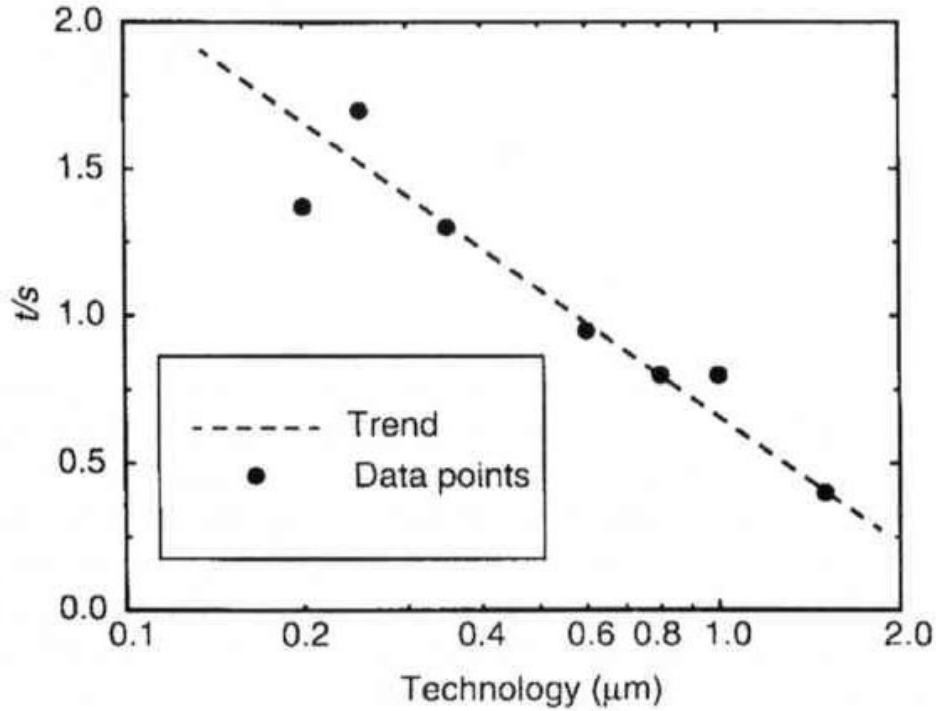
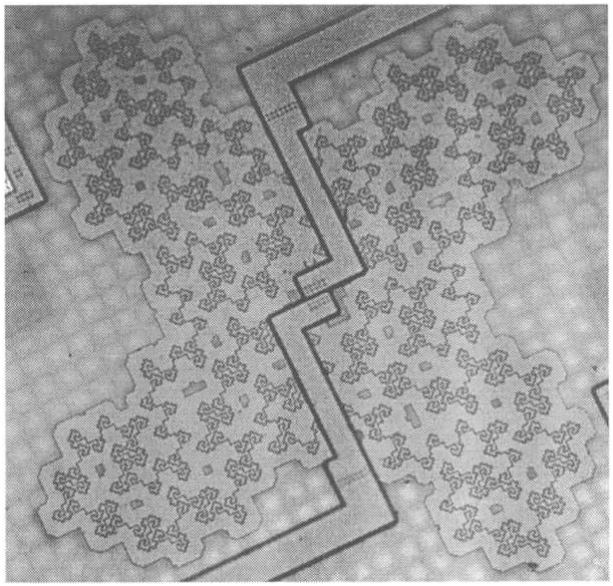
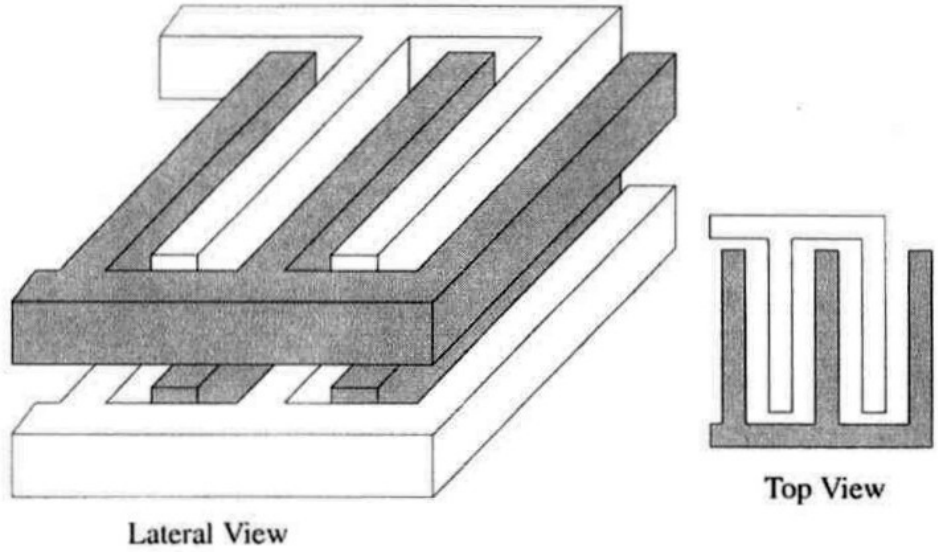


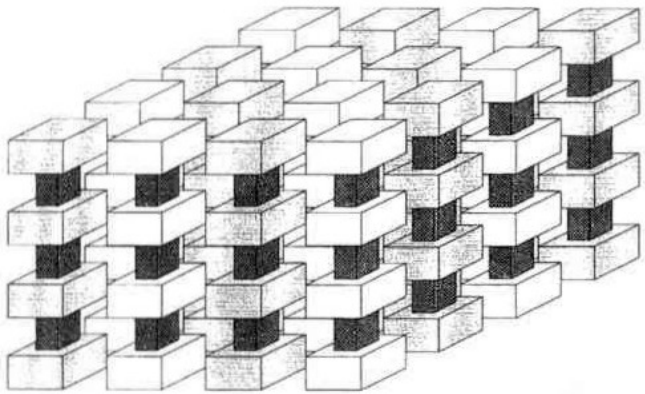
Fig. 3. Ratio of metal thickness to horizontal metal spacing versus technology (channel length).

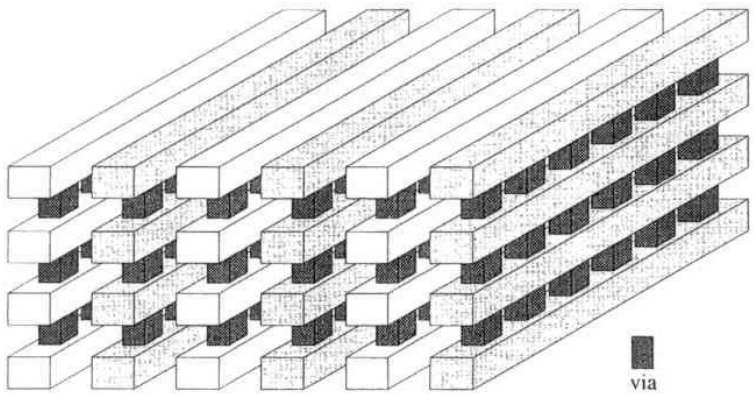
- **Hirad Samavati et al., "Fractal Capacitors", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, December 1998, pp. 2035-2041.**

Multi-metal-layer capacitors







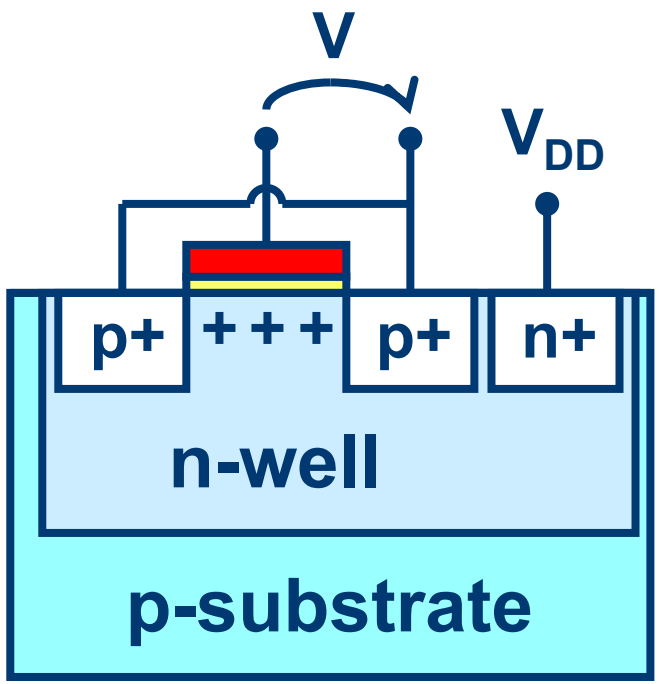


- **Hirad Samavati et al., "Fractal Capacitors", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, December 1998, pp. 2035-2041.**
- **R. Aparicio and A. Hajimiri, "Capacity Limits and Matching Properties of Integrated Capacitors", *IEEE JSSC*, vol. 37, no. 3, March 2002, pp. 384-393.**

MOS capacitors

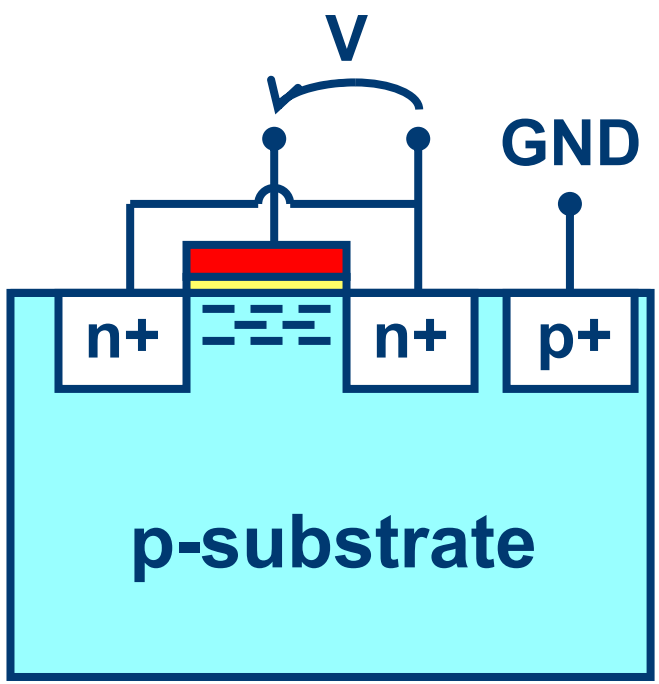
PMOS

Inversion Region



NMOS

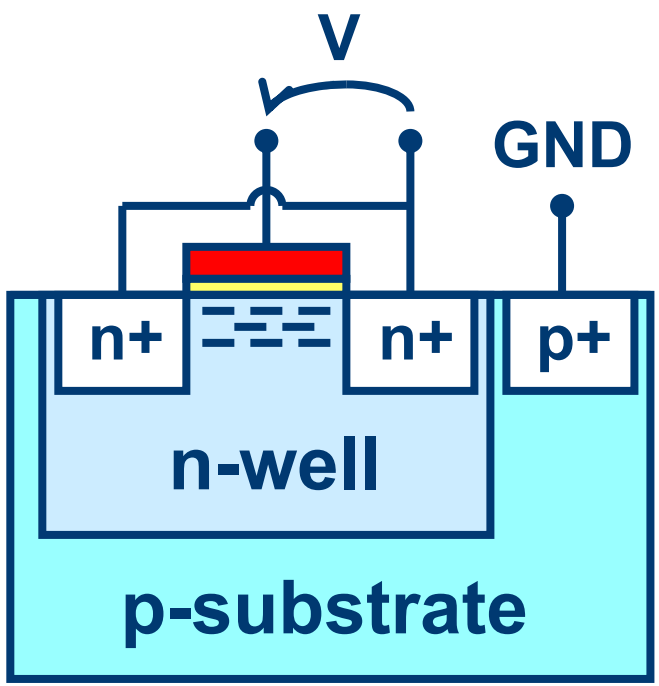
Inversion Region



MOS capacitors

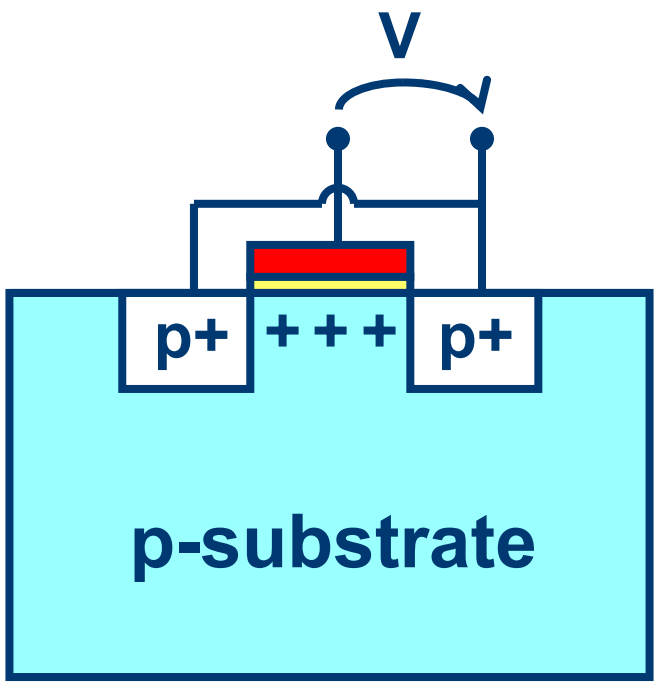
NMOS in an N well

Accumulation Region

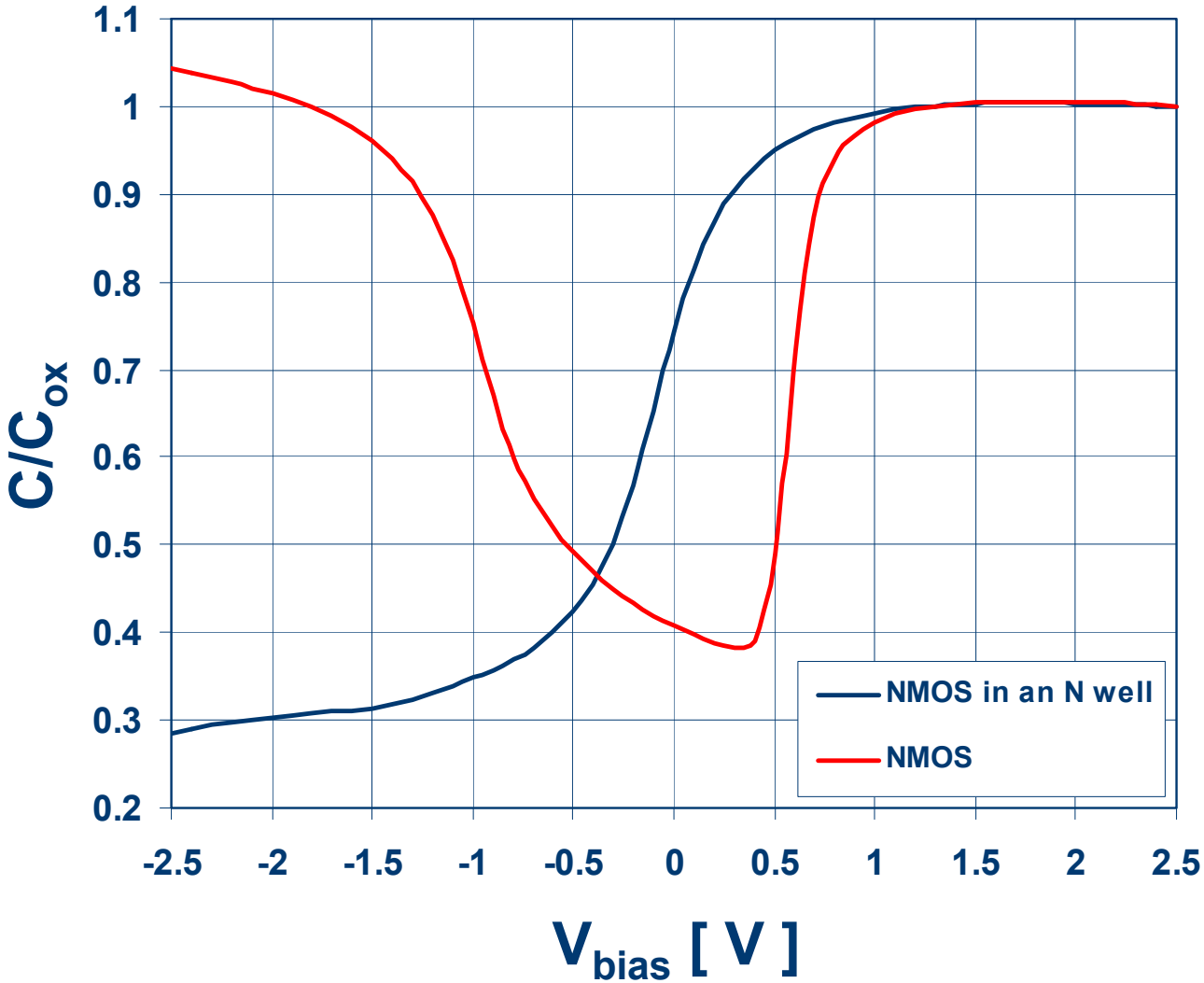


MOS structure

Accumulation Region



C-V characteristics



The NMOS in an N well capacitor is in accumulation for V > 0 V.

The NMOS capacitor is in inversion for V > 0.

Outline

- Scaling down of CMOS technologies
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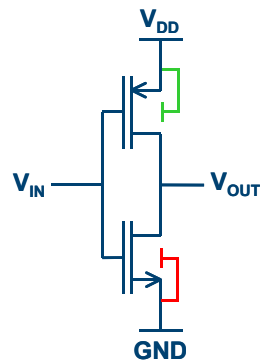
Digital noise in mixed-signal ICs

Integrating analog blocks on the same chip with digital circuits can have some serious implications on the overall performance of the circuit, due to the influence of the "noisy" digital part on the "sensitive" analog part of the chip.

The switching noise originated from the digital circuits can be coupled in the analog part through:

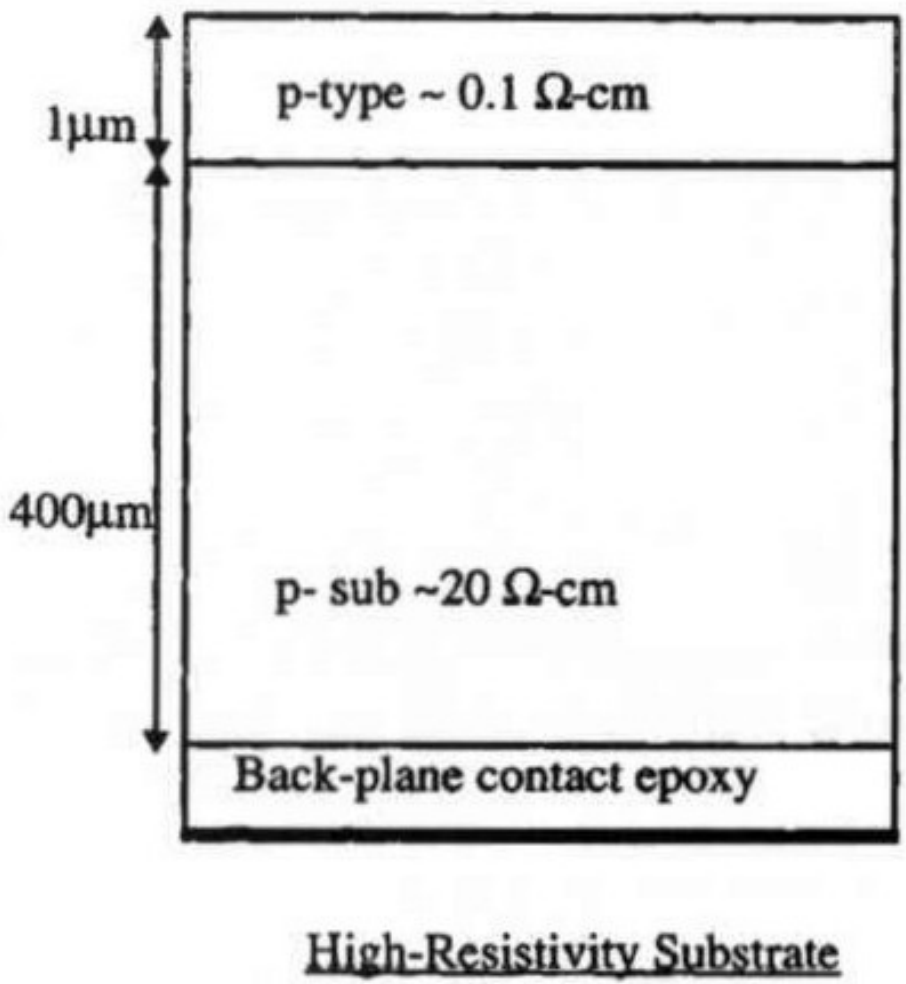
- **The power and ground lines**
- **The parasitic capacitances between interconnection lines**
- **The common substrate**

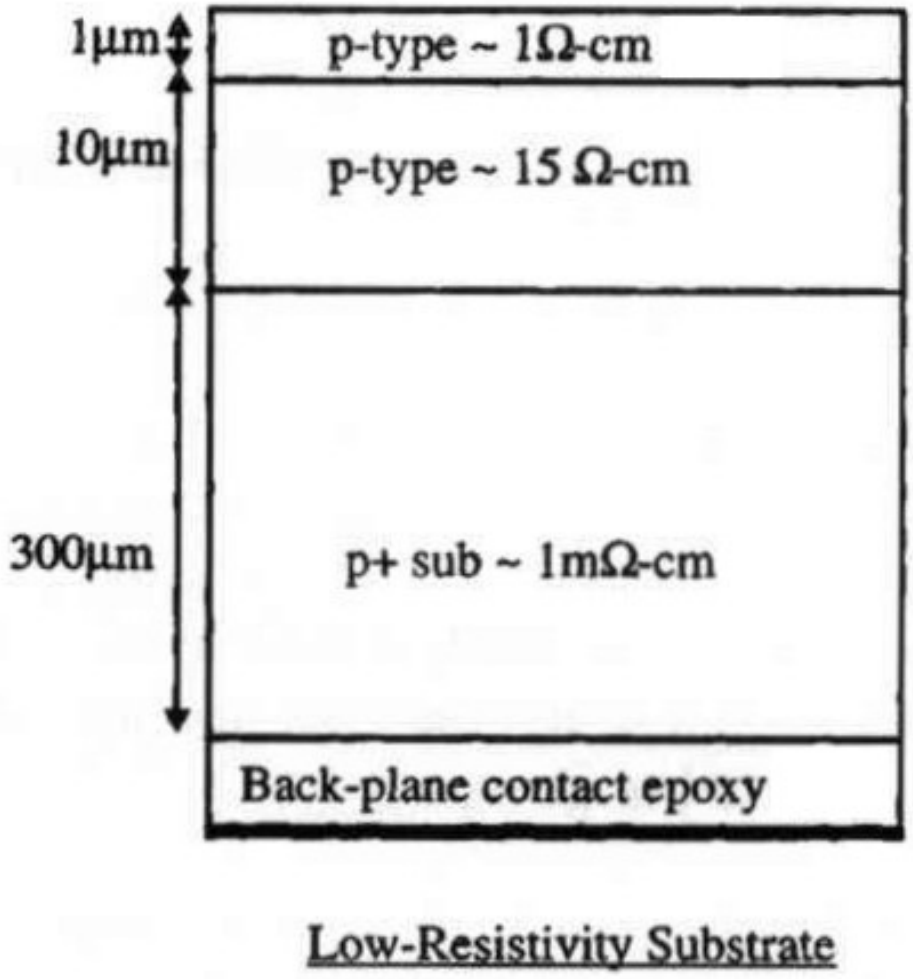


The substrate noise problem is the most difficult to solve.

• A. Samavedam et al., "A Scalable Substrate Noise Coupling Model for Design of Mixed-Signal IC's", *IEEE JSSC*, vol. 35, no. 6, June 2000, pp. 895-904.
• N. K. Verghese and D. J. Allstot, "Computer-Aided Design Considerations for Mixed-Signal Coupling in RF Integrated Circuits", *IEEE JSSC*, vol. 33, no. 3, March 1998, pp. 314-323.
• M. Ingels and M. S. J. Steyaert, "Design Strategies and Decoupling Techniques for Reducing the Effects of Electrical Interference in Mixed-Mode IC's", *IEEE Journal of Solid-State Circuits*, vol. 32, no. 7, July 1997, pp. 1136-1141.

Different types of substrates





R. Gharpurey and R. G. Meyer, "Modeling and Analysis of Substrate Coupling in Integrated Circuits", *IEEE JSSC*, vol. 31, no. 3, 1996, pp. 344-353.

Substrate noise: how to reduce it

To minimize the impact of disturbances coming from the substrate on the sensitive analog blocks, we have mainly three ways:

- **Separate the "noisy" blocks from the "quiet" blocks. This is effective especially in uniform lightly doped substrates. For heavily doped substrates, it is useless to use a separation greater that about 4 times the epitaxial layer thickness.**
- **In n-well processes, p+ guard rings can be used around the different blocks. Unfortunately, this is again effective mainly for lightly doped substrates. Guard rings (both analog and digital) should be biased with separate pins.**
- **The most effective way to reduce substrate noise is to ground the substrate itself in the most "solid" possible way (no inductance between the substrate and ground). This can be done using many ground pins to reduce the inductance, or, even better, having a good contact on the back of the chip (metallization) and gluing the chip with a conductive glue on a solid ground plane.**
- **Separate the ground contact from the substrate contact in the digital logic cells , to avoid to inject the digital switching current directly into the substrate.**

D. K. Su, M. J. Loinaz, S. Masui and B. A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits", *IEEE Journal of Solid-State Circuits*, vol. 28, no. 4, April 1993, pp. 420-429.