The Abdus Salam
International Centre for Theoretical Physics

Workshop on "Physics for Renewable Energy"
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"Cyrstalline Si Technologies"

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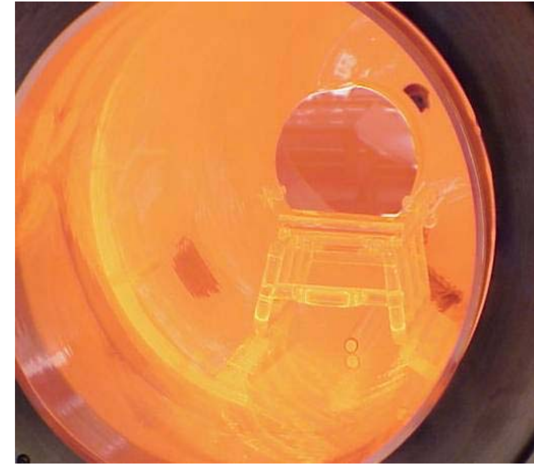
Crystalline Si Technologies

Luisa Pirozzi

Workshop on Physics for
'RENEWABLE ENERGY'

ICTP, Trieste, 19-10-2005



ENEA Crystalline Si PV laboratory – Rome

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-Cell Design

-Silicon technology

- Cell fabrication processes

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-Cell Design

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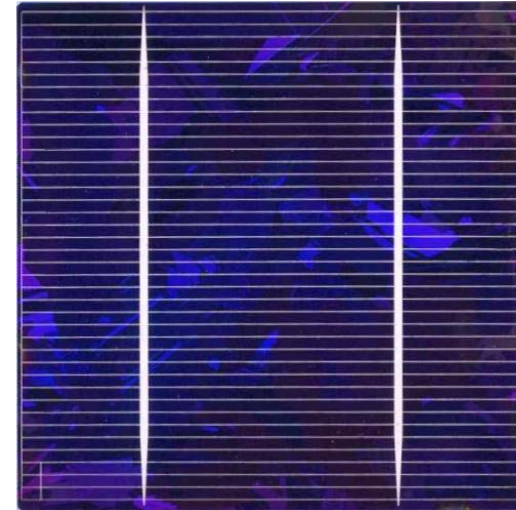
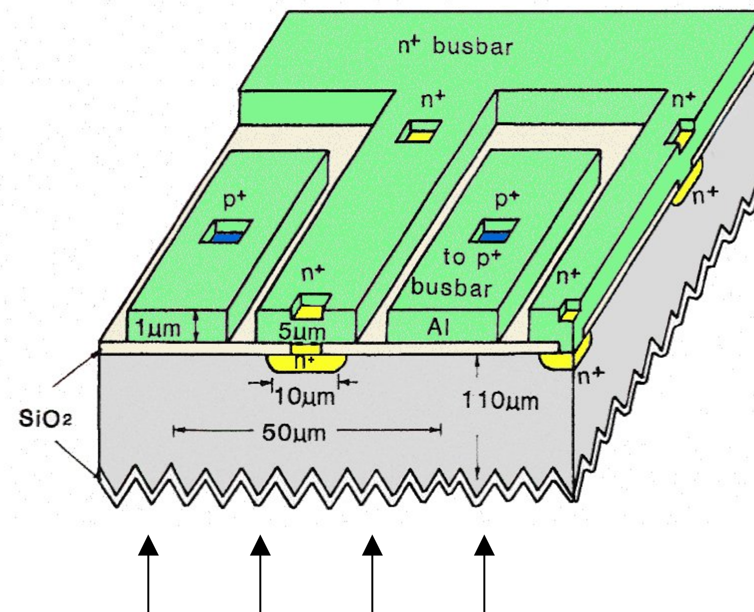
- the **cell design** must take into account its application:

Production-terrestrial, space, concentration,architecture, etc-
Lab- high efficiency, theoretical limit-

- process lay-out:
from three to more than 20 steps
production line –clean room

-Si cells theoretical efficiency limit: 26-28%
-Record efficiency: 24.7%
- Average efficiency (production): 14%





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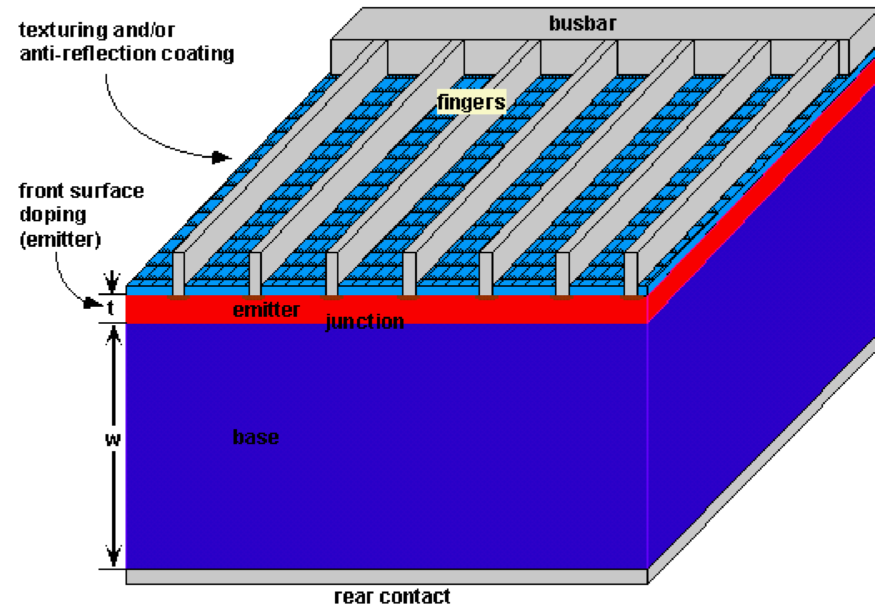
Cell Parameters



- Jsc- short circuit current
  - optical **absorption**
  - base **recombination** (red light)
  - emitter **recombination** (blue light)

- Voc- open circuit voltage
  - bulk **recombination** (Job)
  - emitter **recombination** (Joe)
  - Space charge region (Jor)

- Fill Factor
  - Ideality factor (**n**)
  - Series resistance (**Rs**)
  - Shunt resistance (**Rsh**)

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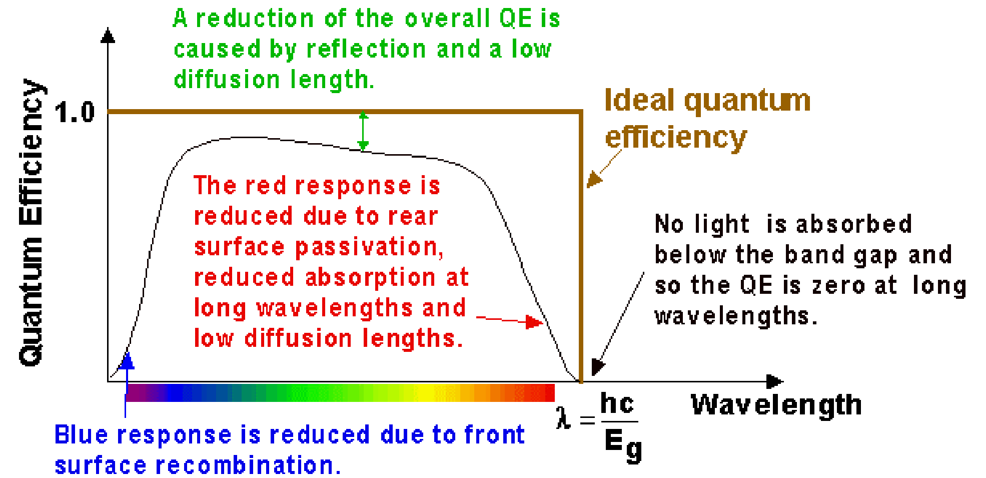
To optimise cell efficiency:

-Increase carriers generation

-Increase carriers ***collection***



Losses: ***recombination***, ***resistive***

***Recombination*:**

Joe: Front surface

Emitter

Jr: space charge region

Job: Base

Back

***Resistive*:**

Bulk

Emitter

Back

Contact grid

Shunt

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Crystalline Silicon

- 85% of world-wide solar cell production

(400 MW, 2.5 $10^9$$)

- Second most abundant element
- Only semiconductor employed in microelectronic industry

Large-scale production/Technology coming from microelectronics

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-Silicon technology

Silicon is the second most abundant element, but about half of the cell cost is due to the substrate.

Silicon production steps:

1) From sand to metallurgical-grade Silicon (MG-Si)

2) MG-Si to semiconductor-grade Silicon (SeG-Si)

3) Crystal growth

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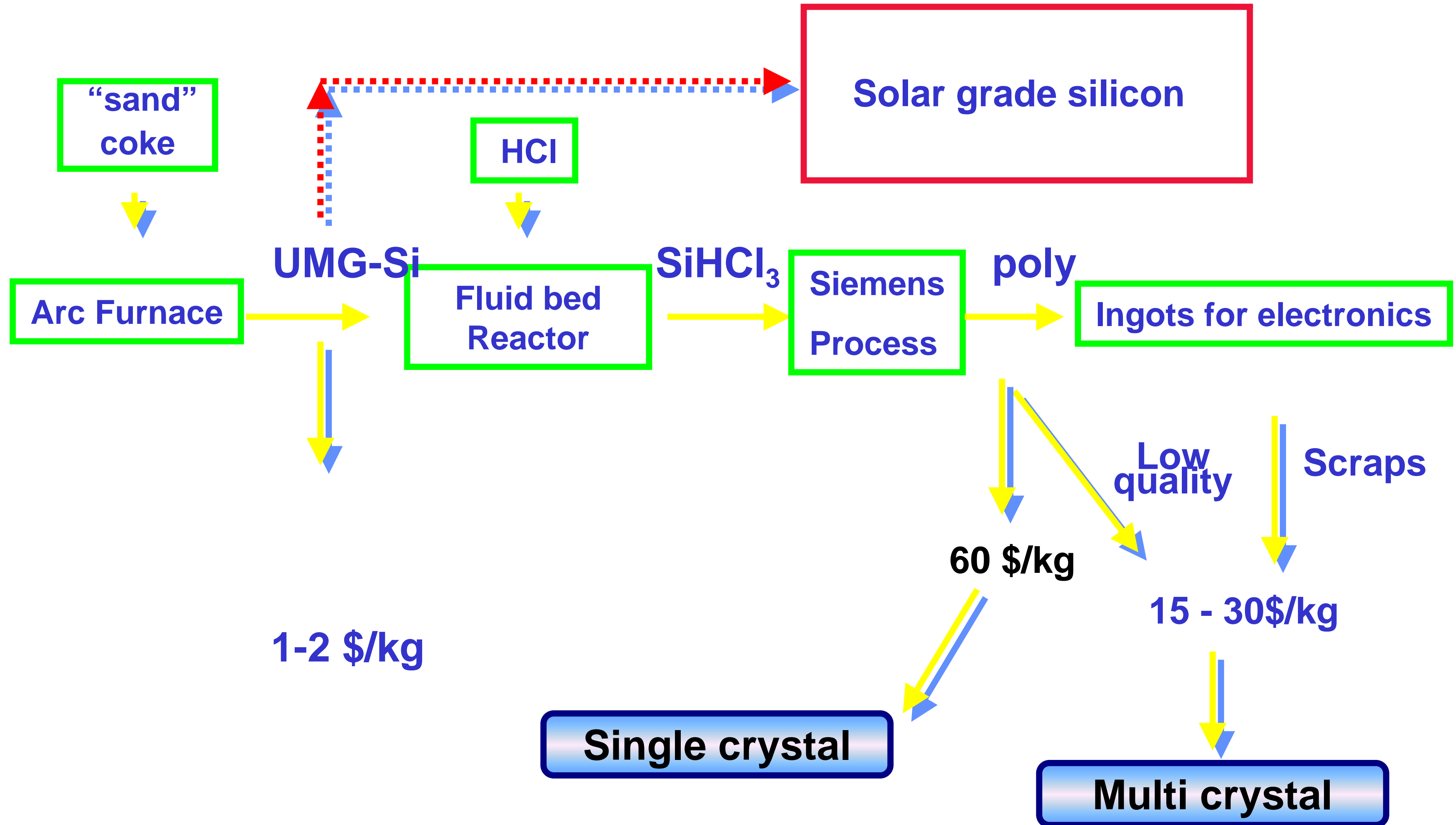
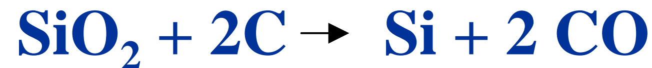
Silicon



Metallurgical-grade Silicon (MG-Si)

- Due to the relative impurity of sand, quartzite – 99% SiO_2- is the starting material.

- Silicon is produced in an Arc Furnace, at T about 1900°C, reducing SiO_2 by Carbon (coke, coal and wood chips):



$$SiO_2 + 2C \rightarrow Si + 2\,CO$$

Liquid silicon is poured into shallow troughs.

MG-Si 98% pure (major impurities Fe and Al).
Cost 1-2$/Kg

Metallurgical-grade Silicon (MG-Si)

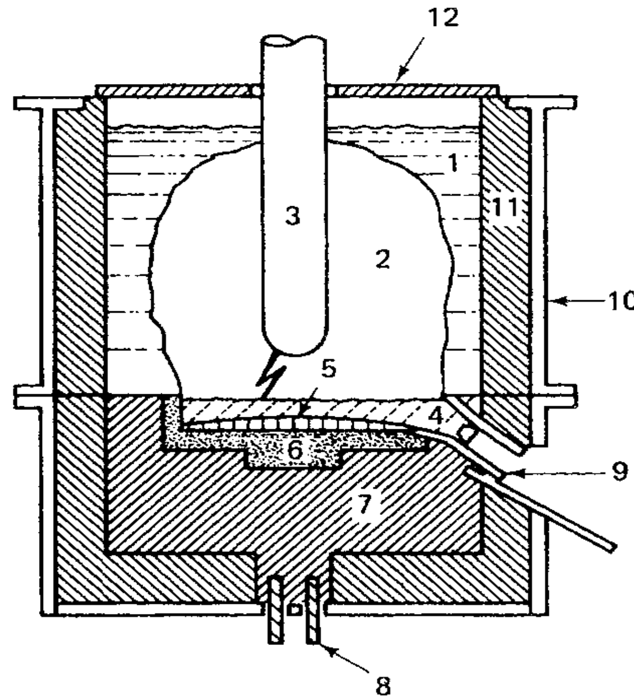


Figure 6.1. Cross section showing typical features of an arc furnace as used to produce metallurgical-grade silicon: 1, carbon and quartz; 2, cavity; 3, electrode; 4, silicon; 5, silicon carbide; 6, hearth; 7, electrode paste, 8, copper electrodes; 9, tapping spout; 10, cast-iron shell; 11, ceramic; 12, graphite lid. (After Ref. 6.1, © 1976 IEEE.)

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Semiconductor grade Si (SeG-Si)

For use in electronics, impurities must be almost completely removed

MG-Si purification (Siemens process)

MG-Si is converted to a volatile compound

$$Si + 3HCl = SiHCl_3 + H_2$$

Trichlorosilane is produced by multiple fractional distillation

SeG-Si is obtained reducing Trichlorosilane by H_2:

$$SiHCl_3 + H_2 = Si + 3HCl$$

Result: polysilicon

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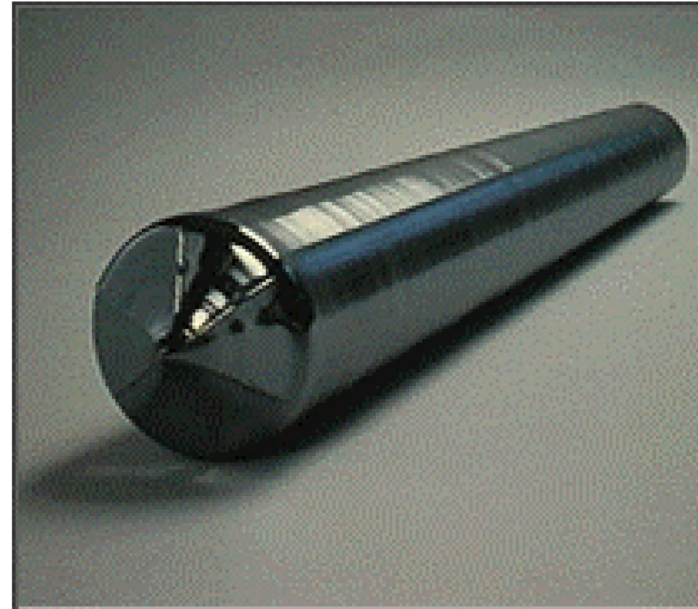
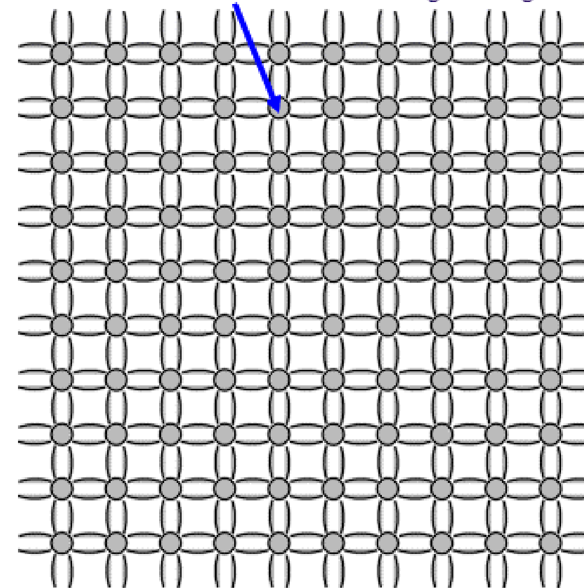
Crystal Growth



-Silicon for electronic industry must be not only impurity-free, but also a single crystal, defect-free.

-Poly-Si is molten and grown into single-crystal ingots:

Czochralsky (CZ)
Floating Zone (FZ)



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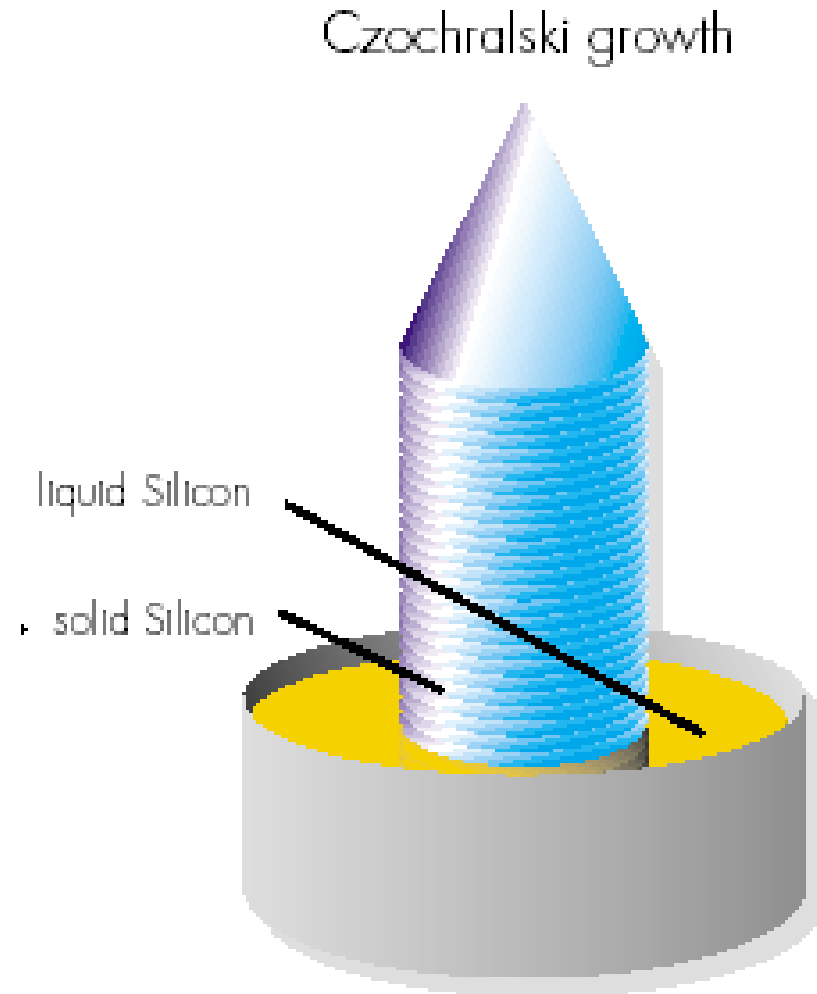
Czochralsky (CZ) method

-SeG polycrystalline Si is molten in a crucible, at T=1410 °C

-A crystal seed is dipped into the molten Si and pulled slowly out of the melt in the vertical direction while rotating:
crystallization at solid/liquid interface

- SeG- Si residual impurities are confined in liquid phase

- dopants (B, P) can be added to the melt
- L_d=200 µm τ=15 µsec



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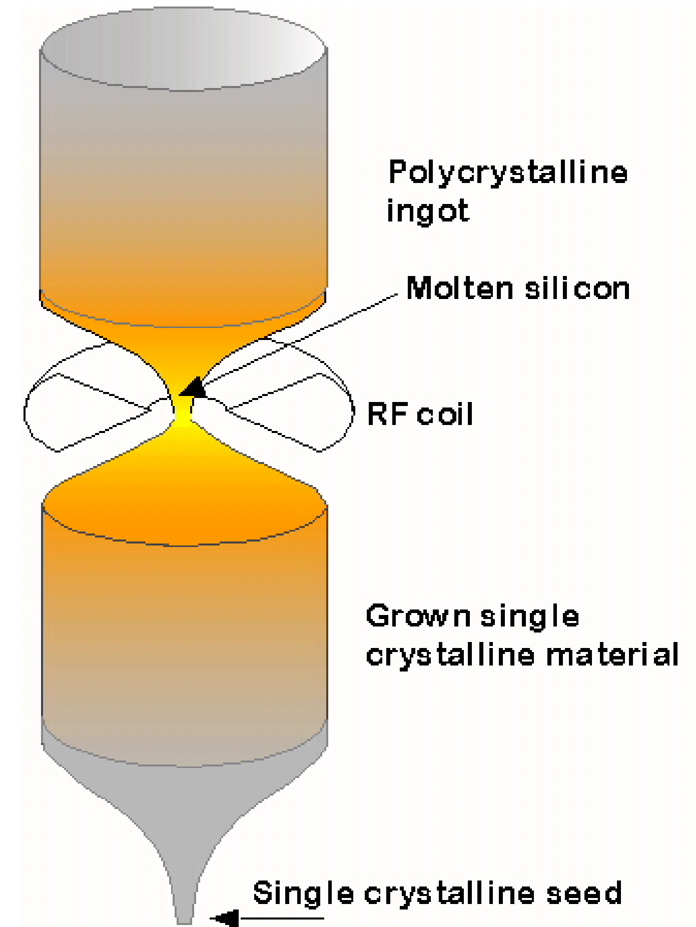
Floating Zone (FZ) Method

-A zone of molten Si is slowly passed along the length of a poly-Si ingot.

-Material melts at one boudary and recrystallizes at the other.

-High purity regrown Si crystal: no crucible, liquid region prevents impurity from entering the growing crystal

-L_d>500 μm τ>100 μsec



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•Microelectronics	1 Si wafer for	$>10^6$ chips
•Photovoltaic	1 Si wafer for	1,5Wp; 1,5KWh/year

•PV application requirements much less severe than in electronics:
-impurity levels
-carriers transport properties

•Silicon especially developed for PV:

Multi-crystalline Si   Ribbon   Solar grade Si

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Multi-crystalline Si

-Crystalline grains random oriented.

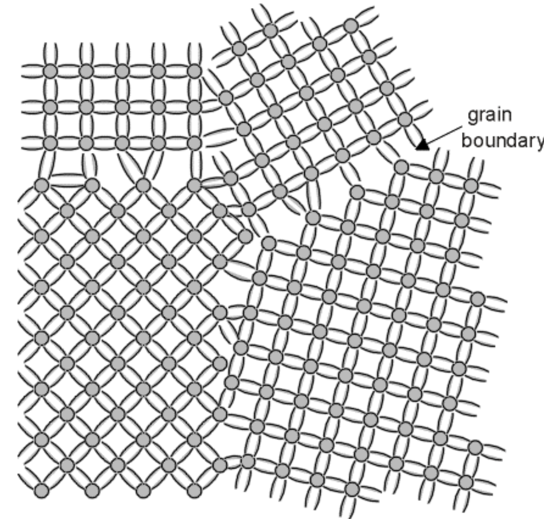
-Grain boundaries: recombination centers - shunt paths for current.

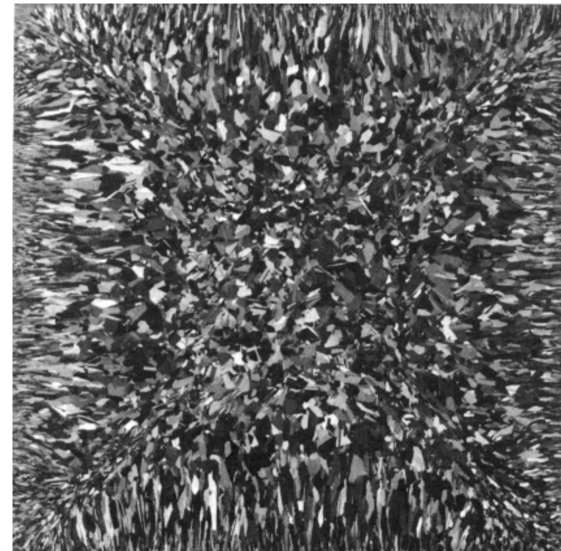
-Columnar structures and large grains (some mm): comparable to single-crystal

$L_d > 150\ \mu m \quad \tau > 10\ \mu sec$

-Production less expensive: 15-30$/kg

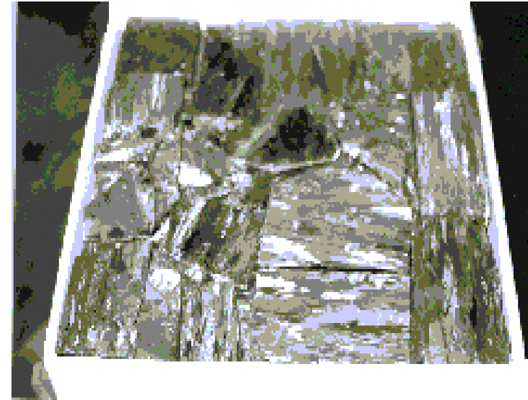
-55% Si cells production on mc-Si (record EFF: 19,8%)





Multi-crystalline Silicon

Casting



-starting material: scraps of ingots for microelectronics, molten in a quartz crucible.

- DS method:
Solidification starts from the bottom: columnar ingot growth.

L_d 200 μm τ >10 μsec

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Ribbon

- Almost half of the material is lost during wafering.

•Silicon is grown in ribbons (250-300 μm)

-EFG method (Edge-defined-Film-fed-Growth):

Molten Silicon moves up the interior of a grafite die by capillarity.

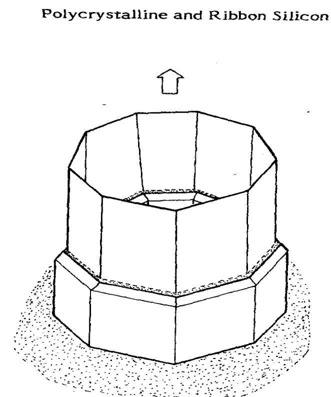
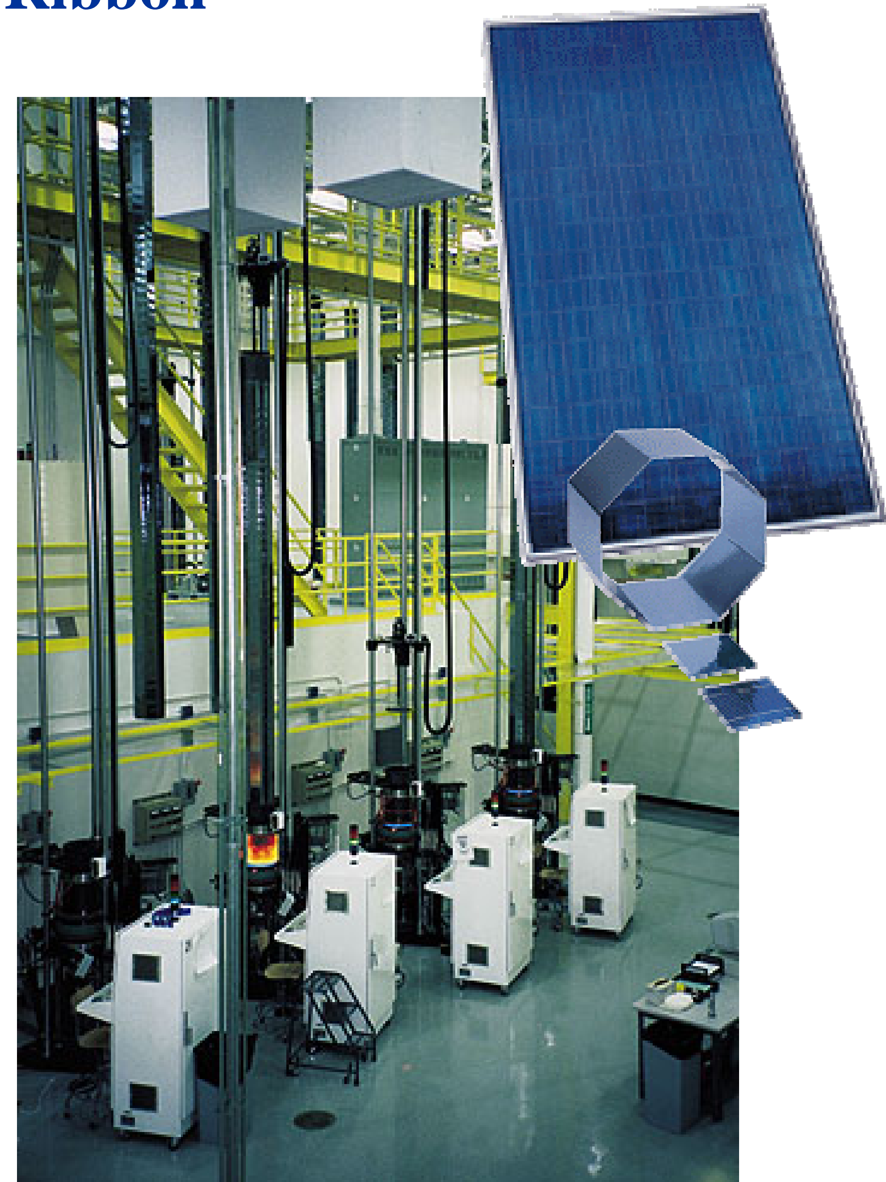


Figure 11.1
Growth of a Nonagonal Ribbon of Silicon using the Edge-Defined Film-Fed Growth (EFG) Method [11.4].



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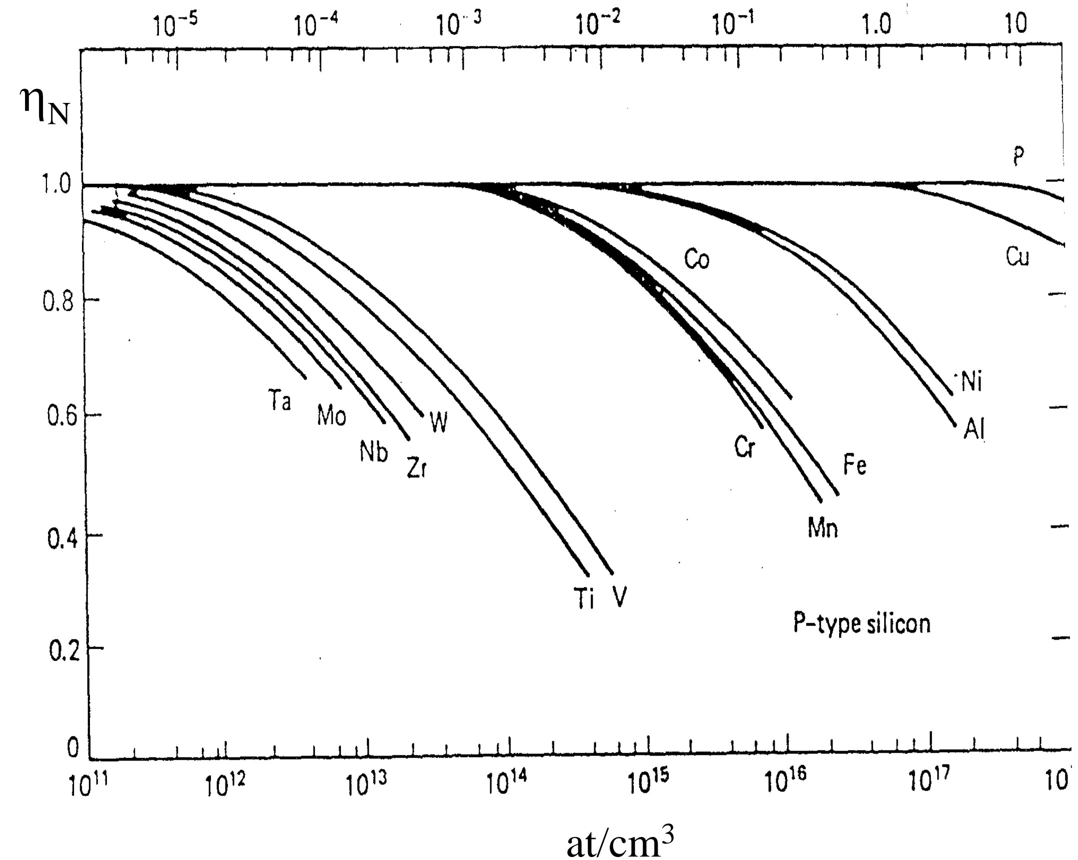
solar grade Silicon

-some metallic impurities can be present in concentrations>$10^{15}/cm^3$ (100 times > SeG-Si)

-Preparation of Silane (SiH_4) from metallurgical grade Si

-Deposition of Si from SiH_4



-Cell fabrication processes

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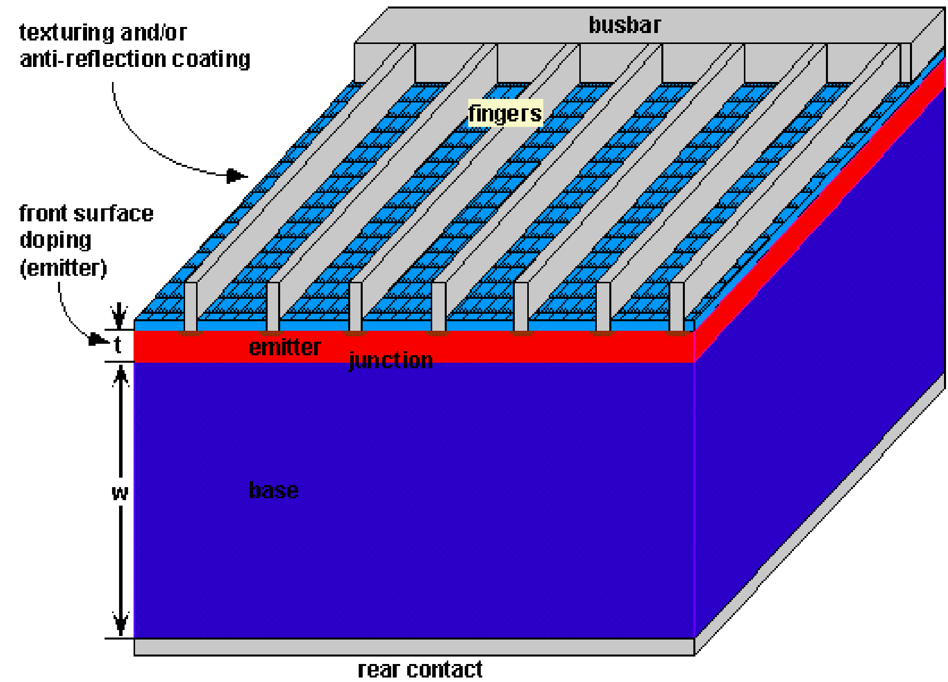
Emitter formation

Ohmic Contacts

Anti Reflection treatments



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Emitter

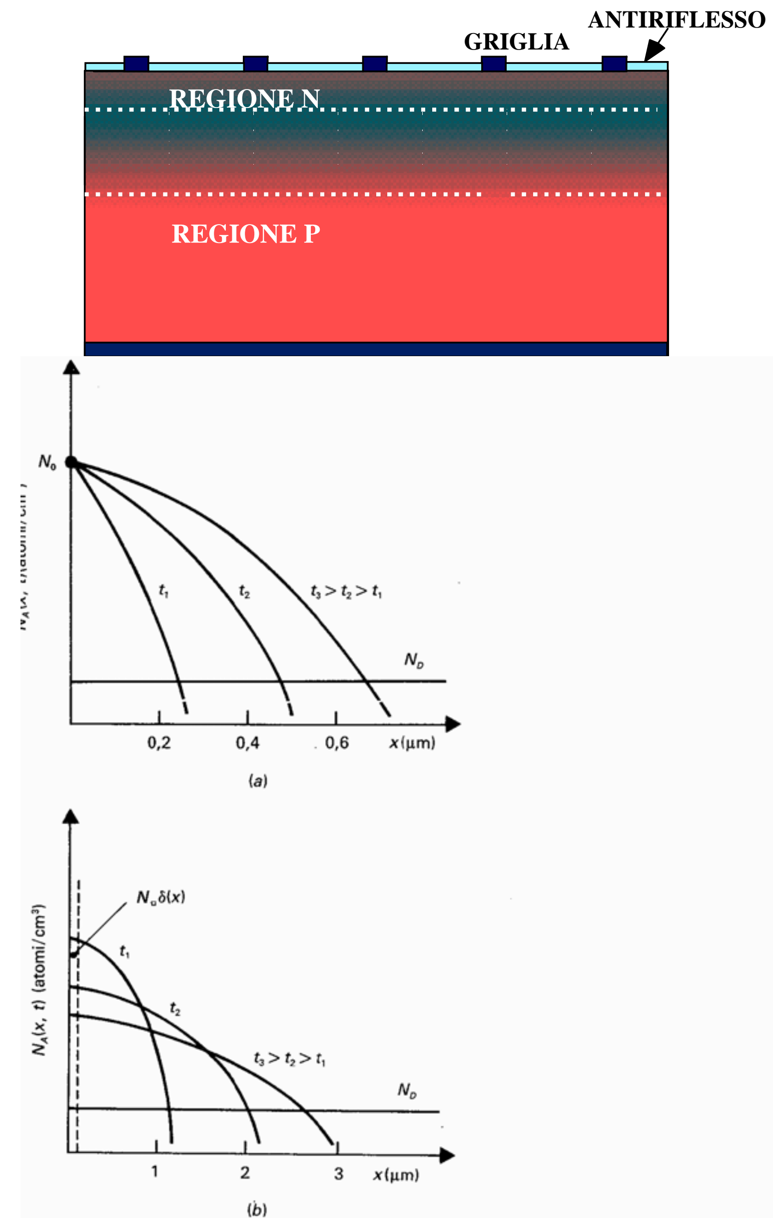
•photogeneration in blue region of spectrum
•collection of photogenerated carriers

shallow, lightly doped, passivated (low recombination)

•Contribution to Series Resistance:

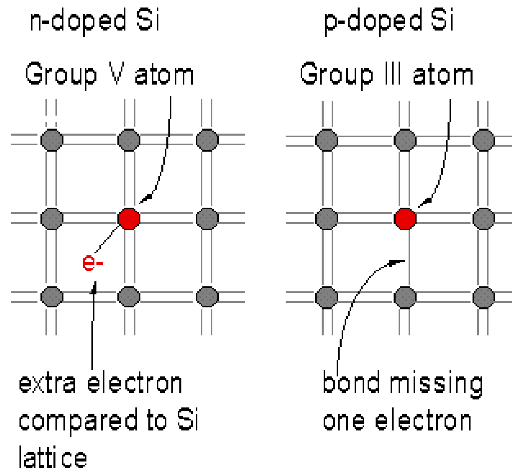
deep, heavily doped

•Compromise: junction profile

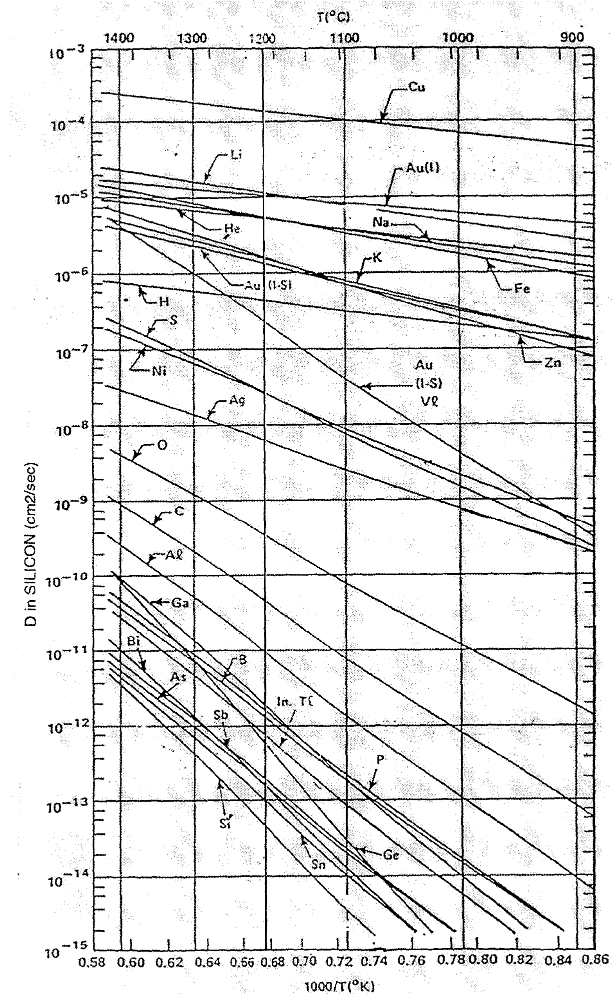


igura 2.4
rogaggio per diffusione termica: (a) da sorgente infinita; (b) da sorgente finita superficiale.

n/p Junction

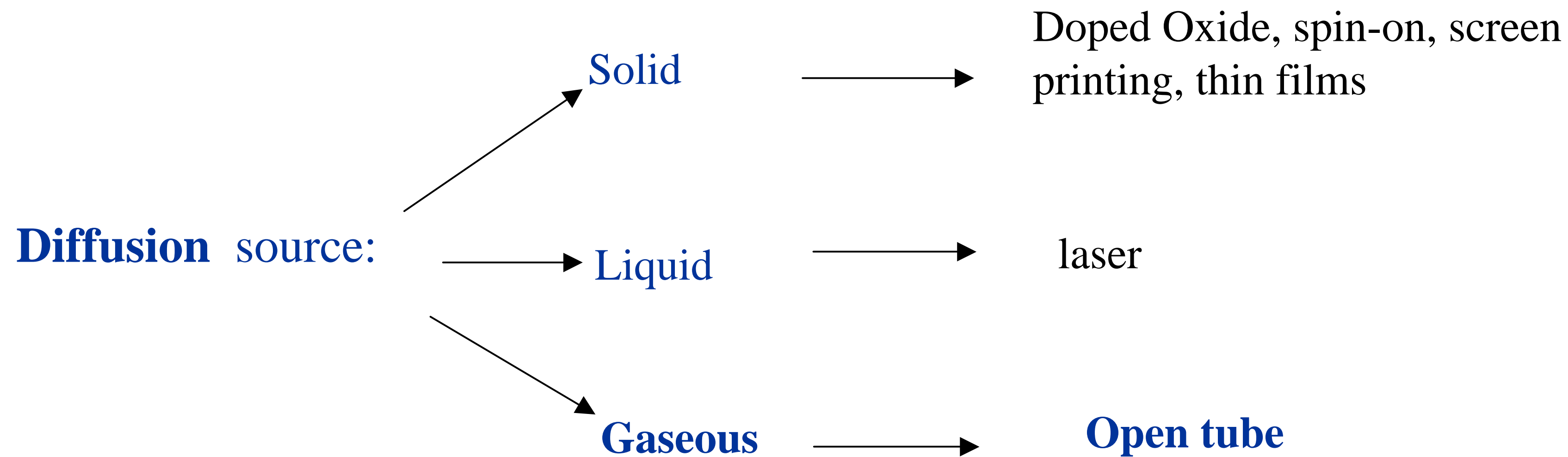


n type (donors)	p type (acceptors)
Phosphorus	Boron
Arsenic	Aluminum
Antimony	Gallium



-**thermal diffusion** of dopant atoms into the silicon (p doped during growth)

Phosphorus thermal Diffusion in Silicon



-Phosphorus: most used

Fick laws: I) $J = -D \, grad \, C$ II) $\delta C / \delta t = D \, \delta^2 C / \delta x^2$

J = flux

C = concentration

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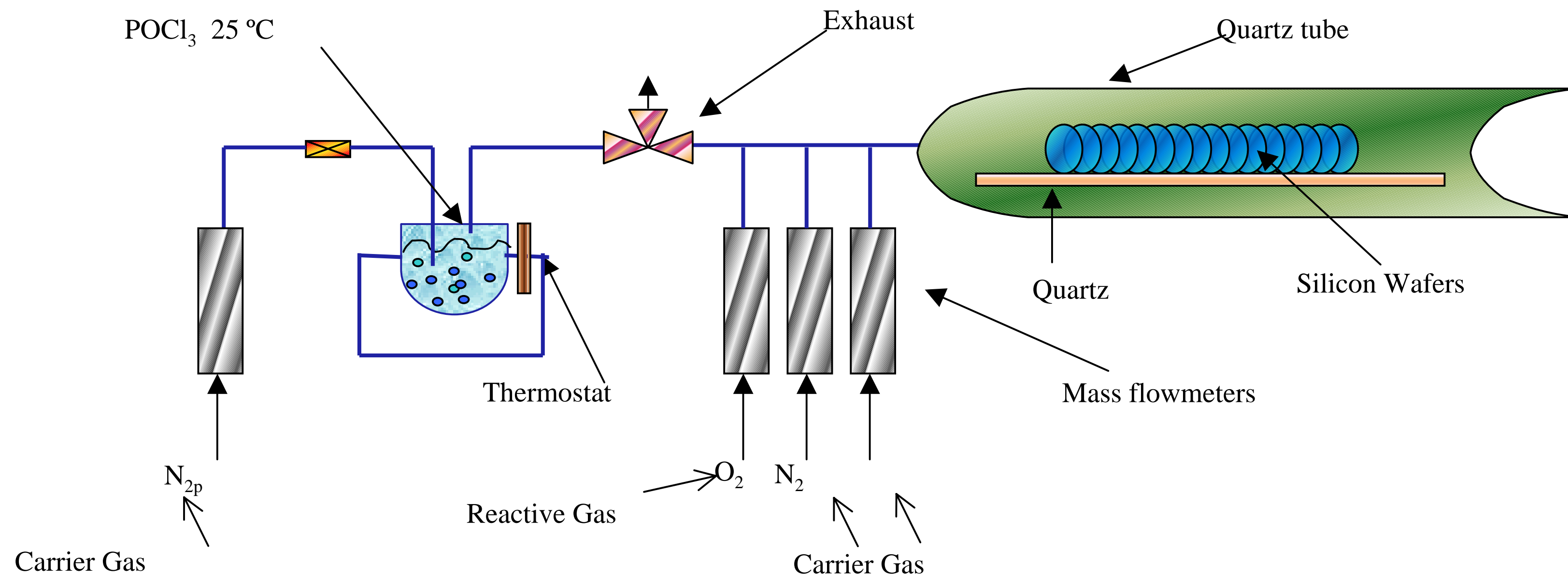

“open tube” diffusion:

a) Predeposition on wafer surface
b) Drive-in: P atoms diffusion

T: 800-1000 °C; N_2 and O_2

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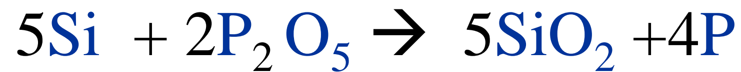
Source: $POCl_3$

$$2POCl_3 + 3/2O_2 \rightarrow P_2O_5 + 3Cl_2$$

$$Si + O_2 \rightarrow SiO_2$$



$$5Si + 2P_2O_5 \rightarrow 5SiO_2 + 4P$$

SiO_2 : better control of diffusion process

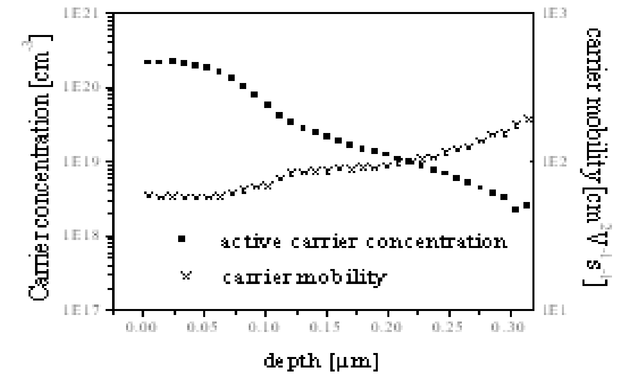


Fig. 3 Electron concentration and mobility as a function of depth in the n-type emitter of a silicon wafer diffused with phosphor.

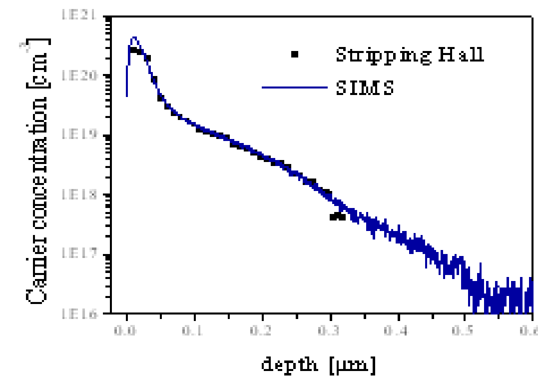


Fig. 4 Comparison of stripping Hall and secondary ion mass spectrometer measurements (SIMS) on a diffused n-type emitter. The stripping Hall results give the total number of electrically active donors. The SIMS measurements give the total number of diffused phosphor atoms, electrically active or not.

•**Temperature**, **time duration** and **dopant source** determine:

-P surface concentration,$\mathbf{C_s}$

-$\mathbf{x_j}$=junction depth

-resistance and τ of diffused region

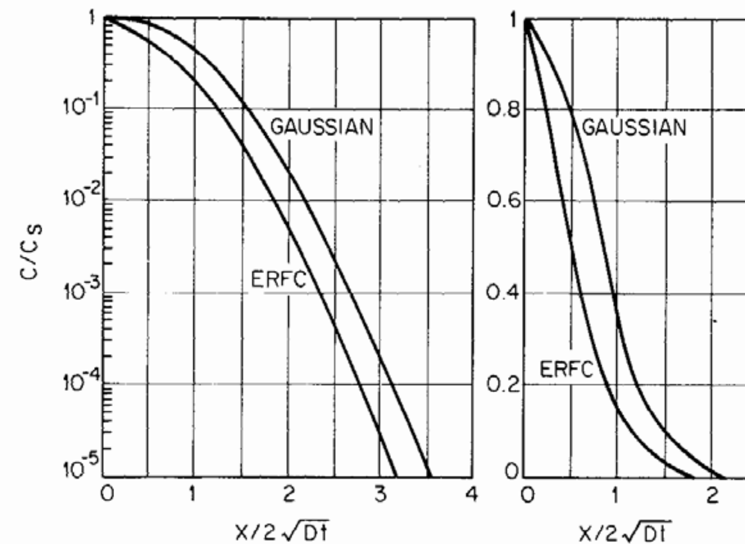
- when Cs > P solubility limit (10^{21} at/cm^3 a 1000ºC)

dead layer: high defect density region , low τ

-Concentration profile:

$$C(x,\mathbf{t})=C_s\ \mathrm{erfc}(x/2\sqrt{D\mathbf{t}})$$

$D= D_0 \exp(-\Delta E/K\mathbf{T})$ P diffusion coefficient in Si (10^{-14} cm^2/sec a 980 ºC)

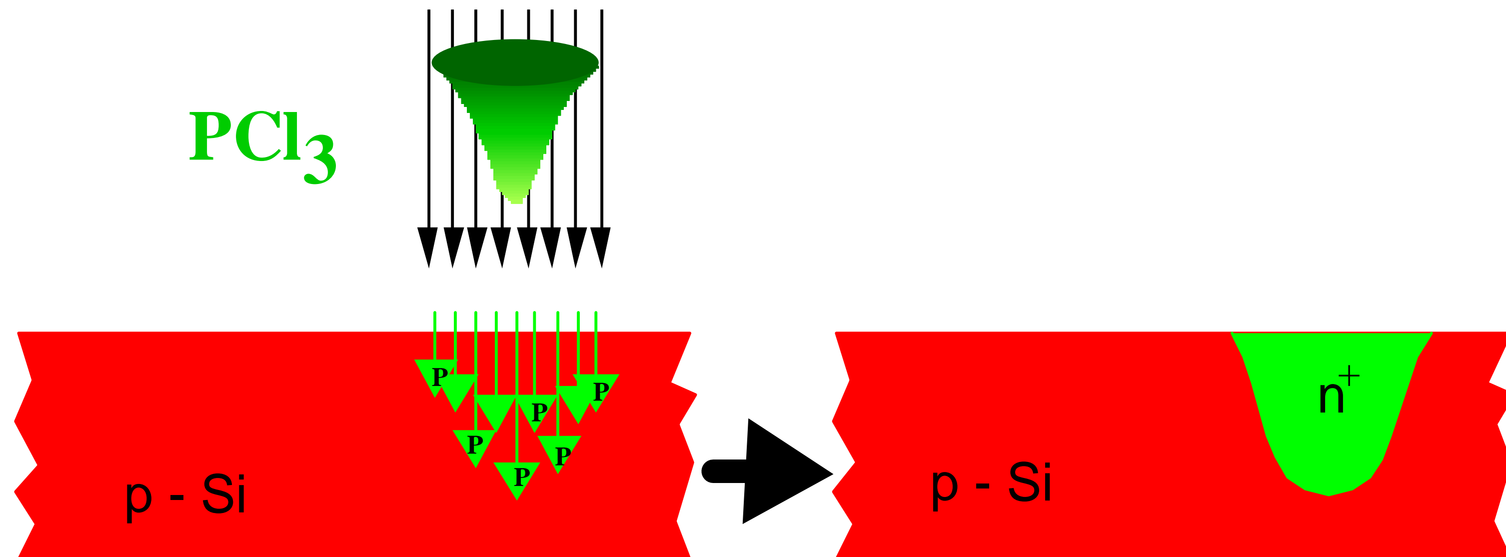


3 Normalized concentration versus normalized distance for Gaussian and error tion complement (erfc) distributions plotted in both semilog and linear scales. (After

LASER ASSISTED DOPING

laser beam creates dopant atoms (PCl_3 pyrolysis or solid source) and simultaneously induces **melting** of silicon: dopant liquid phase diffusion.

Localized process, low thermal budget
Fast diffusion kinetics



SURFACE PASSIVATION

•Surface: critical discontinuity in the crystal structure
-High density of allowed states within the forbidden gap

•Silicon: surface-state density reduced growing passivanting oxide
-interface between oxide and Si moves towards bulk

•**Thermal Oxidation**: open tube, in O_2 at T 800-1000 °C

•low T alternative: SiN layer

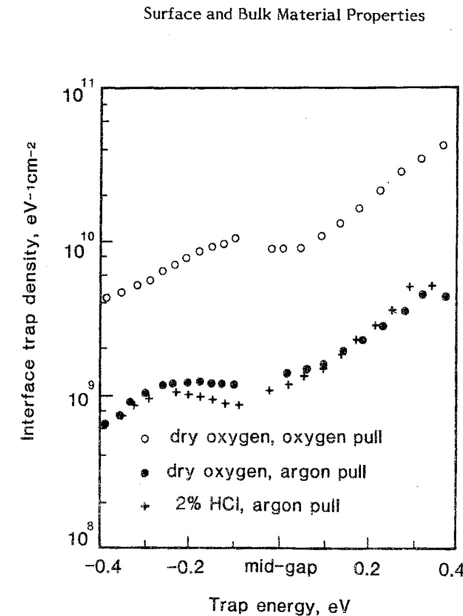
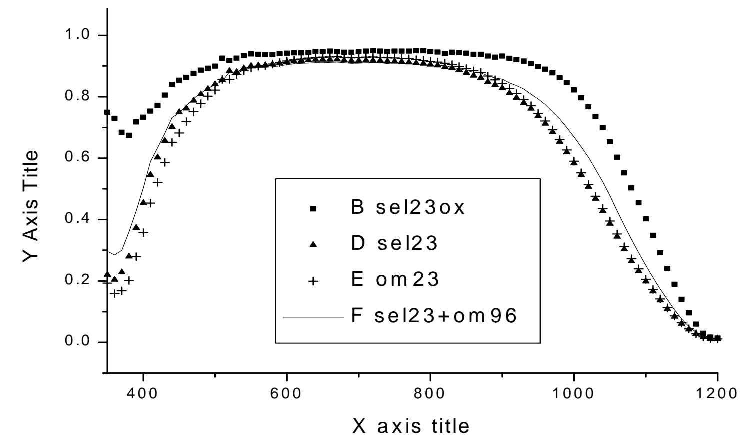
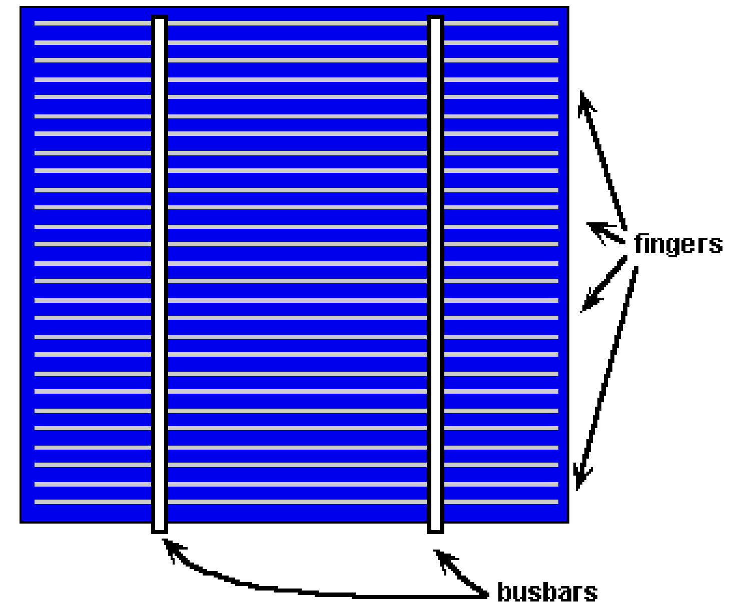


Figure 7.1
Surface State (Interface Trap) Density Measured at the Interface between Silicon and its Oxide. The oxide was grown at 1000°C in the ambients shown (after Eades & Swanson [7.3]).

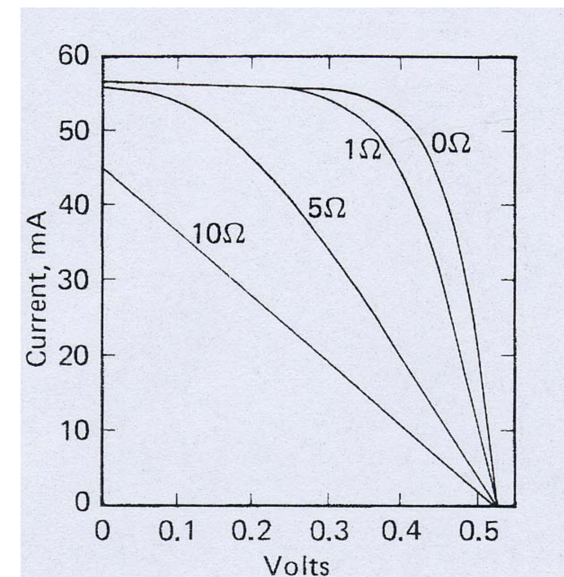


Ohmic Contacts

-**Front** contact must minimize series resistance losses, providing at the same time the maximum light amount to reach the cell surface.



-A good **back** contact allows to increase J_{sc} and V_{oc} (confinement techniques).



-Good ohmic contact **metal/silicon**

-Low metal **resistivity**

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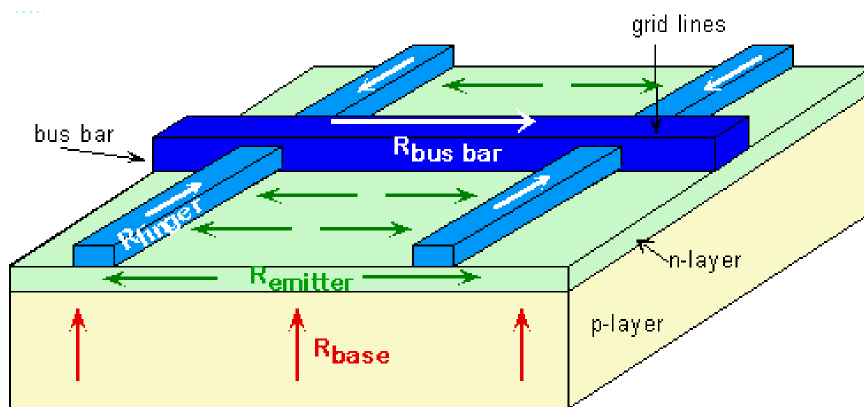
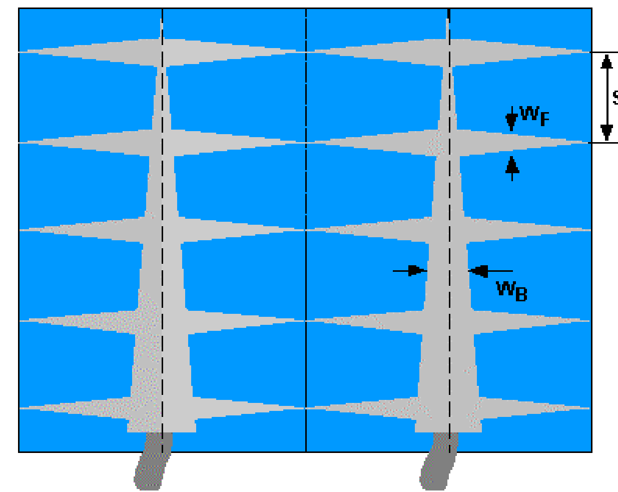
Ohmic Contacts

Front Grid:

-**Busbar** are directly connected to the external load

-**Fingers** collect current to delivery to a busbar.





Rs=Rbase+Remitter+Rgrid

Contact technologies

- photolitography
  vacuum evaporation
- screen printing
- electrochemical growth

Deposition technique/ Metal	Electro-plating Electroless	Evaporation	Screen printing
Ni	Front	Front	
Au	F/B	F/B	F/B
Ag	Front	Front	Front
Ti		Front	
Pd		Front	
Al	Back	Back	Back

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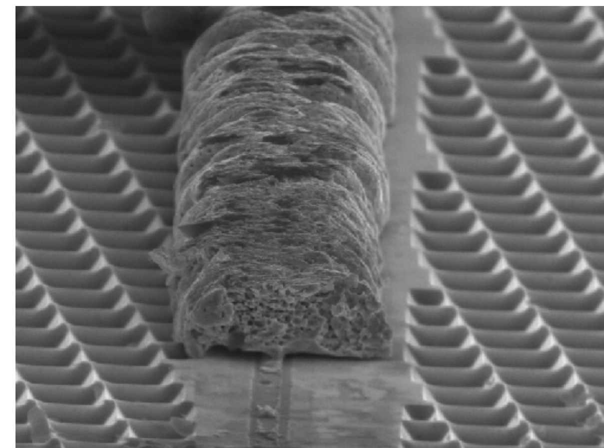
photolitography

- photosensitive polymer is deposited on wafer surface
-Regions to metallize are exposed through a mask to UV light
- **vacuum evaporation**

Front:
Ti (400 A) adherence to Si
Pd (200 A) barrier layer
Ag 1-5 μm good electrical conductivity
Back:
Al 1μm

-**Lift-off**: photoresist removed in acetone

-**Annealing**: 400- 600 °C N_2 or forming gas
ohmic contact
Resolution: few microns
Shadowing < 4%



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Screen printing

-contact grid is obtained by depositing on wafer surface, through metal **screens**, inks or conductive pastes

-inks contain metal grains (Ag, Al), glasses, organic binders and solvent

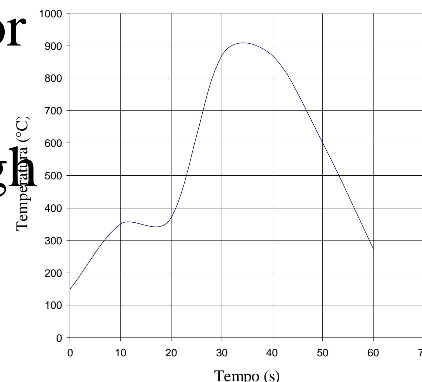
-Firing:

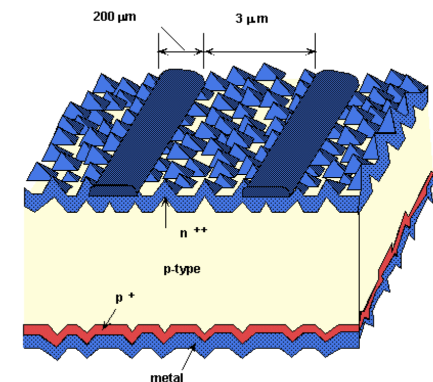
In a belt furnace, the glass melting temperature (about 800°C) is reached for few minutes

Contact to Si: alloy metal/Si (Al) through glass matrix (Ag)

Resolution: 80-100 micron

Shadowing:10%





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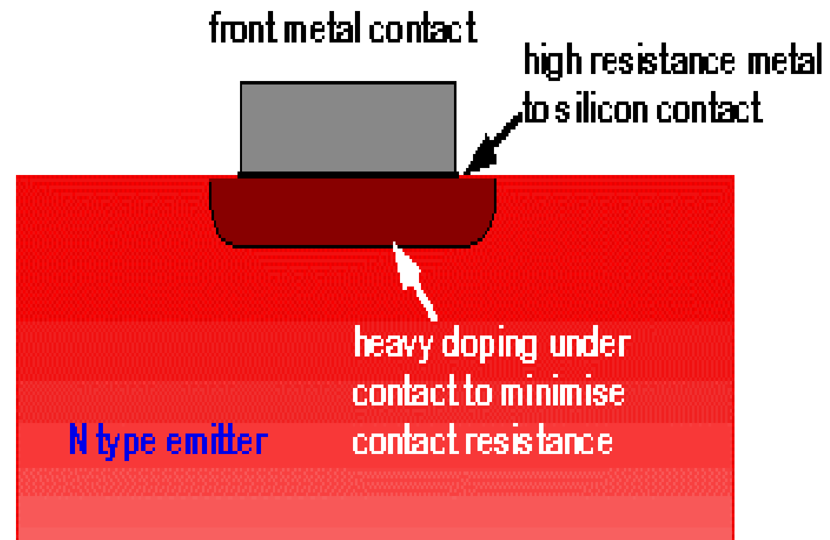
Selective Emitter

•Heavy doped emitter :
low response in blue region -
"*dead layer*", photogenerated carriers have low probability to be collected-



•**Selective emitter:**
regions under contacts are heavy doped, to reduce Rc
Exposed region is low doped to increase collection in blue spectral portion

- double diffusion, laser doping

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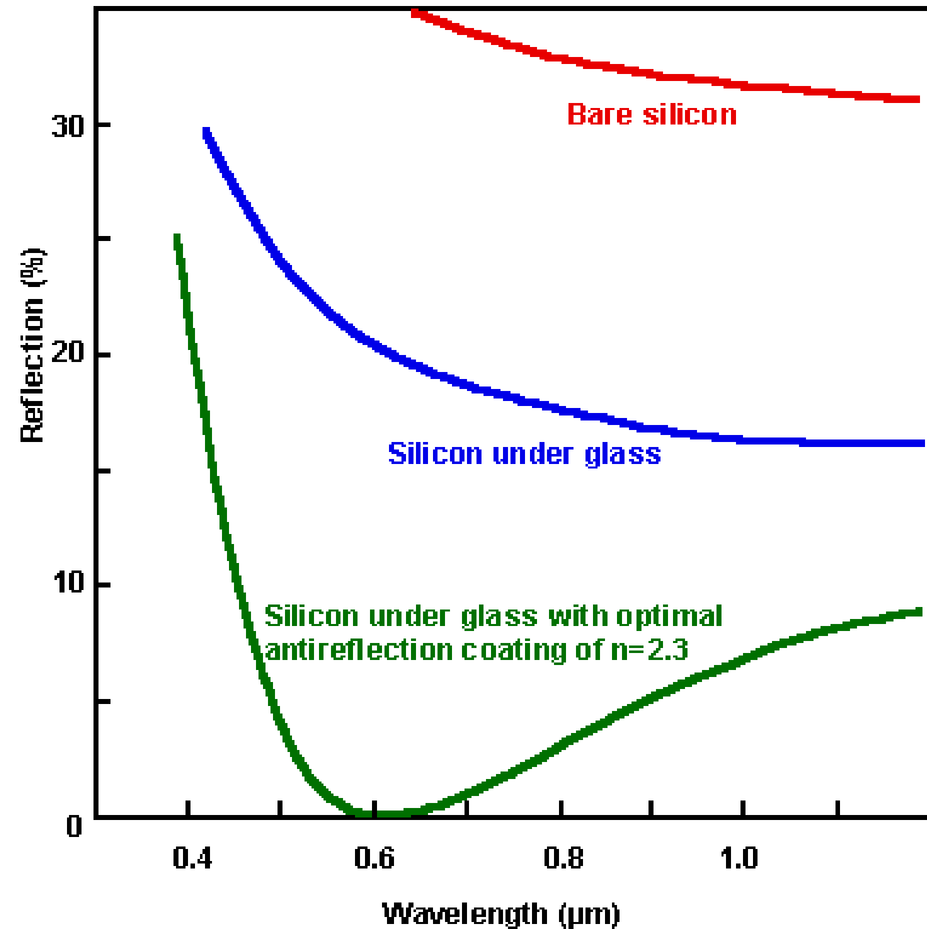
AntiReflection treatments

•Silicon reflects 35% of incident light, and up to 54% at short λ (high refractive index n)

•Techniques to reduce losses:

-Deposition of one or more layers of thin oxides

- Surface Texturization



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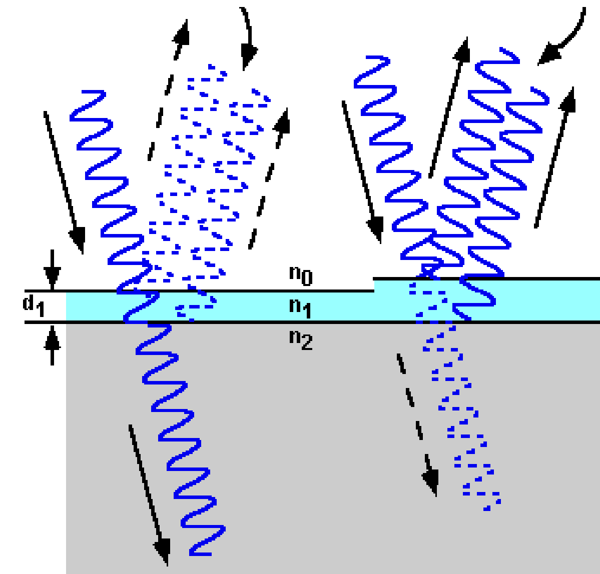
Thin AR layers

•losses due to **reflection** can be drastically **reduced**

$$R = \left(\frac{n_2 - n_0}{n_2 + n_0} \right)^2$$

$$R = \frac{r_1^2 + r_2^2 + 2 r_1 r_2 \cos 2\delta}{1 + r_1^2 r_2^2 + r_1 r_2 \cos 2\delta}$$



$$r_1 = \left(\frac{n_0 - n_1}{n_0 + n_1} \right) \qquad r_2 = \left(\frac{n_1 - n_2}{n_1 + n_2} \right) \qquad \delta = \left(\frac{2\pi n_1 d_1}{\lambda} \right)$$

$$R = R_{\min} \Longrightarrow n_1 d_1 = \left(\frac{\lambda_0}{4} \right) \qquad d_1 = \left(\frac{\lambda_0}{4 n_1} \right)$$

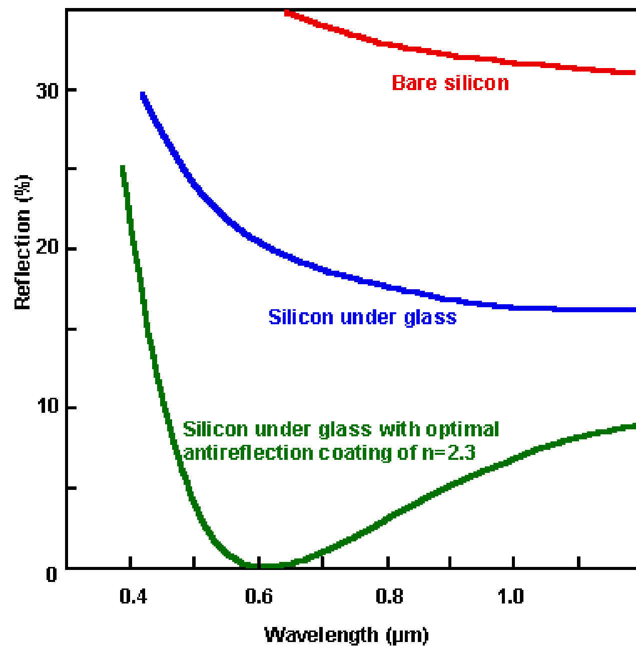
$$R_{\min} = \left(\frac{n_1^2 - n_0 n_2}{n_1^2 + n_0 n_2} \right)^2 \Longrightarrow R_{\min} = 0 \qquad n_1 = \sqrt{n_0 n_2}$$

Thin AR layers

• **single layer AR coating**:

λ_0= 600 nm; n_1=2.0; d_1=750 A

•Losses reduced to 10%



Material	n
Si	3,45
SiO	1,9
Al_2O_3	1,9
Si_3N_4	2,0
TiO_2	2,2
Ta_2O_5	2,2

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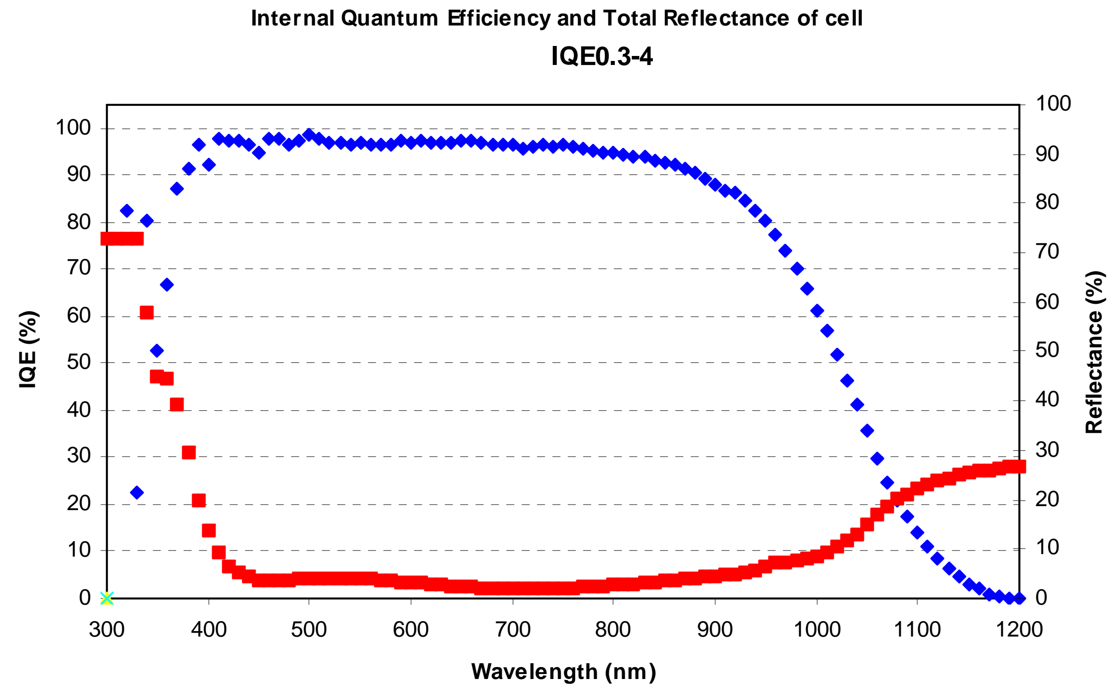
double layer AR coatings

-better match between high index of Si (3,5) and low index of air (1)

-AR effect over a wide wavelength range

- losses reduced to 3%



$$R_{min} = \left(\frac{n_1^2 n_3 - n_2^2 n_0}{n_1^2 n_3 + n_2^2 n_0} \right)^2$$

Material	n
Si	3,45
TiO_2	2,2
SiO_2	1,5
ZnS	2,3
MgF_2	1,4

1st layer: n_1=2.2-2.6
2nd layer: n_3=1.3-1.6

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ARC deposition methods

- vacuum Evaporation
- Sputtering
- Chemical Vapour Deposition
- Plasma Enhanced CVD

- thickness uniformity and reproducibility
- Stoichiometry control

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TEXTURING

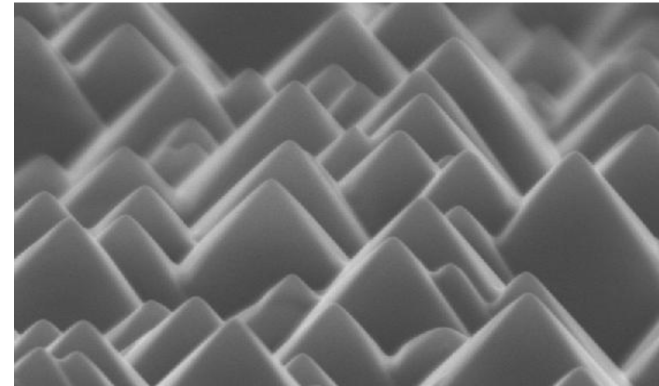
•pyramidal structures (about 10 microns) on wafer surface

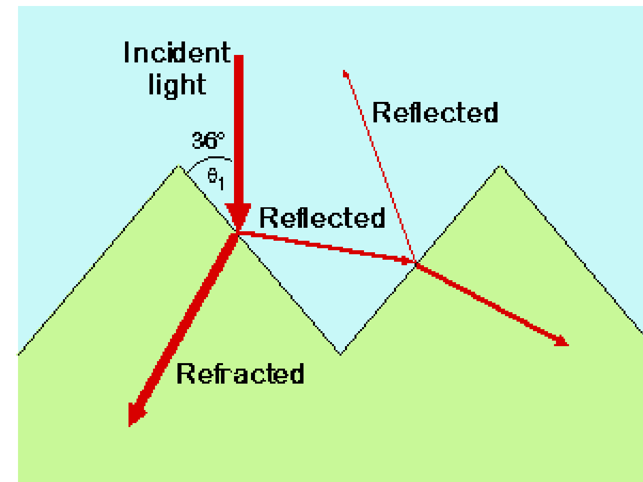
• incident light is trapped (multiple reflections)

-larger exposed area
-Oblique incidence (increased collection efficiency at long λ)

Reflectance < 10%

with ARC < 4%





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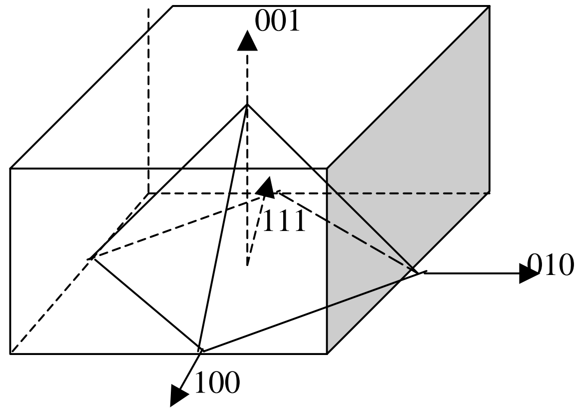

-for Si <100> oriented, structure is achieved by intersection between the <100> and <111> planes (α=54.7°), allowing at least two consecutive reflections

-wet anisotropic etch
NaOH or KOH based

-Different etch rates along different crystallographic directions:

etch rate about 35 faster for <100> direction than for <111> direction.

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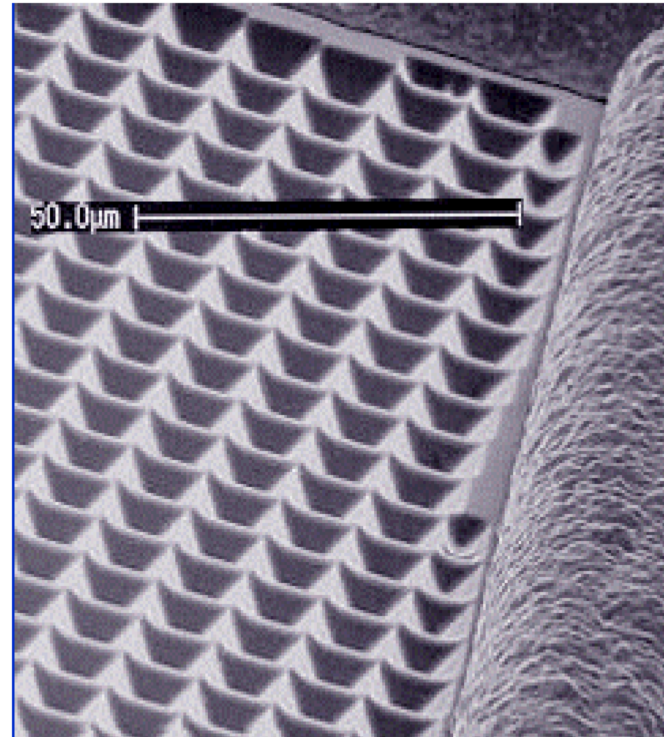
TEXTURING

-Inverted pyramids structure reduces reflection to few percent

-honeycomb: traps light in multi-crystalline Si cells



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Thank you for your attention