The Abdus Salam
International Centre for Theoretical Physics

United Nations
Educational, Scientific
and Cultural Organization

International Atomic
Energy Agency

Workshop on "Physics for Renewable Energy"
October 17 - 29, 2005

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"Amorphous Silicon / Cyrstalline Silicon Heterojunction Solar Cell"

E. Centurioni
CNR/IMM
AREA Science Park - Bologna
Italy

Amorphous silicon / crystalline silicon heterojunction solar cell

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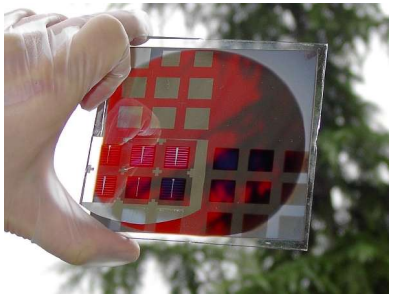
Summary

- Heterojunction solar cell general overview
- fabrication steps
- emitter properties
- a-Si / c-Si interface properties
- a-Si buffer layer
- epi-Si buffer layer
- n or p type c-Si ?
- conclusion

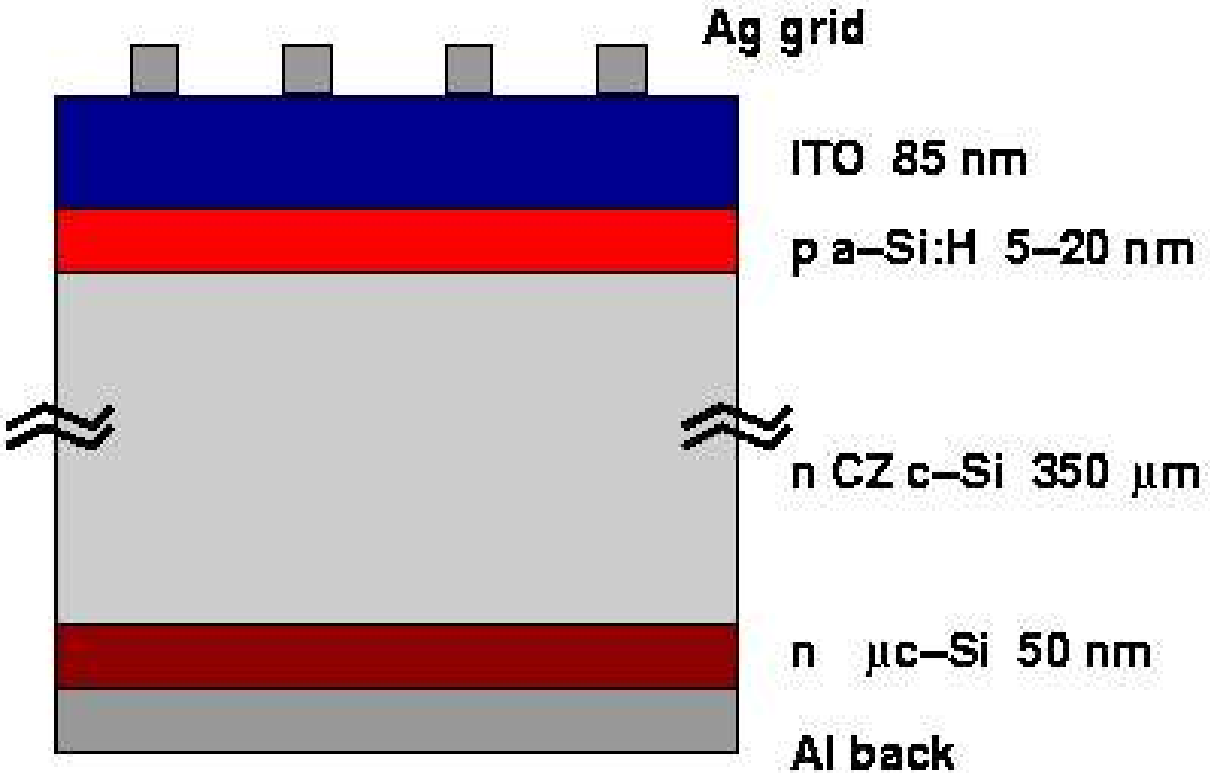
Crystalline Si technology:
high efficiency, expensive



Thin film **amorphous** silicon solar cell:
low efficiency, cheap

Amorphous silicon /**crystalline** silicon heterojunction solar cell:
High efficiency, cheap technology

Heterojunction solar cell layout

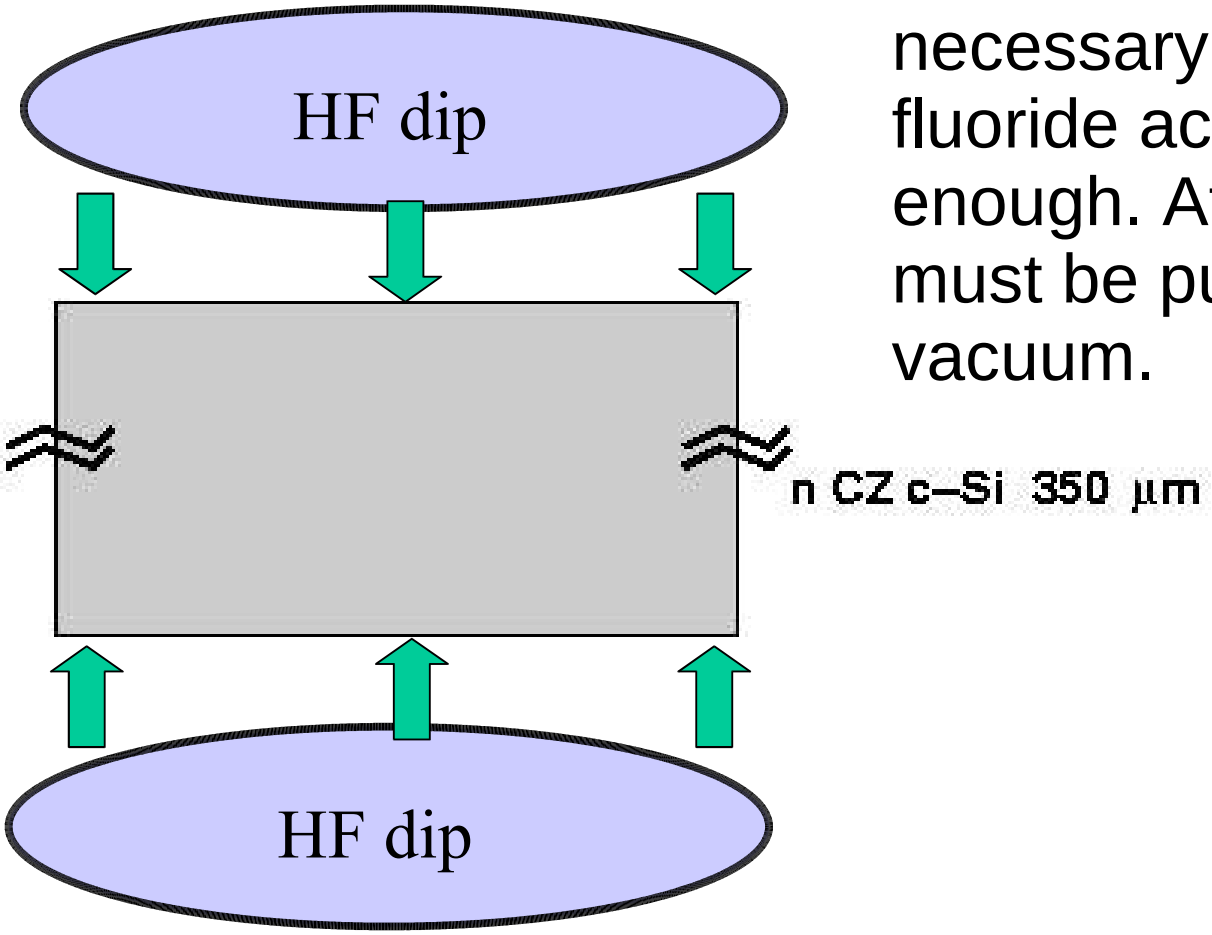


Simple low temperature process (< 250 C)

PECVD, sputtering, evaporation, low T screen-printing

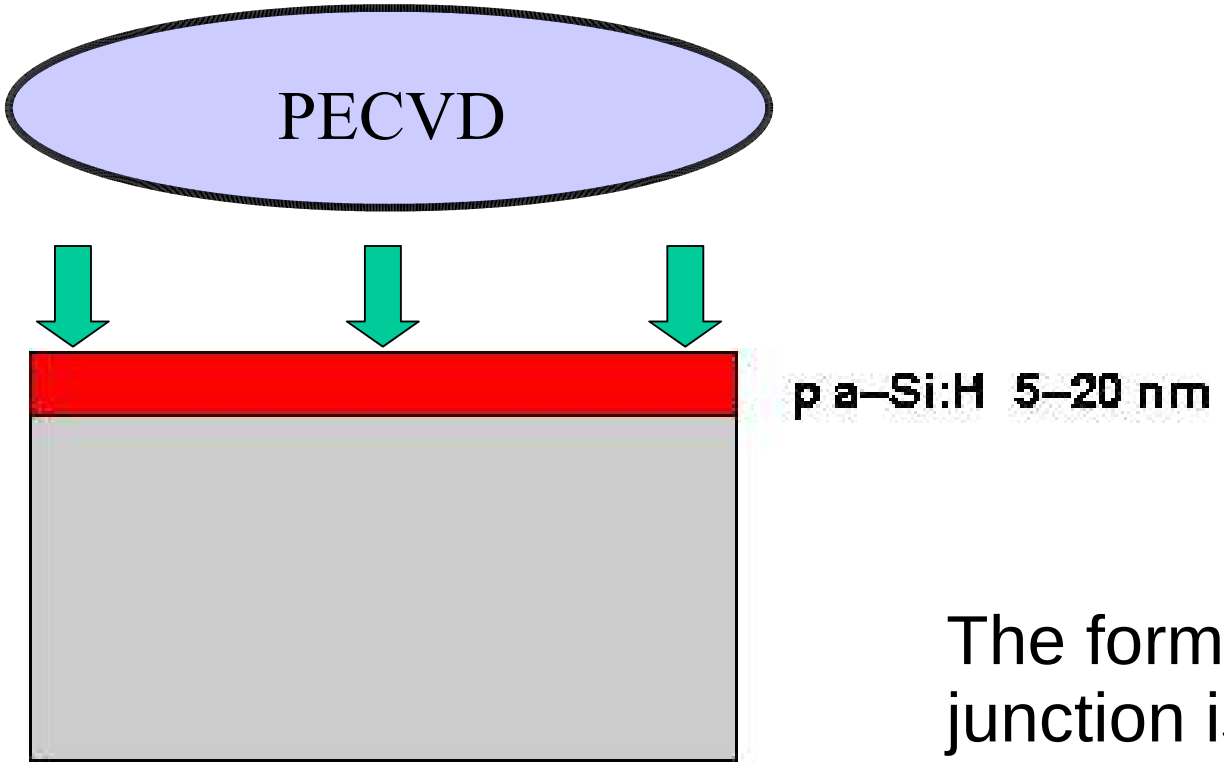
It is not an esoteric device: Market percentage in 2003 was 8%

Fabrication process: step 1 c-Si wafer cleaning



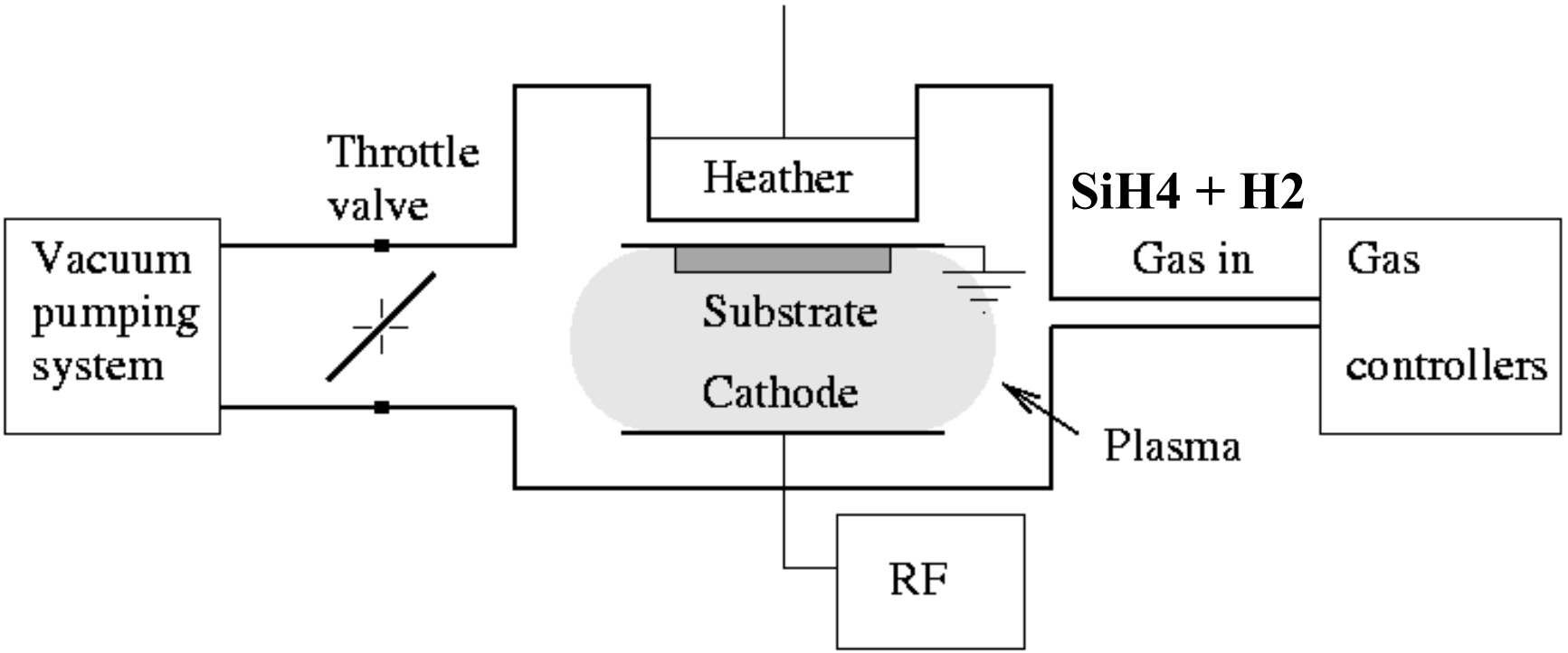
Removal of native oxide is necessary. A simple dip in hydro fluoride acid (HF) is usually enough. After this step the sample must be put immediately into vacuum.

Fabrication process: step 2 junction formation



The formation of the p-n junction is obtained by PECVD deposition of a p type a-Si layer. The layer should be as thin as possible.

Plasma Enhanced Chemical Vapour Deposition (PECVD)



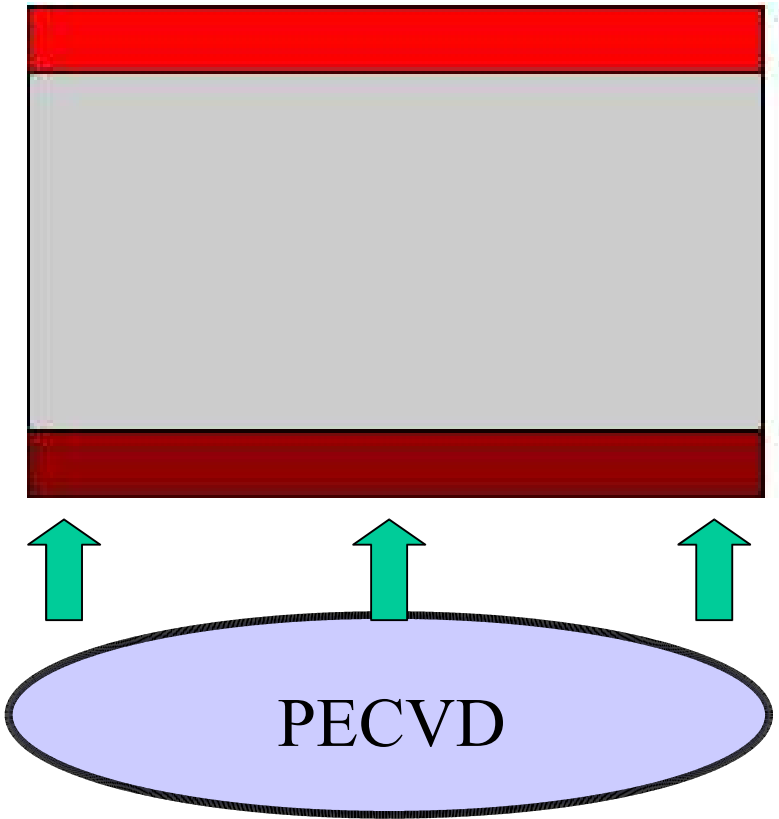
Low temperature process (plastic substrates, TFT display)

Gas dissociation is due to the plasma, not the temperature like in conventional CVD

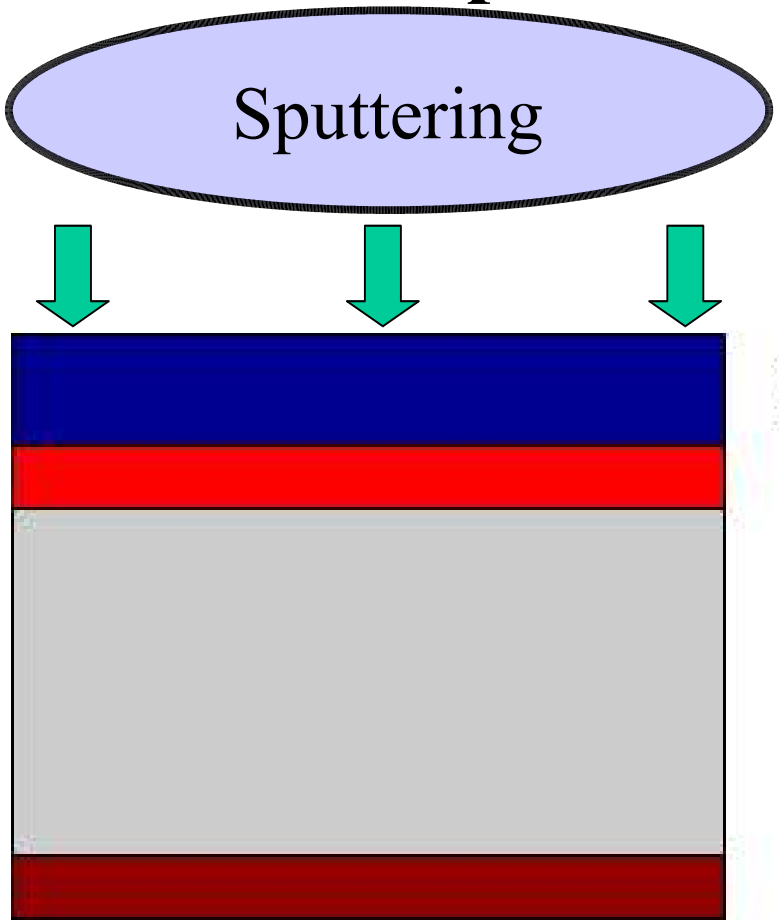
Large area process (~ m^2)

Fabrication process: step 3 n+back contact

A n type a-Si or μc-Si layer is deposited by PECVD on the back side. This layer improves the ohmic contact with the metal contact and / or gives the back surface field effect.

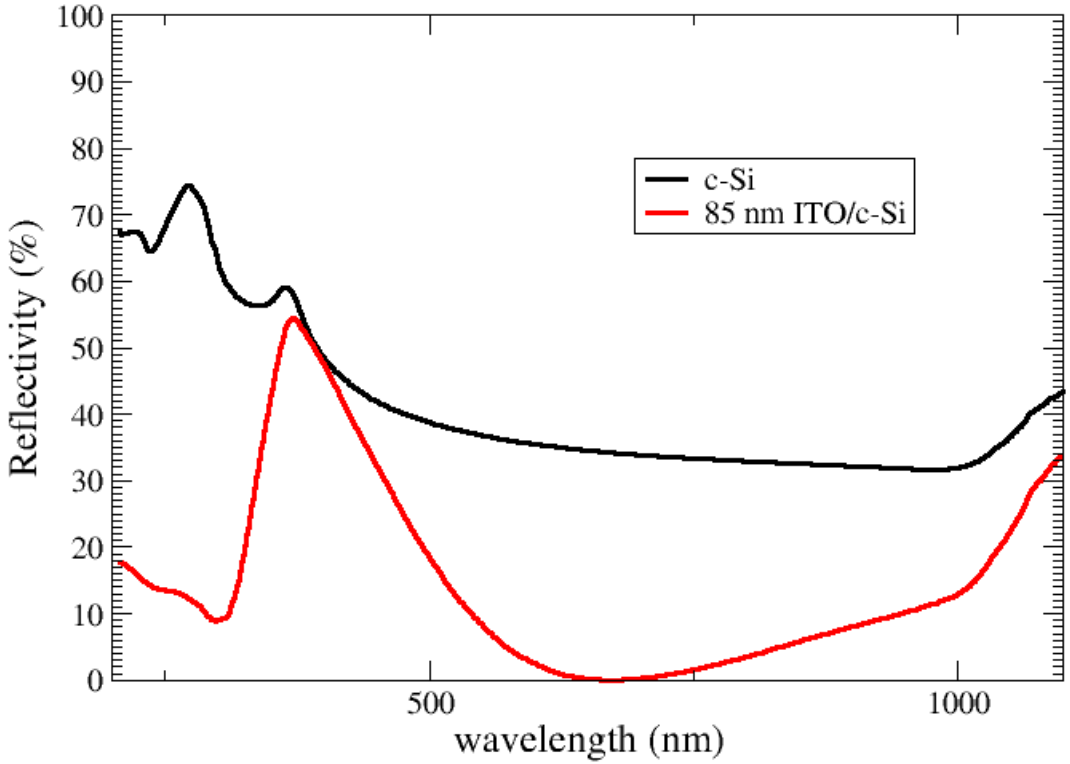


Fabrication process: step 4 TCO deposition



The transparent conductive oxide (TCO) works as a charge collector and as an anti reflecting coating.

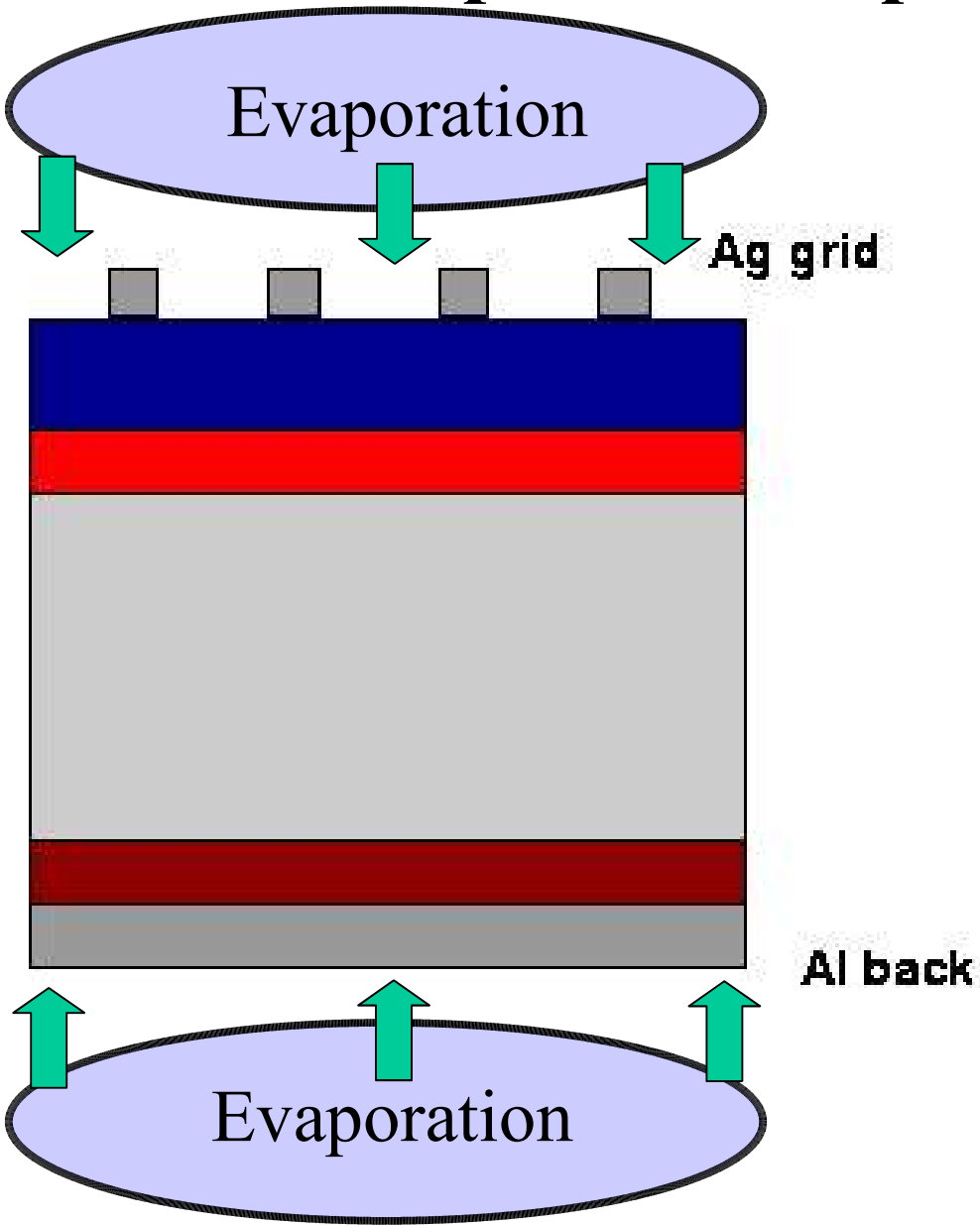
Fabrication process: step 4 TCO deposition



Indium tin oxide (ITO) has a good conductivity (2E-4 ohm cm) that gives a sheet resistance of about 20 ohm square. Because the anti reflecting behavior the short circuit current increases of more than 30%.

Computed reflectivity (**Optical**) of flat c-Si and 85 nm of ITO on c-Si.

Fabrication process: step 5 contacts deposition

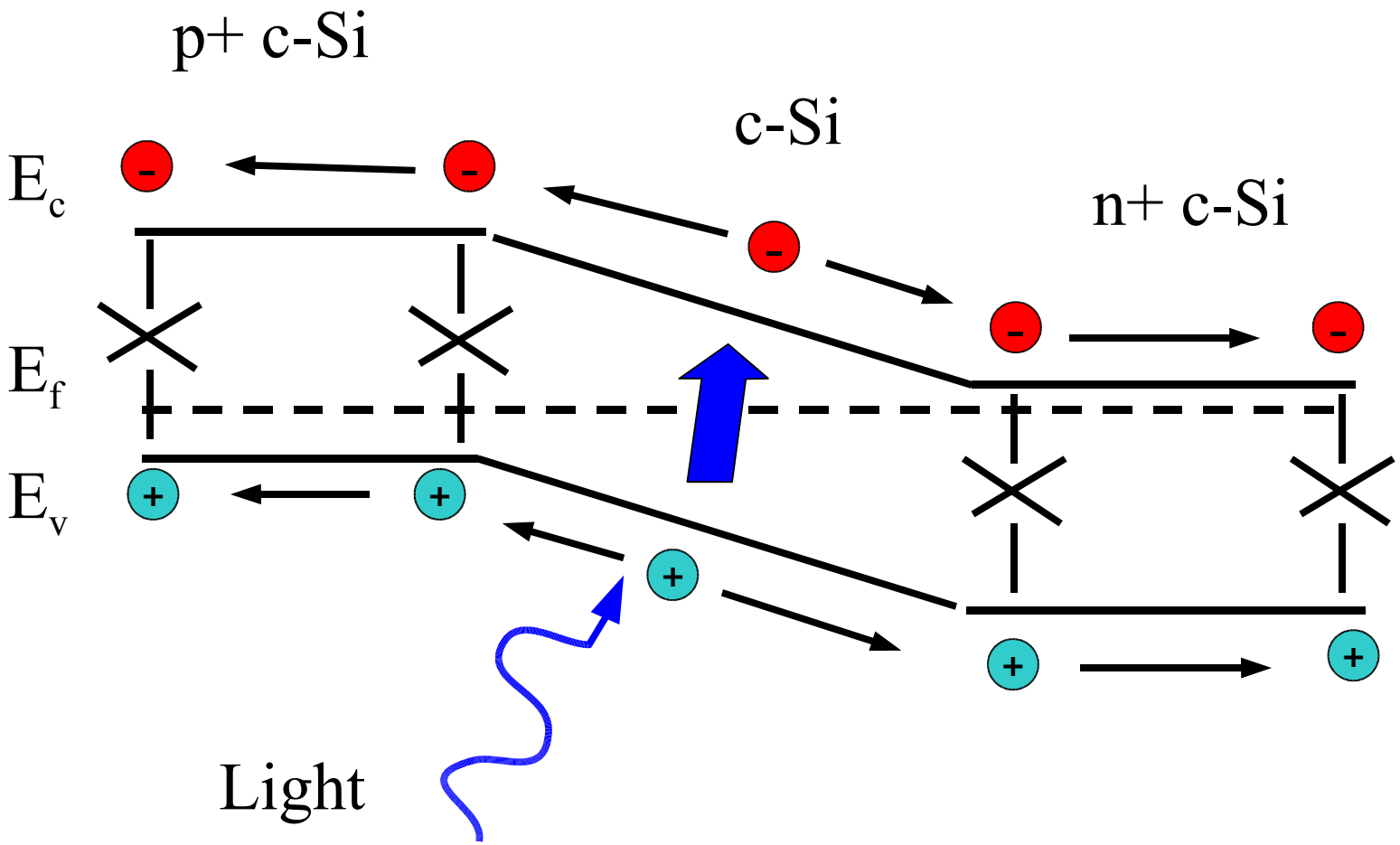


Electric contacts are obtained by thermal evaporation through metal mask. Low temperature screen printing technique can be also used.

Heterojunction main features

- high lifetime of charge carriers in the c-Si base
- complete low temperature process
- no degradation of c-Si electronic qualities
- low energy consumption
- low temperature coefficient
- in-line production
- stable efficiency
- compatible with low cost poly silicon wafers

Homojunction energy band diagram

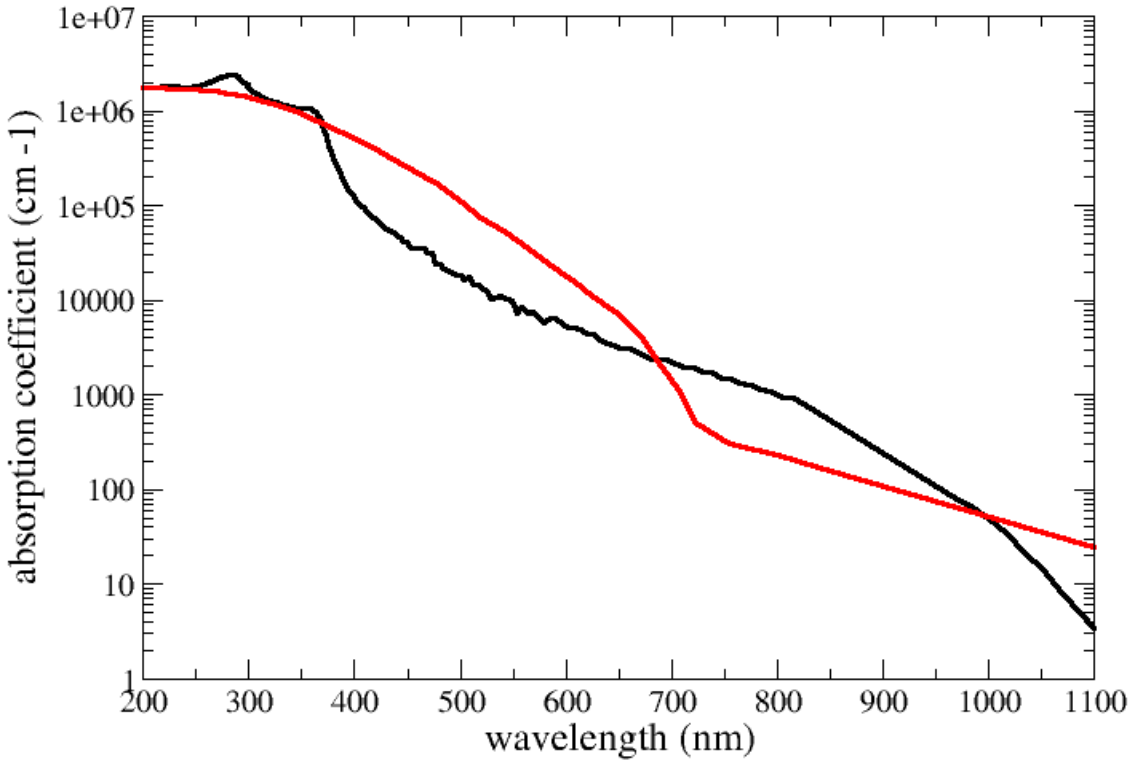


Amorphous silicon properties

High energy gap 1.7 eV

Pseudo direct band gap

Poor electronic properties
(if compared with c-Si)

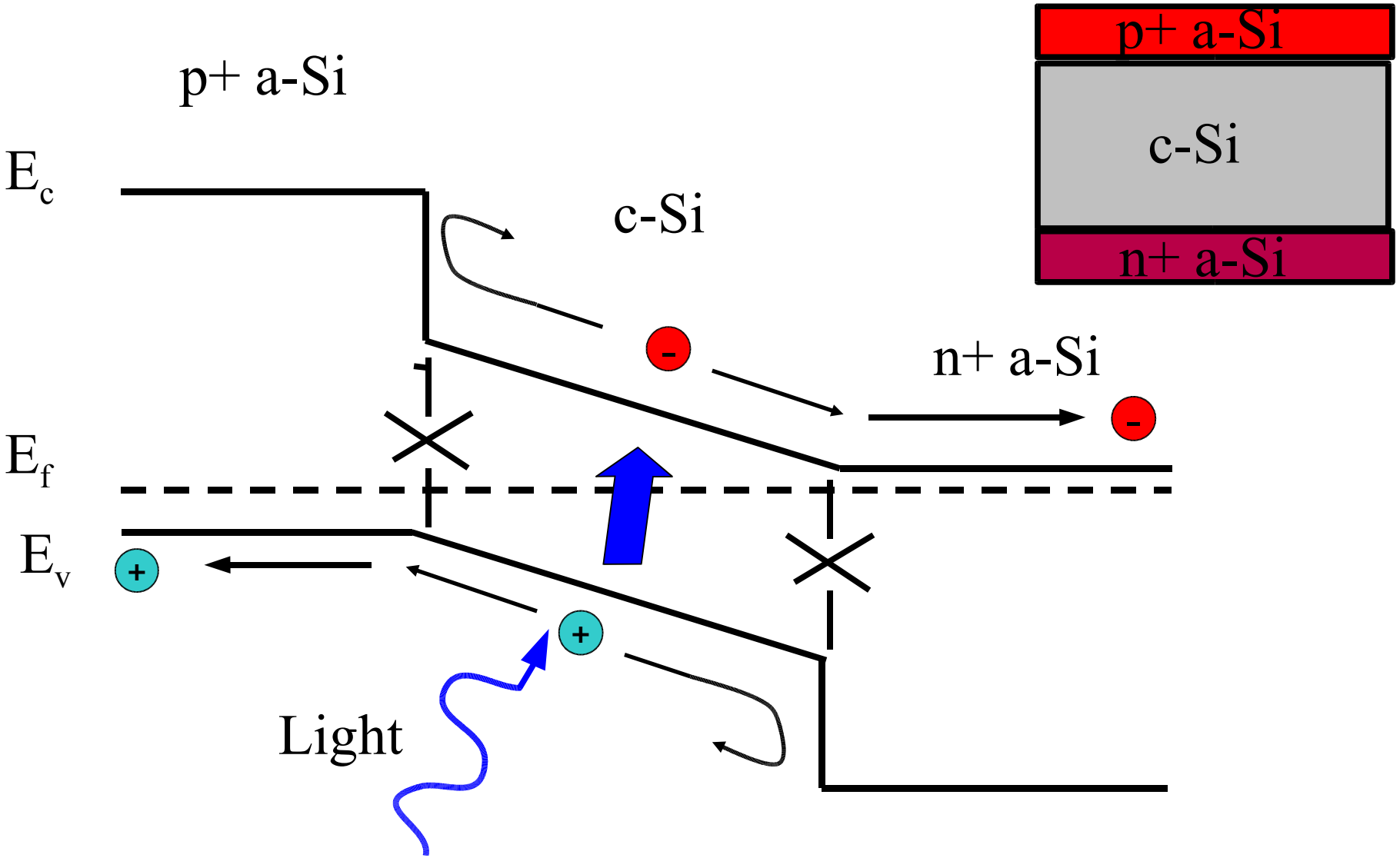


C-Si (black) and a-Si (red) absorption coefficient

Amorphous silicon electronic properties

	a-Si:H	c-Si
mobility e (cm^2/vsec)	1	1300
mobility h (cm^2/vsec)	3E-3	500
conductivity n (siemens/cm)	1E-2	100
conductivity p (siemens/cm)	1E-4	100
gap (eV)	1.7	1.1

Heterojunction energy band diagram



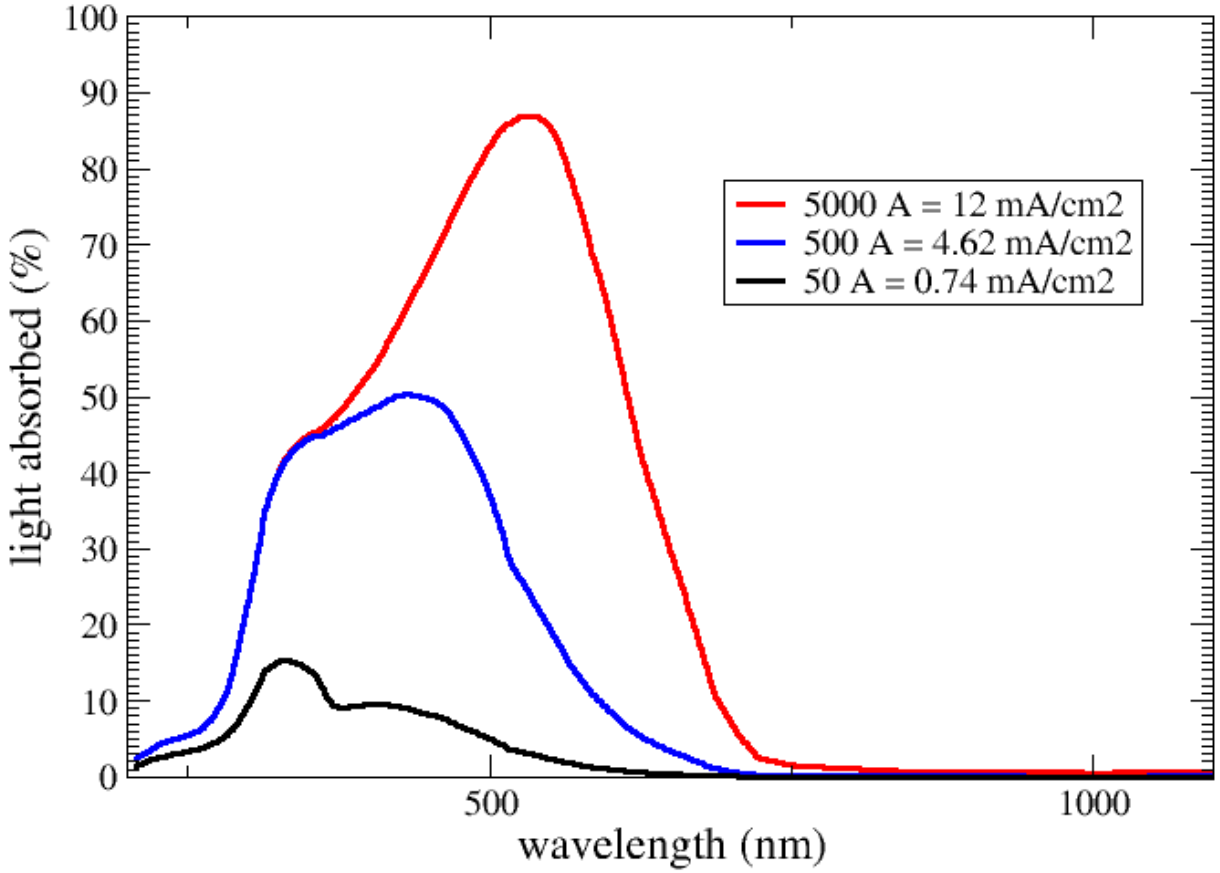
Amorphous silicon emitter properties

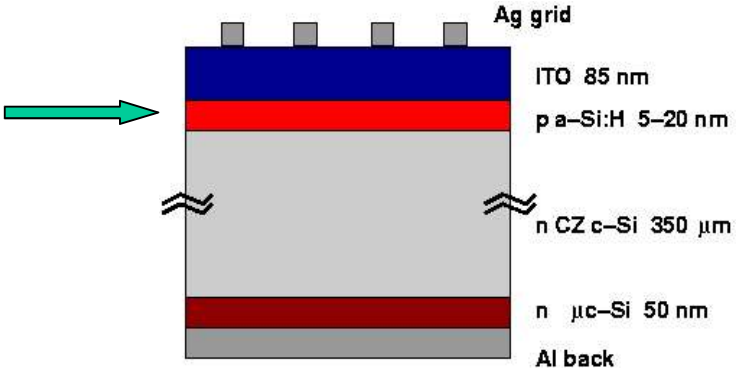
it works as a barrier for minority carrier injected from the c-Si base limiting the recombination

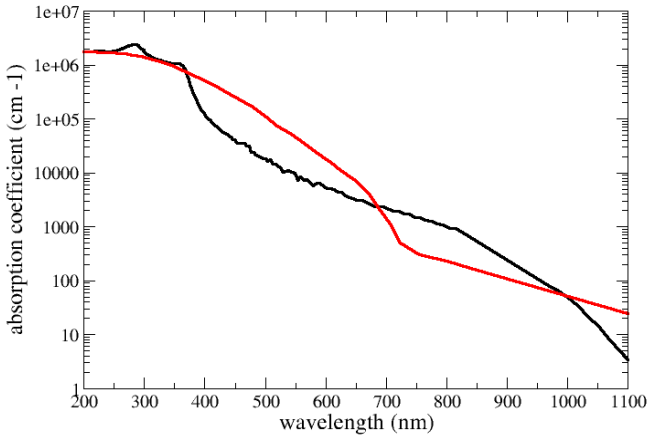
mainly because poor electronic properties is a dead layer, i.e. light absorbed is not collected

the interface between a-Si and c-Si mus have a low defect density in order to reduce recombination

a-Si emitter is a dead layer

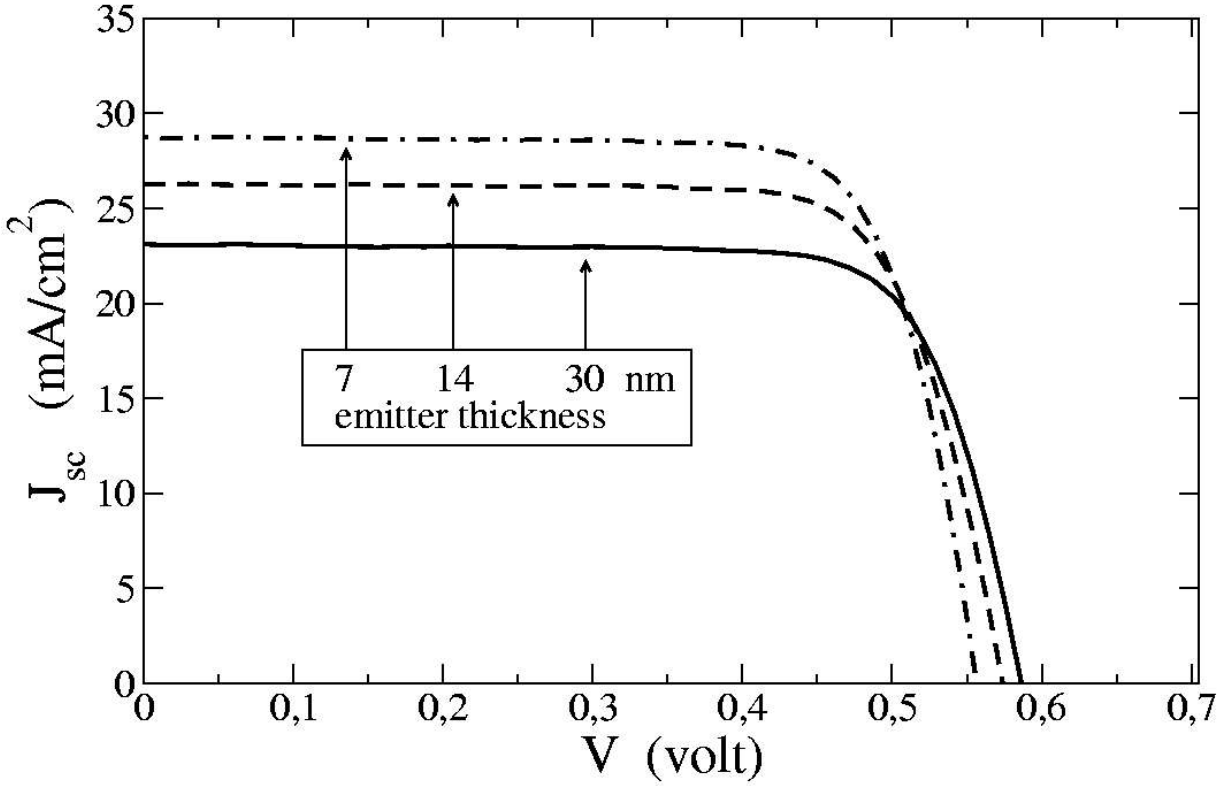


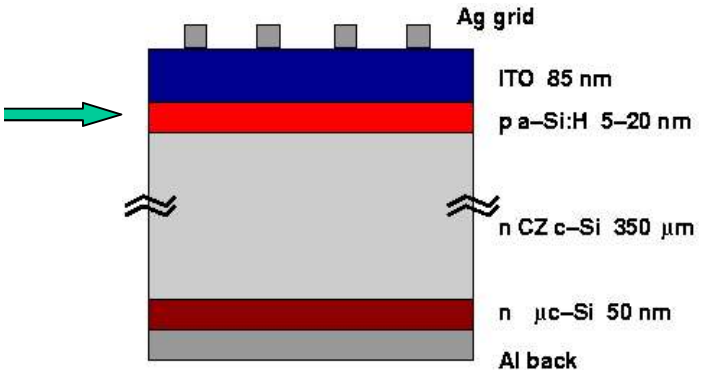


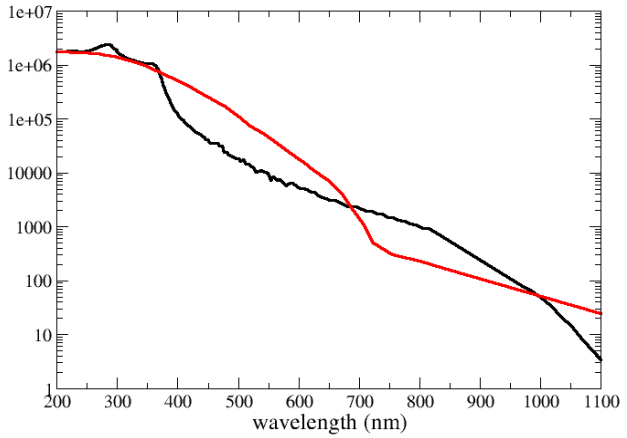


Calculated emitter light absorption.
Software used: **Optical**

a-Si emitter is a dead layer







Experimental light J-V for different emitter thickness

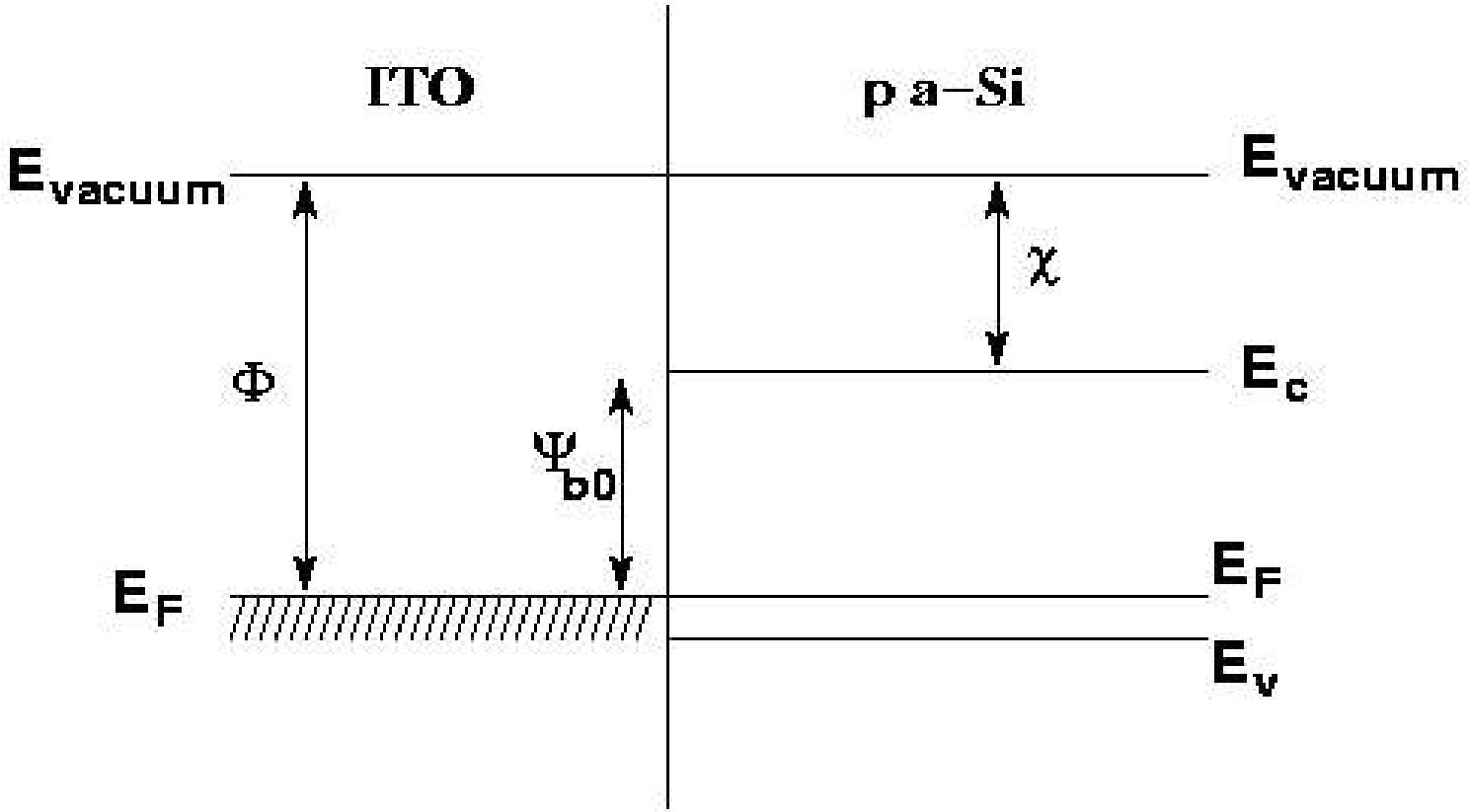
a-Si emitter characteristics

a-Si emitter should be as thin as possible to reduce photogenerated current losses

a-Si emitter should be able to sustain the electric field (avoid depletion) with the c-Si but also with the TCO

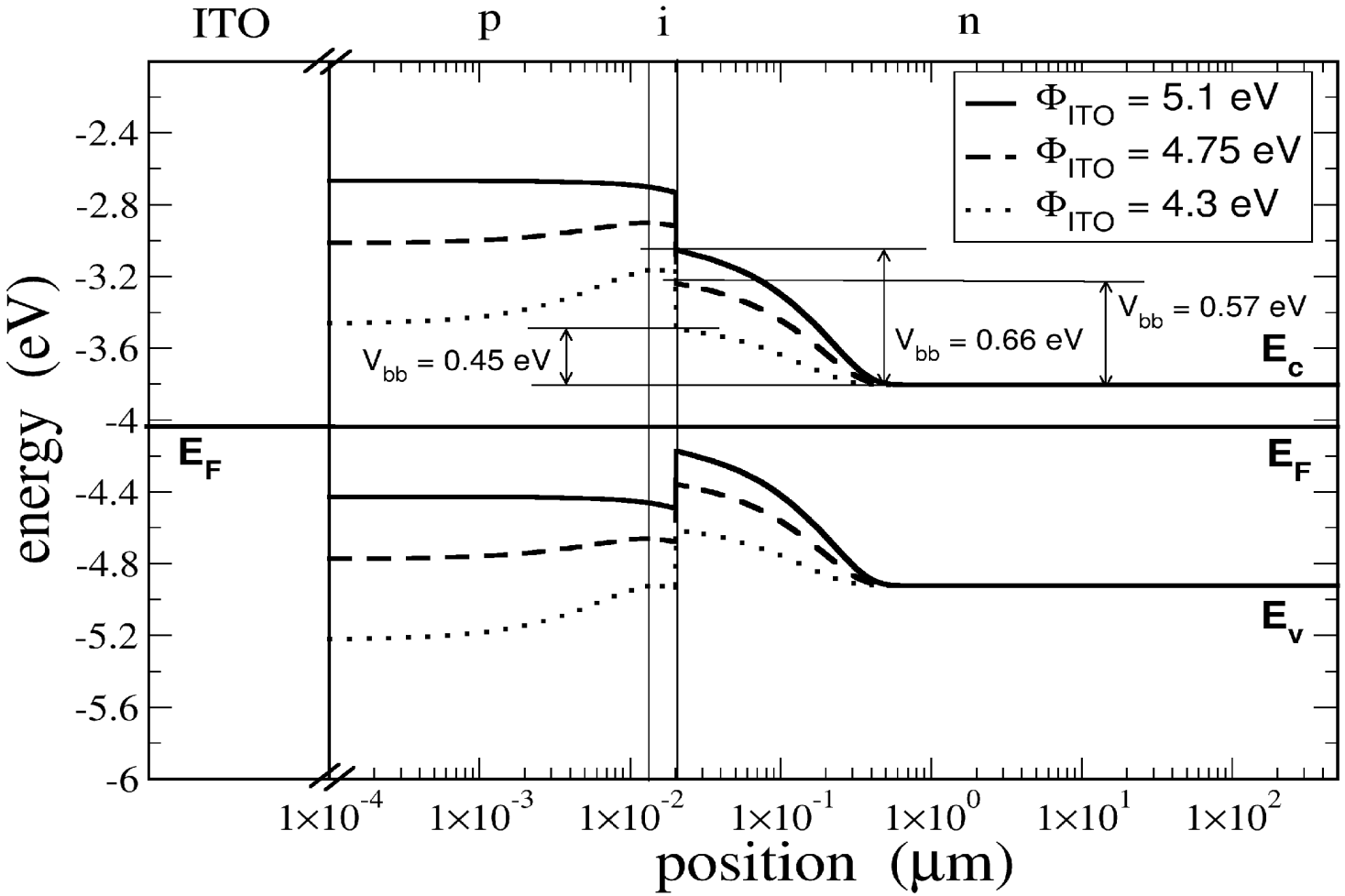
typical thickness used is 50 -100 A

emitter depletion due to ITO work function



Energy barrier at the ITO / a-Si interface
ITO work function is set equal to a-Si work function.

emitter depletion due to ITO work function



Computed heterojunction band diagram for different ITO work function at thermodynamic equilibrum. Software used: **AMPS**

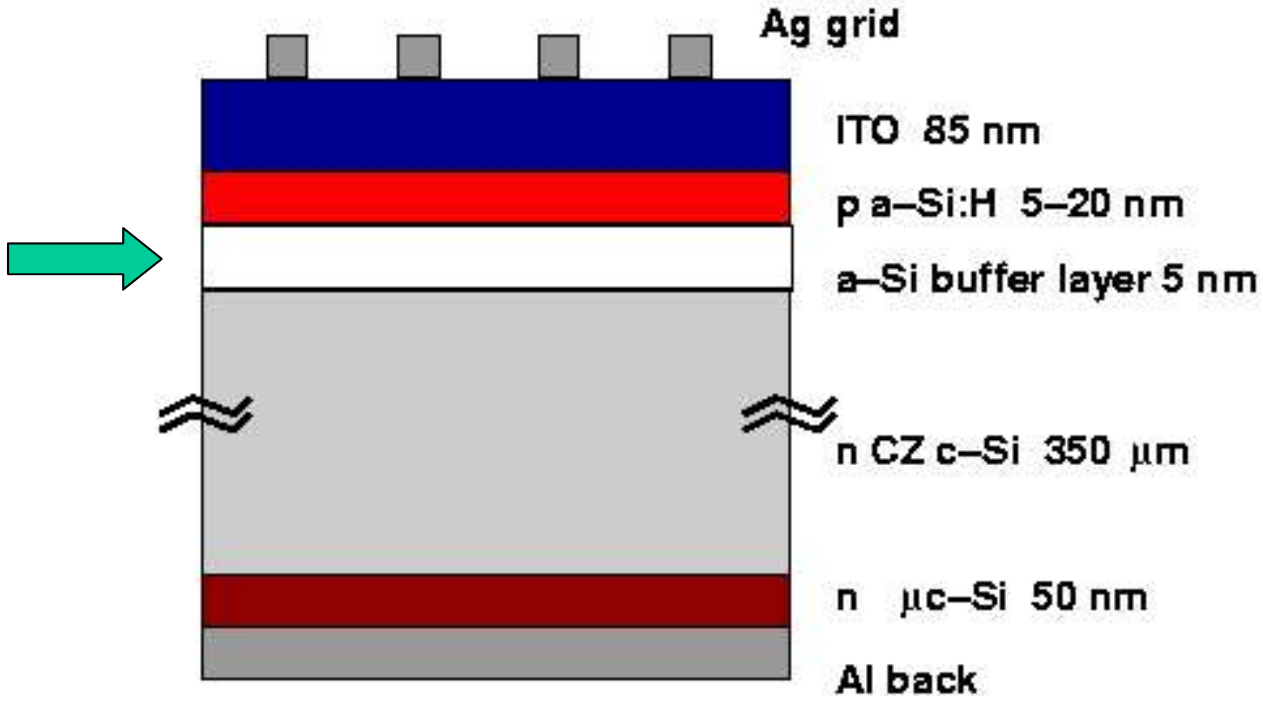
The a-Si/c-Si interface

The interface between c-Si a-Si can have a high defect density, i.e. energy levels in the forbidden gap

Energy levels in the forbidden gap cause charge carrier recombination at the interface limiting mainly the open circuit voltage

Defects at the interface must be reduced or passivated: the classical solution is the use of an intrinsic a-Si buffer layer

The a-Si buffer layer



An intrinsic a-Si layer at the interface between p a-Si and n c-Si is used to reduce defect density.

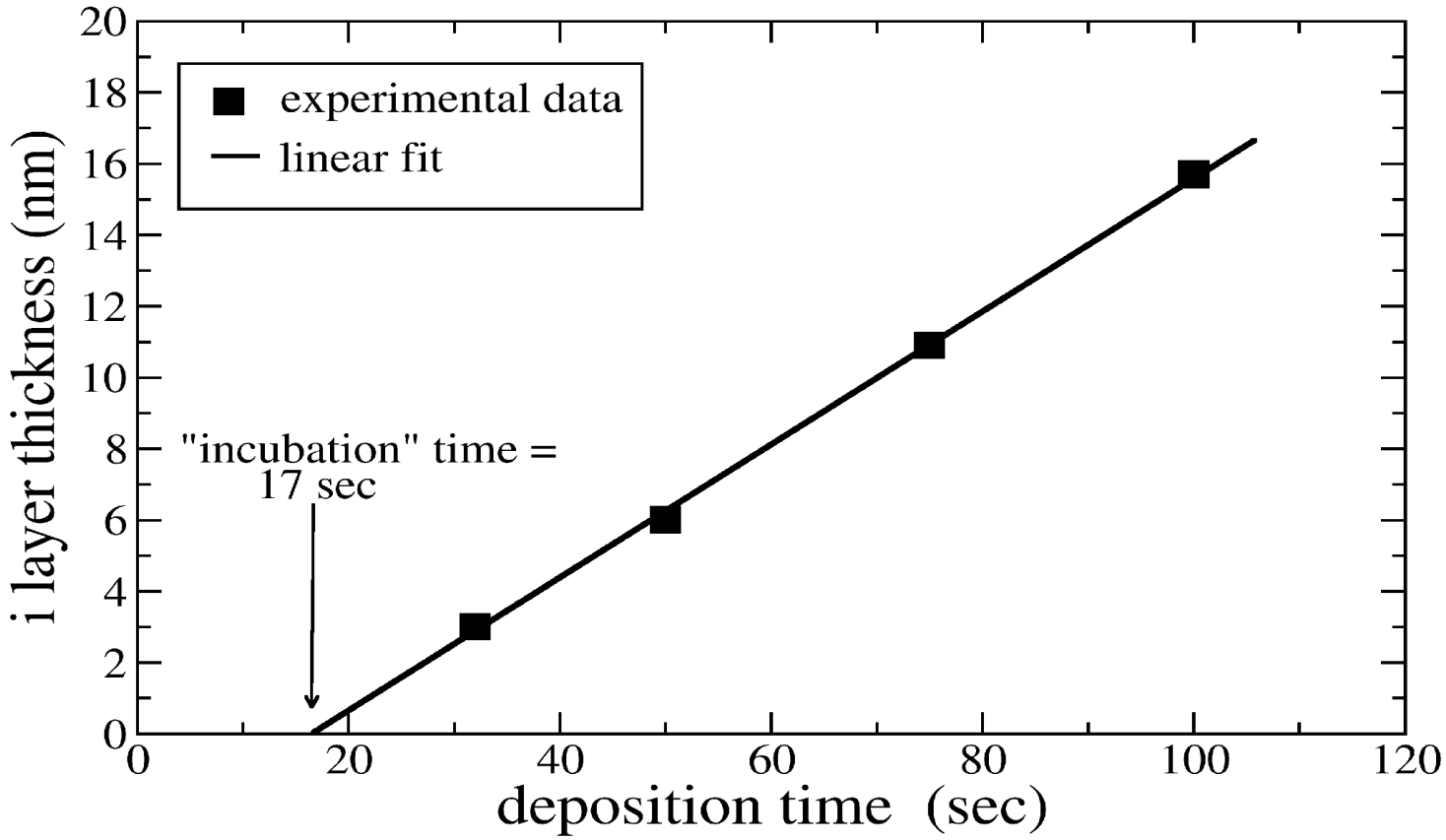
The a-Si buffer layer

The deposition of an amorphous silicon layer on top of crystalline silicon is not trivial

How to measure thickness ? How to measure opto-electronics properties ?

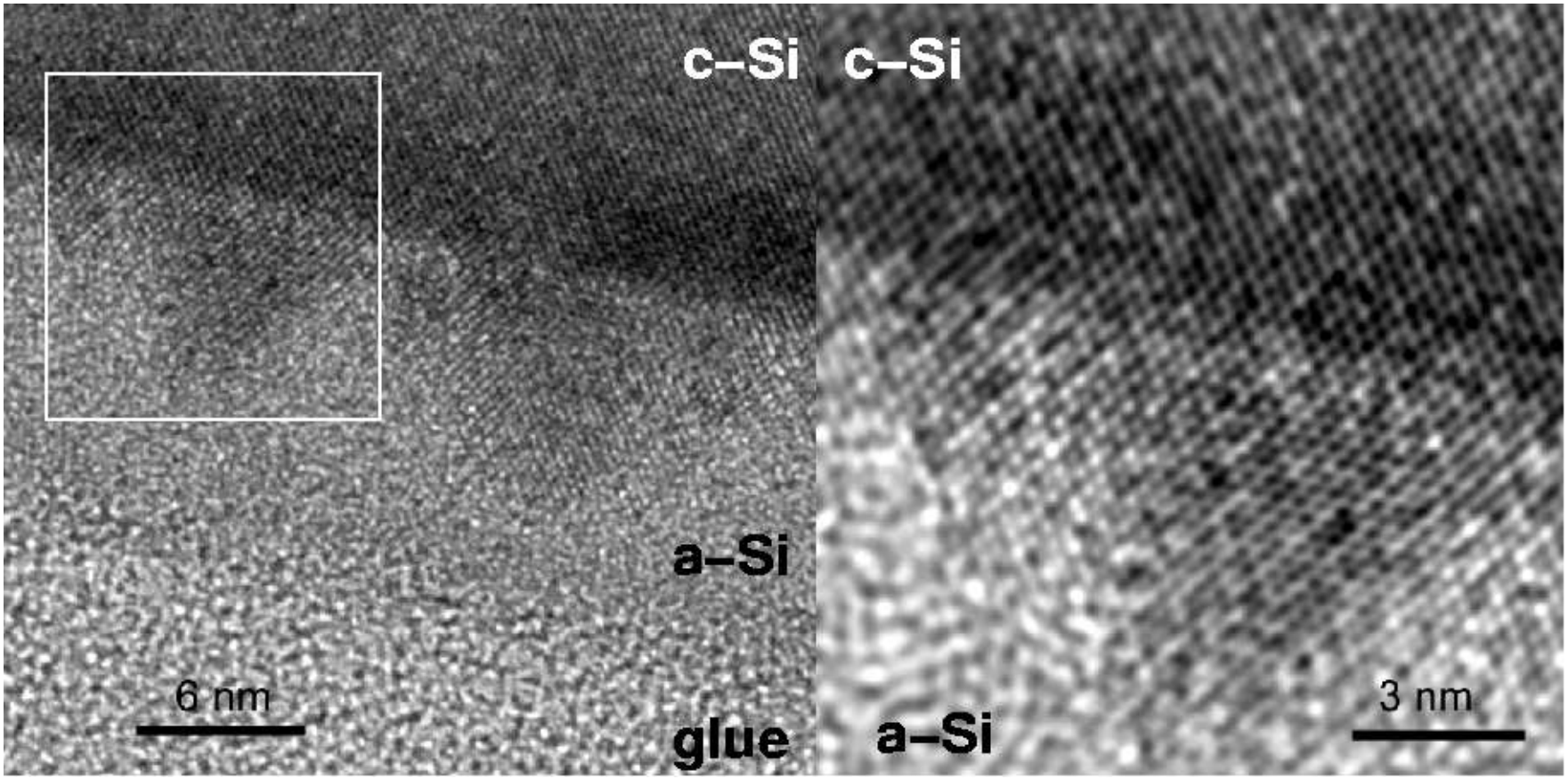
Usually a glass substrate is used for these purposes, but the result on silicon may be not the same

Amorphous silicon buffer layer



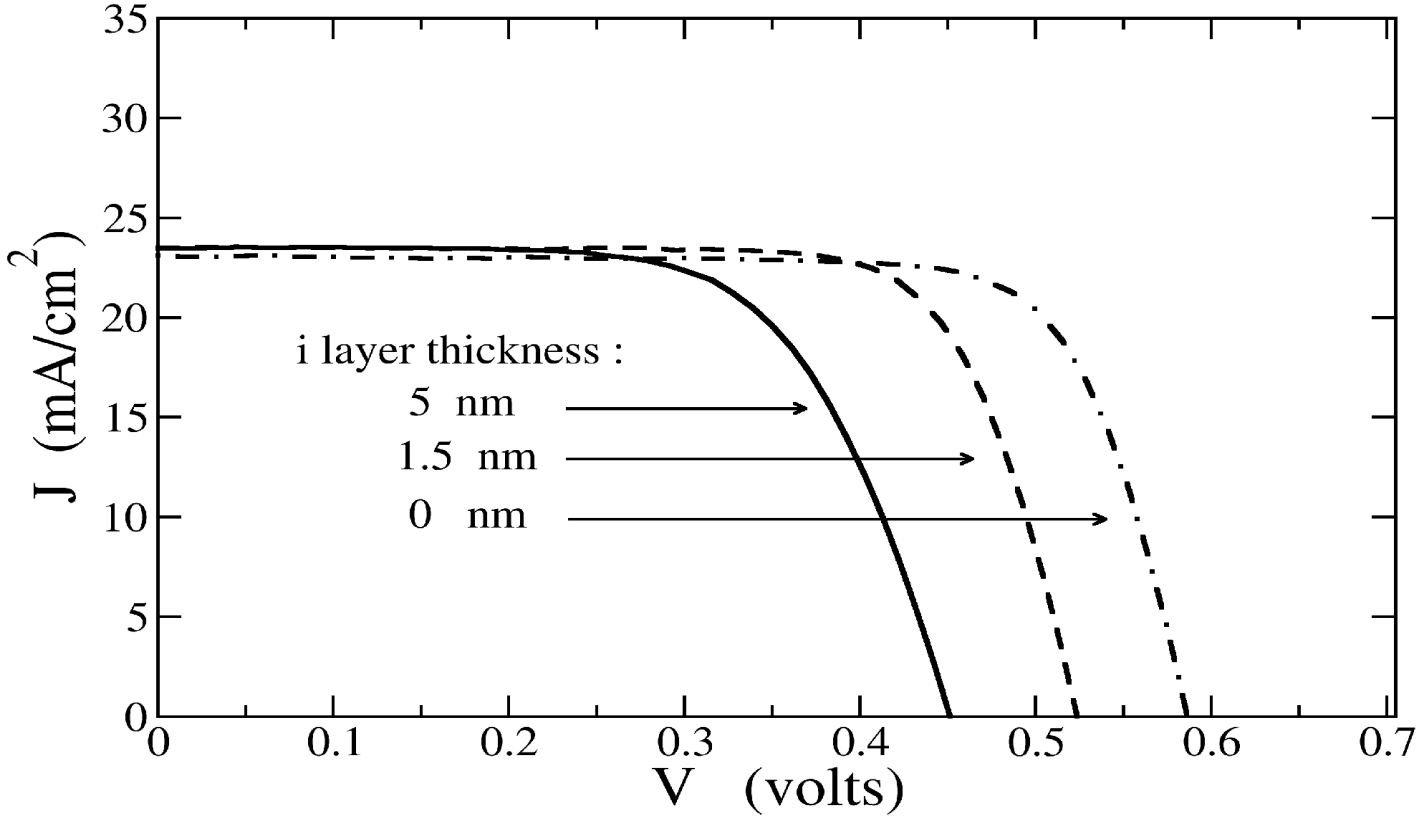
Amorphous silicon thickness for different deposition time. The substrate is crystalline silicon, the thickness was evaluated with spectroscopic techniques.

Amorphous silicon buffer layer ?



Cross section HR-TEM image of a-Si deposited on top of c-Si.

Amorphous silicon buffer layer ?



Experimental J-V curve for different thickness of “a-Si” buffer layer.

... is the buffer layer actually amorphous ?

in the literature the use of H2 dilution is often reported: H2 dilution enhance the epitaxial growth if the substrate is c-Si. However the same deposition condition used on glass substrate lead to a full a-Si layer (test and taylor)

no HRTEM are reported in the literature to prove the a-Si nature of the buffer layer

epitaxial nature of intrinsic buffer layer ?

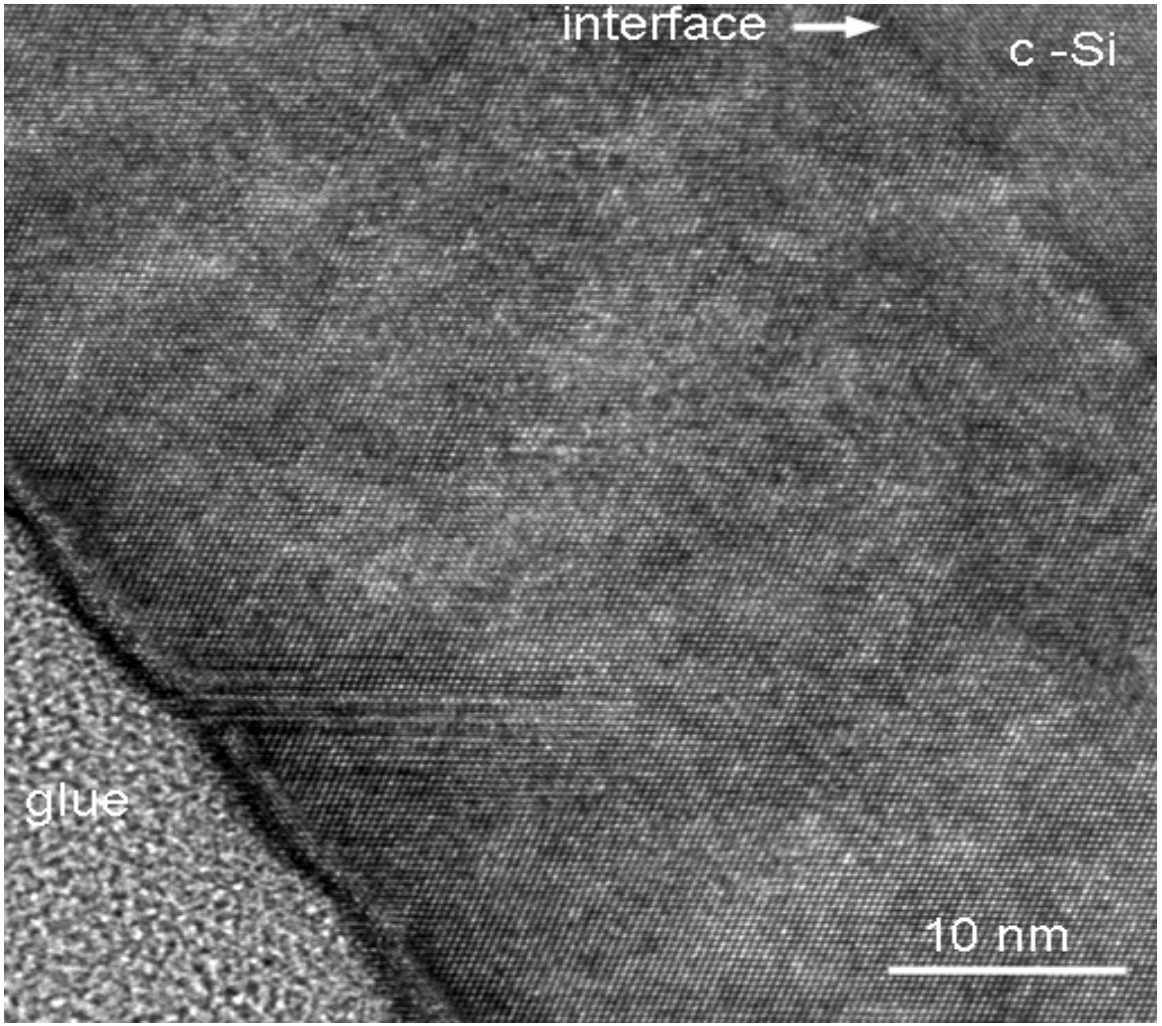
A new buffer layer concept with low temperature (PECVD) epitaxial silicon

Epitaxial silicon (epi-Si) can be deposited by PECVD at deposition temperature lower than 150 °C, using a hydrogen-silane mixture with a high hydrogen dilution

A completely epitaxial silicon layer can be used as buffer layer

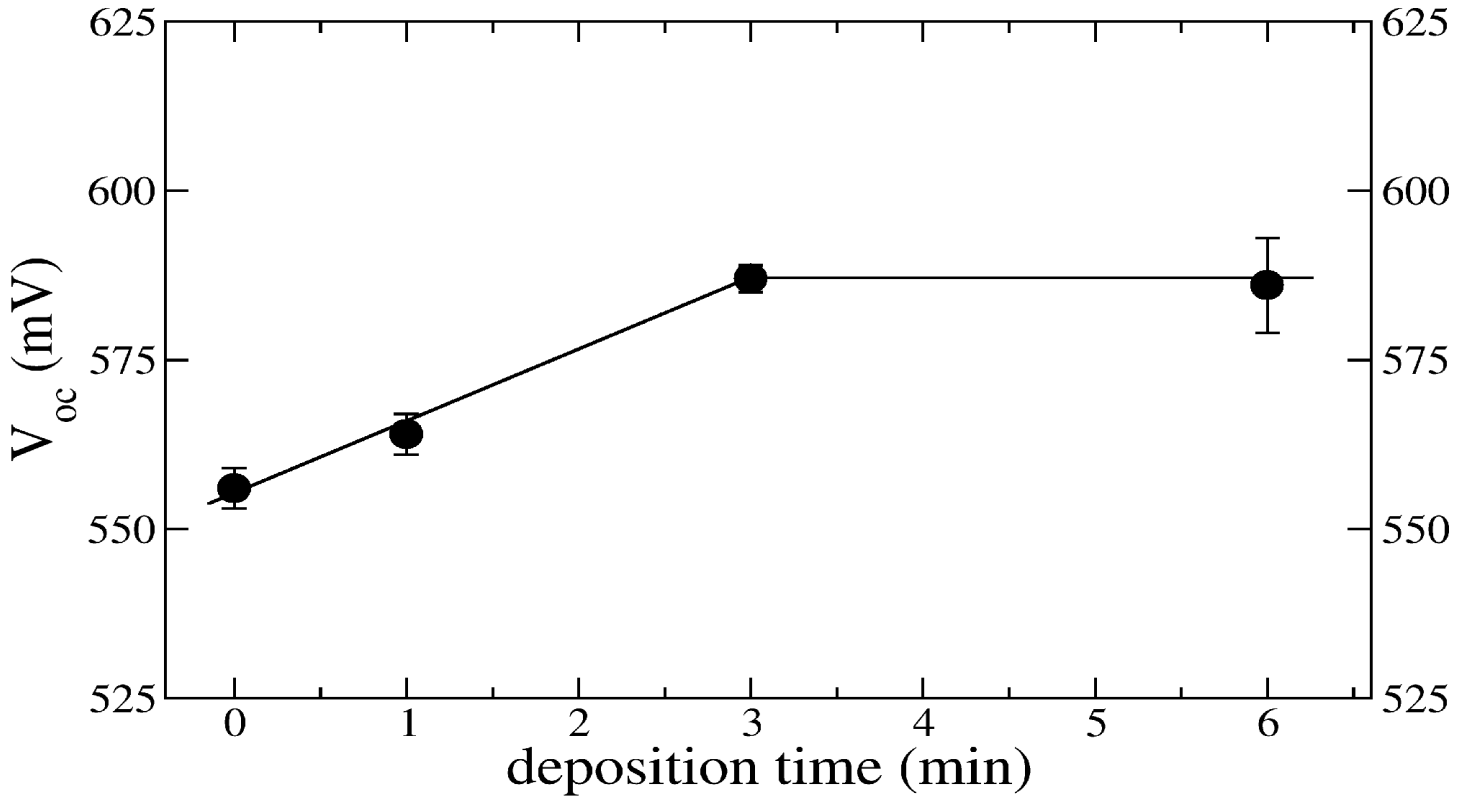
A set of heterojunction devices have been fabricated with different deposition conditions for the intrinsic *epitaxial* buffer layer

Epitaxial PECVD growth



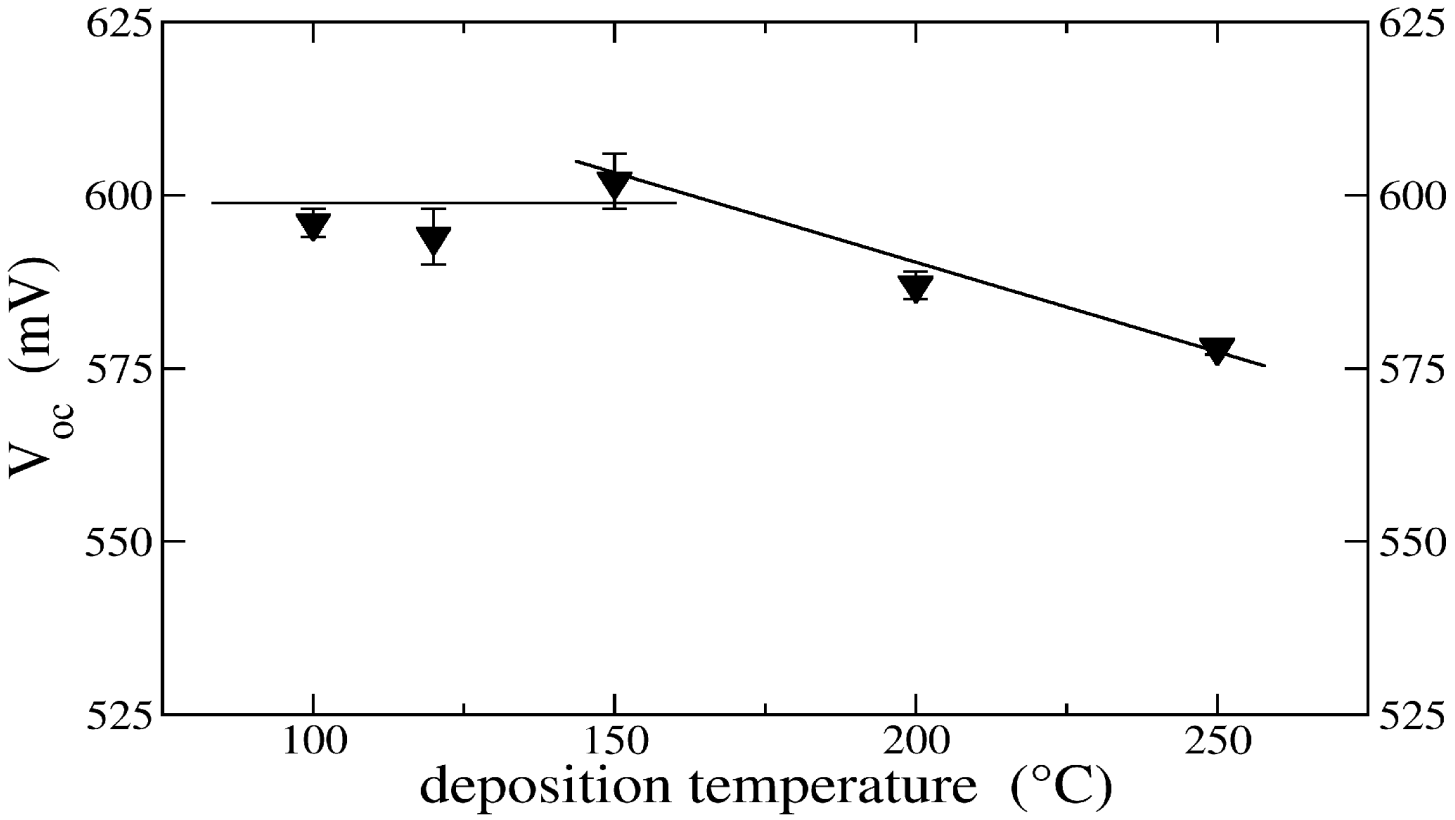
Example of epitaxial growth by PECVD.

Best conditions for epi-Si buffer layer



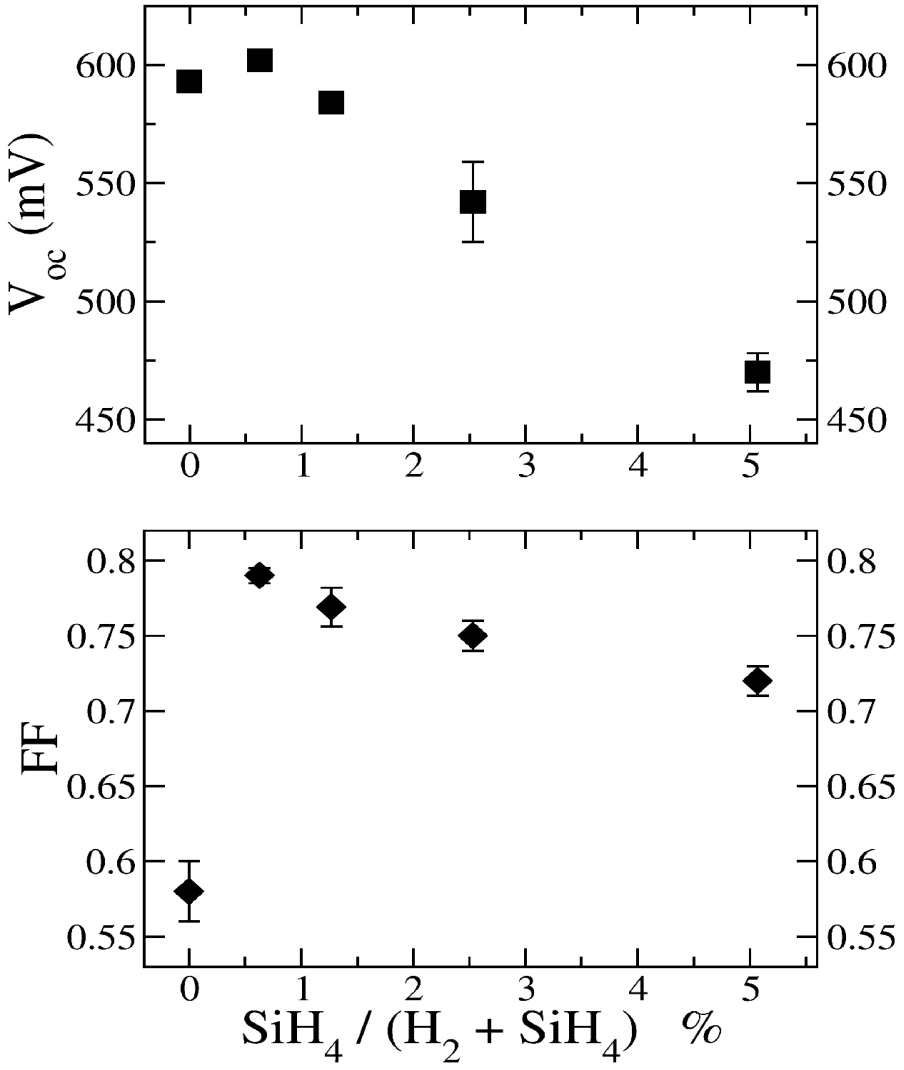
Open circuit voltage vs. i epi-Si deposition time

Best conditions for epi-Si buffer layer



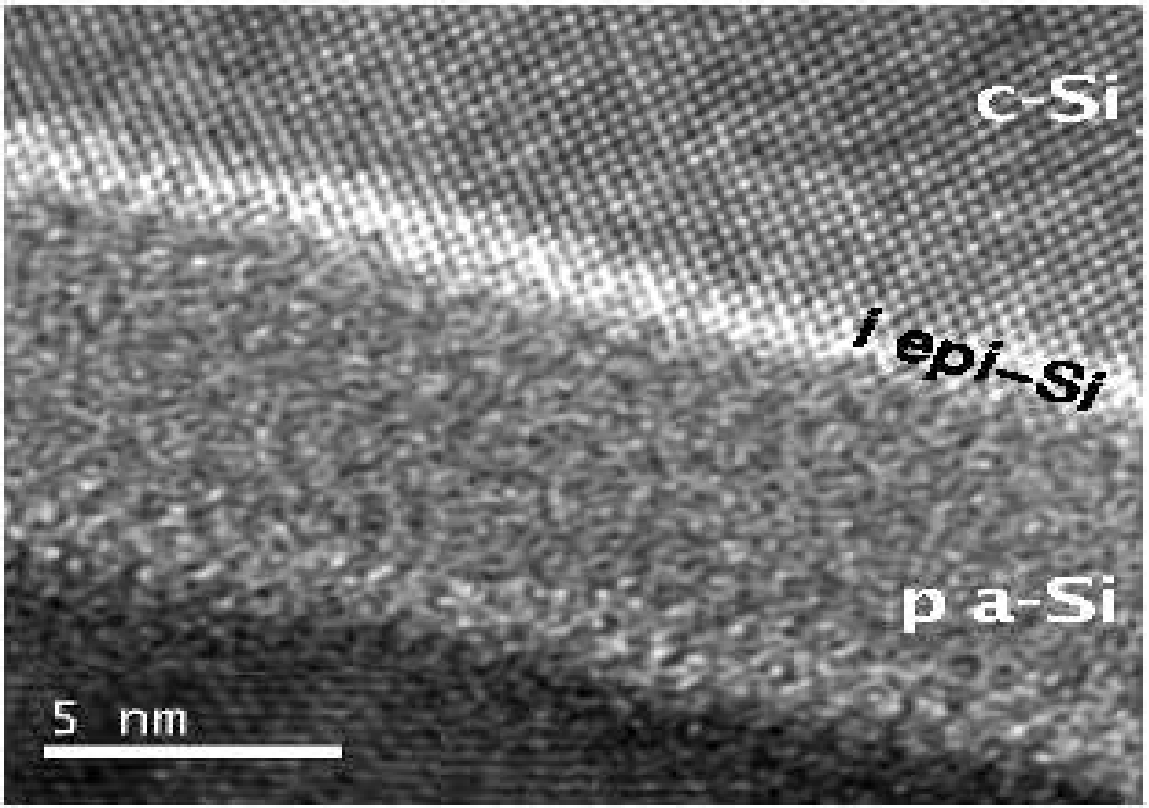
Open circuit voltage vs. i epi-Si deposition temperature

Best conditions for epi-Si buffer layer



Cell performance vs. i epi-Si silane concentration

HJ solar cells with epi-Si buffer layer

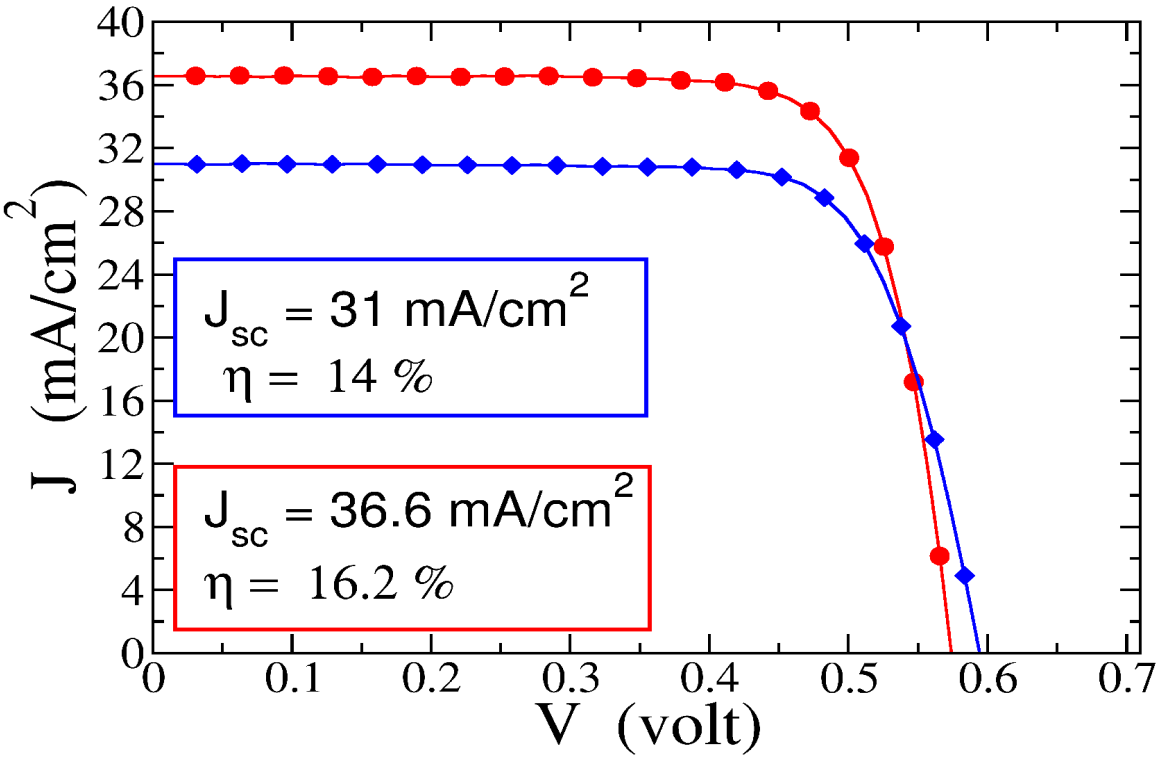


HR-TEM cross section image of
HJ solar cell with the i ***epi-Si*** layer

Epitaxial growth: condition close to chemical equilibrum i.e. etching rate close to deposition rate

The thickness of the best epi-layer is very thin: network rearrangement

HJ solar cells with epi-Si buffer layer



Using an ***i epi-Si*** buffer layer an open circuit voltage gain of 50 mV has been demonstrated

the i epi-Si buffer layer works both on flat silicon (blue) and on textured silicon (red)

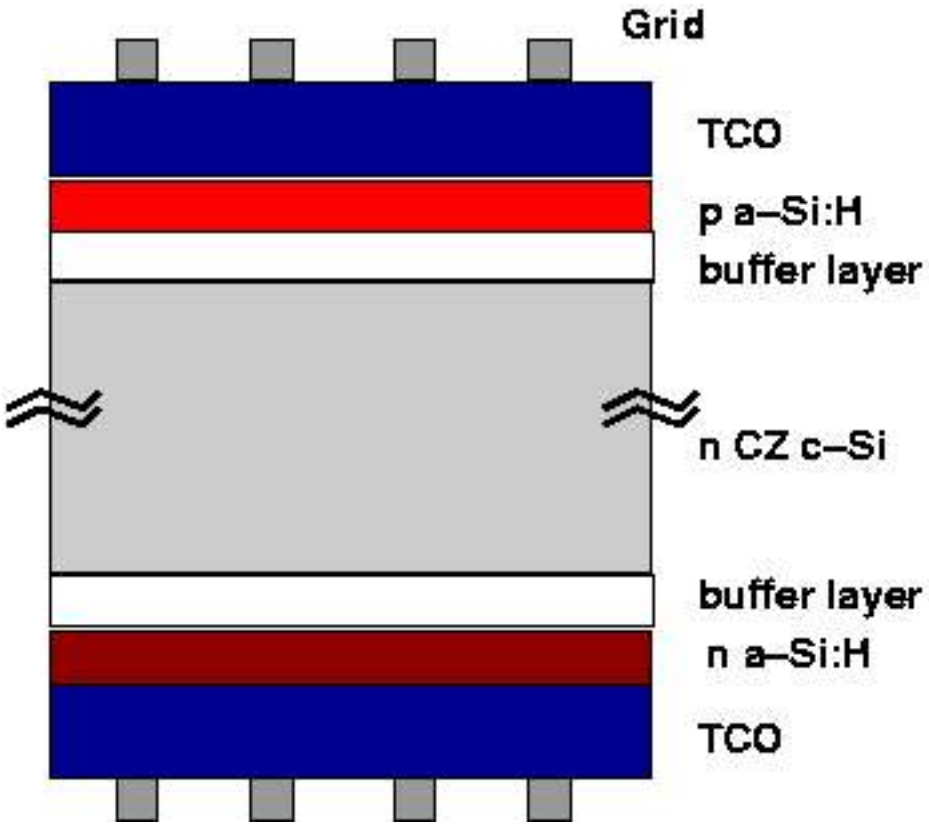
n or p type c-Si ?

Both the p a-Si / n c-Si and n a-Si / p c-Si structure can be used. Advanteges are:

n type:
band diagram more favourable
no degradation of minority carrier lifetime due to boron doping
best efficiency has been demonstrated using n type c-Si (Sanyo)
higher availability (Shell)

p type:
higher minority carrier diffusion length
patent ?

Double side heterojunction solar cell



The passivation scheme can be applied also on the back side, a further improvement of performance has been demonstrated by Sanyo

The process is simplified

The solar cell can be illuminated on both sides

Heterojunction solar cell state of the art

Sanyo: HIT 210W photovoltaic module 17 % efficiency
19.5 % mass production cell efficiency
21.5 % laboratory efficiency
n type **CZ** Si substrate, double side, **low T (< 250 C)**

Fraunhofer ISE, Germany
14 % efficiency on **p** type **CZ** Si, **low T (< 250 C)**
15 % efficiency on **p** type **FZ** Si, **low T (< 250 C)**

Hahn-Meitner Institute Berlin, Hagen Univ. Germany
17 % efficiency on **p** type **Flat FZ** Si with **BSF (800-1000 C)**

CNR-IMM Bologna Italy
16.2 % efficiency on **n** type **CZ** Si, **low T (< 250 C)**

ENEA Portici (Na) Italy
17 % efficiency on **p** type **CZ** Si **BSF (800 C)**

Conclusion

The physics of heterojunction solar cell is different from conventional solar cell, mainly because the passivating properties (energy barrier for minority carrier) of a-Si. V_{oc} for an heterojunction solar cell (up to 720 mv) is higher than V_{oc} for a conventional c-Si solar cell, better high temperature performance

The a-Si/c-Si interfaces on both sides of the device dominates the V_{oc} of the heterojunction solar cell

A buffer layer at the interfaces is necessary in order to have high V_{oc} . It is still not clear the actual nature of the buffer layer (amorphous, epitaxial, surface rearrangement)

More work needed !

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