First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

Contribution ID : 78

Type : not specified

## Laboratory Session. RVI Projects. Digital Signal Processing with FPGA.

Friday, 4 July 2008 16:30 (2:30)

Content

Summary

 Primary author(s):
 MARIA LIZ CRESPO

 Presenter(s):
 MARIA LIZ CRESPO

 Session Classification:
 Laboratory Session. RVI Projects. Digital Signal Processing with FPGA.