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First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

Tuesday 08 July 2008

**Laboratory Session. Designing Systems in Altera FPGAs Using Altera's System Level
Development Tools. (17:00-18:30)**

time	title	presenter
17:00	Laboratory Session. Designing Systems in Altera FPGAs Using Altera's System Level Development Tools.	JIMMY YEAP