Table of contents

First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

Thursday 10 July 2008

Validating the Intel Leading-Edge Architecture Microprocessor during Pre-Silicon.

(15:00-16:00)

time	title	presenter
15:00	Validating the Intel Leading-Edge Architecture Microprocessor during Pre-Silicon.	CHEW BENG WAN