First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

Contribution ID: 96 Type: not specified

SYNOPSIS Representative: Variation Aware Static Timing Analysis for sub-65nm ASIC Design

Thursday, 10 July 2008 17:30 (1:00)

Content

Summary

Session Classification: SYNOPSIS Representative: Variation Aware Static Timing Analysis for sub-65nm ASIC Design