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First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

Wednesday 18 June 2008

Laboratory Session. VHDL Simulation Environment. A design example (15:00-16:00)

time	title	presenter
15:00	Laboratory Session. VHDL Simulation Environment. A design example	MARIA LIZ CRESPO