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First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

Friday 20 June 2008

Laboratory Session. Finite State Machine: VHDL Description and Simulation (16:30-19:30)

time	title	presenter
16:30	Laboratory Session. Finite State Machine: VHDL Description and Simulation	MARIA LIZ CRESPO