The Abdus Salam
International Centre for Theoretical Physics

United Nations
Educational, Scientific and
Cultural Organization

IAEA
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1977-10

First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific

16 June - 11 July, 2008

Example.

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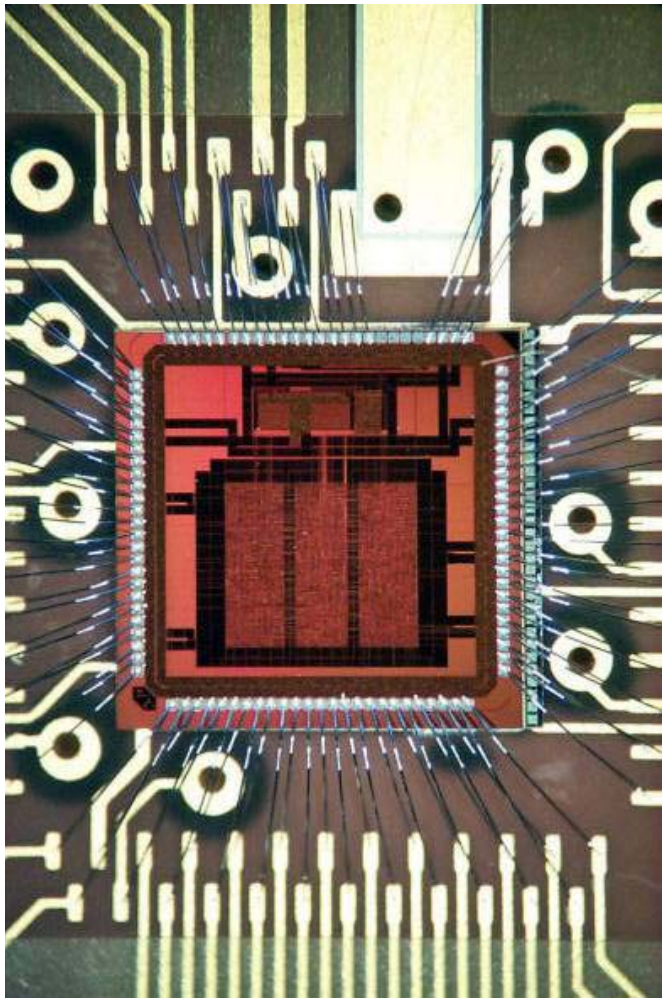
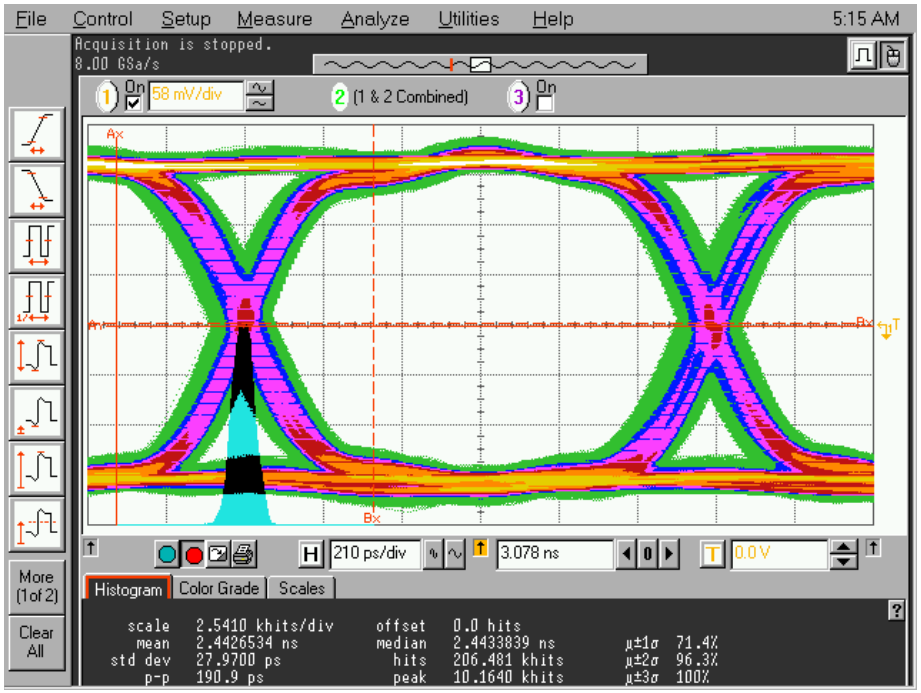
Outline

- Introduction
- Transistors
- The CMOS inverter
- Technology
- Scaling
- Gates
- Sequential circuits
- Storage elements
- Phase-Locked Loops
- Example:
  - GOL

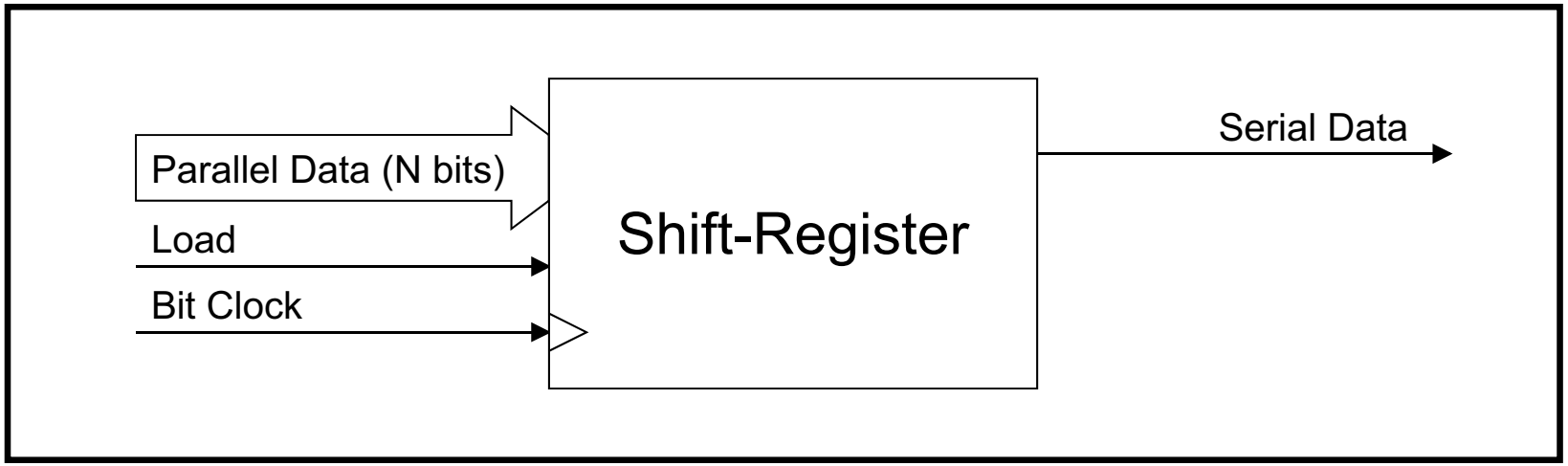


GOL – Rad tolerant Gbit/s serializer

- The GOL is a parallel-to-serial data transmitter:
  - At a rate of 40 MHz, it accepts 16 or 32-bit parallel data in
  - It generates a serial bit stream out at:
    - 0.8 Gbit/s for 16-bit in
    - 1.6 Gbit/s for 32-bit in
  - It is compatible with two standard line encoding protocols:
    - The G-Link
    - The 8B/10B
  - Two serial output drivers
    - 50 Ω differential
    - Laser/VCSEL



Data Serializers

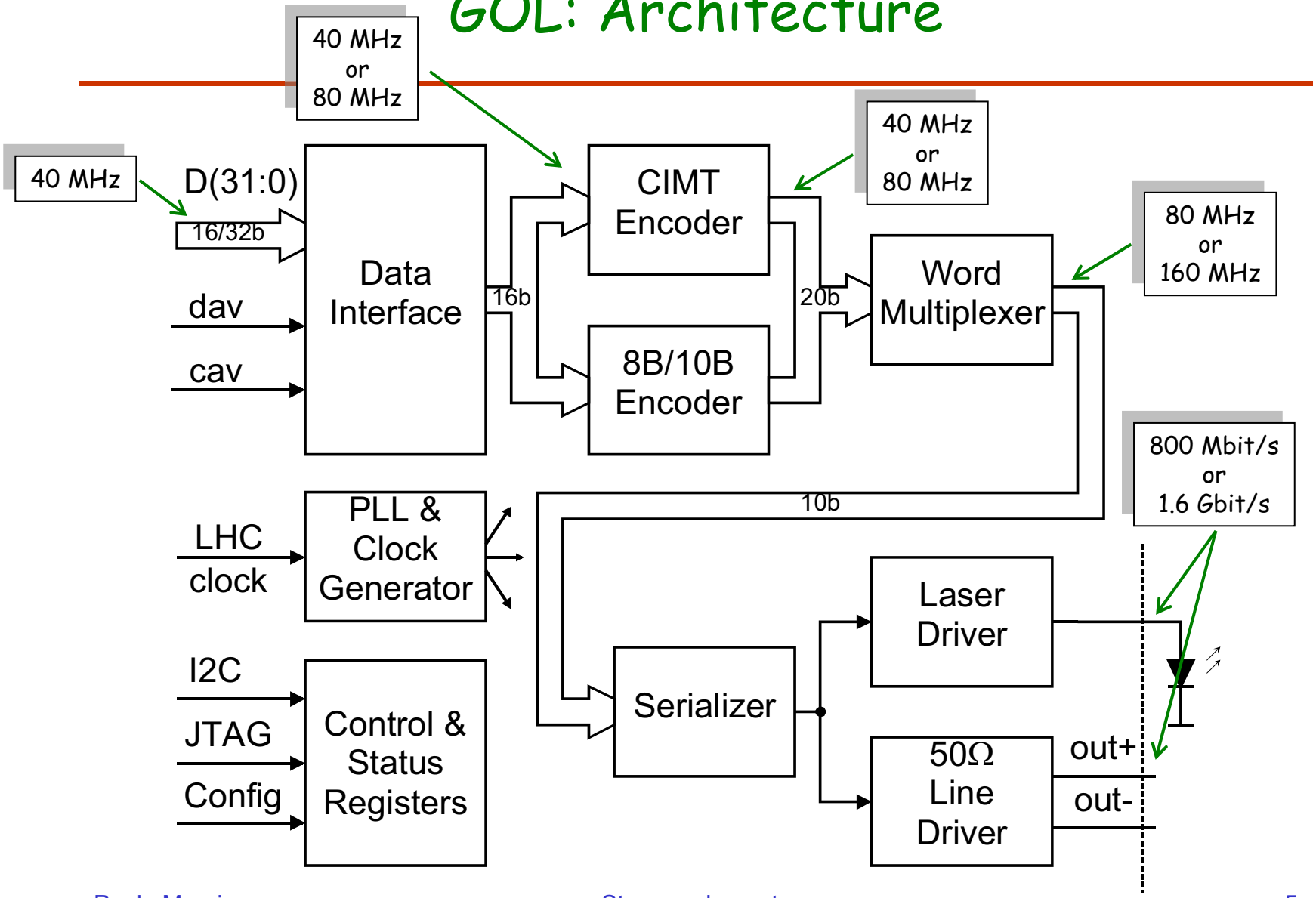


- What is a serializer?
  - A shift register!
  - Parallel loaded at the "word rate"
  - "Emptied" at the "bit rate"
  - "Bit rate" = (#bits in word) × (word rate)
- Would a simple shift register work?
  - NO!
  - There is no information about the bit boundaries (clock)
  - There is no information about the word boundaries (frame)

Data Serializers

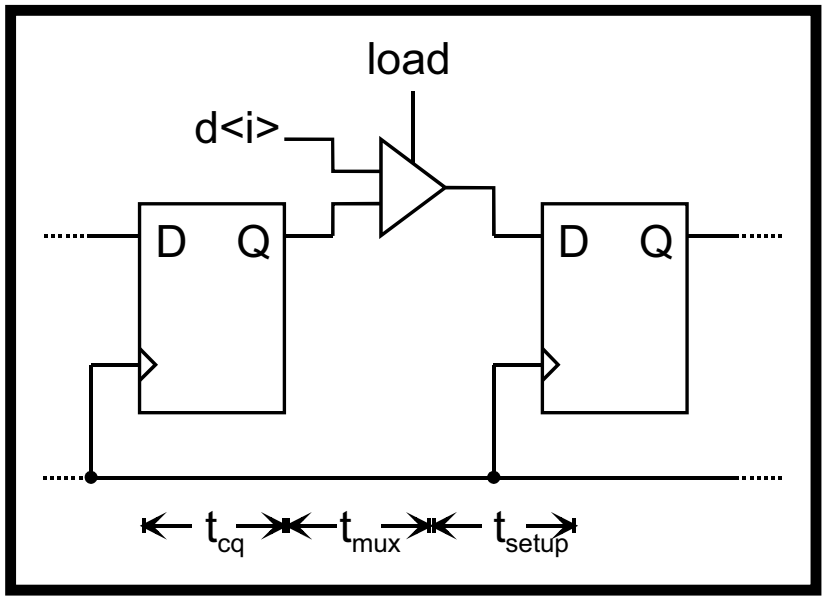
- To be useful, a serializer must convert the raw data into a "line encoded" version.
- The line code "adds":
  - A number of "redundant" bits to the word being transmitted
  - Ensuring DC signal balance
  - Ensuring enough transitions for clock recovery
  - Identifying the frame/word boundaries
  - Providing a somehow limited error checking capability
- 8B/10B word encoding
  - Each 8-bit word is mapped into a 10-bit word
  - The maximum run length is 5 (enough transitions for clock recovery)
  - Maximum unbalance between 1s and 0s is ±2
- CMIT word encoding
  - Adds 4 bits to each 16-bit word
  - Each frame has a well define master transition
  - The word to be transmitted is simply flipped or not depending on previous disparity and its own disparity

GOL: Architecture



GOL: Serializer

- Parallel-load shift register:
  - cascade of flip-flops and 2-to-1 multiplexers
- Operation speed is limited by:
  - Clock to Q delay
  - Mux delay
  - Flip-flop setup time
- Maximum frequency:
  - $1/(t_{cq} + t_{mux} + t_{setup})$

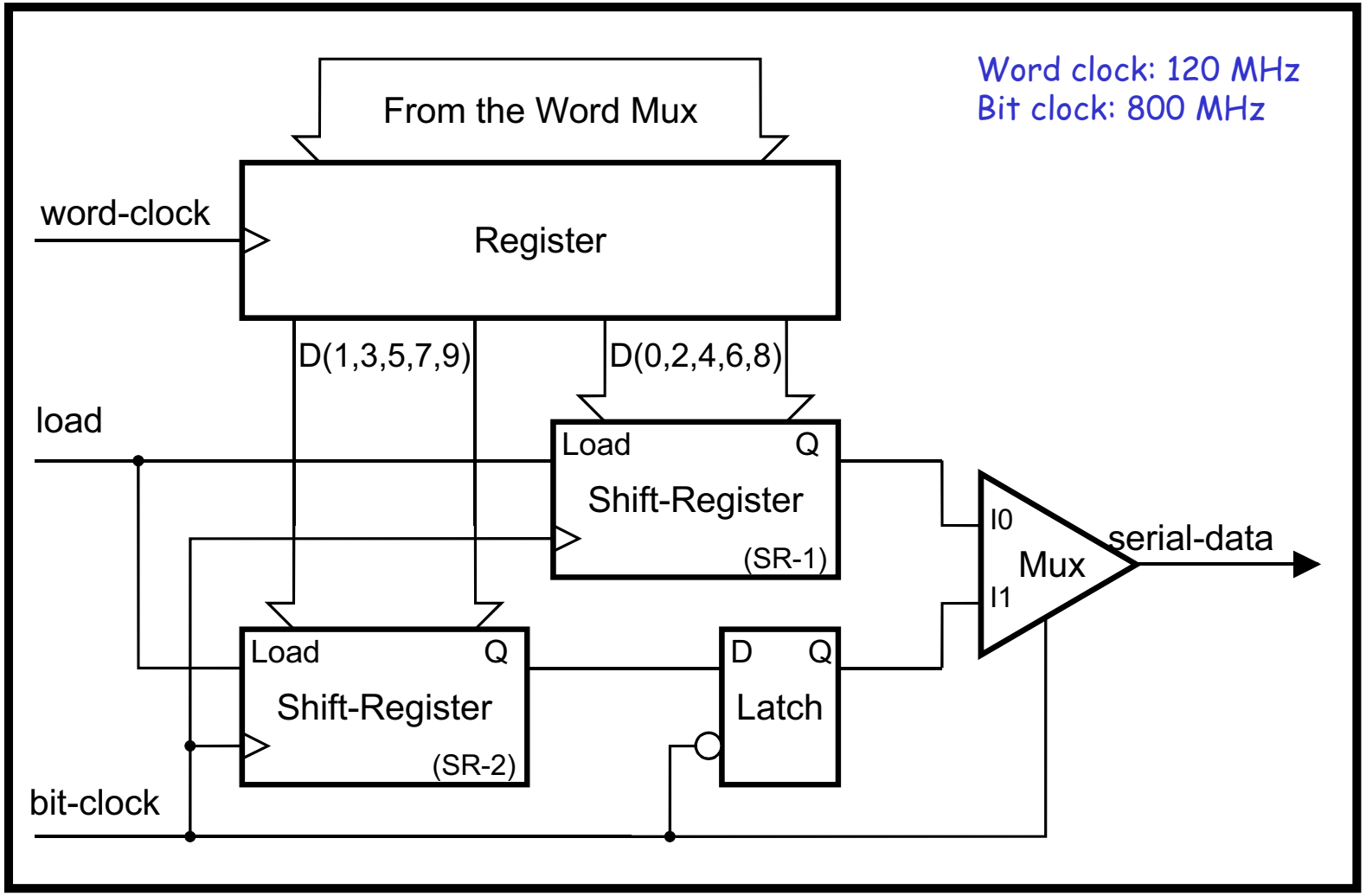


GOL: Serializer

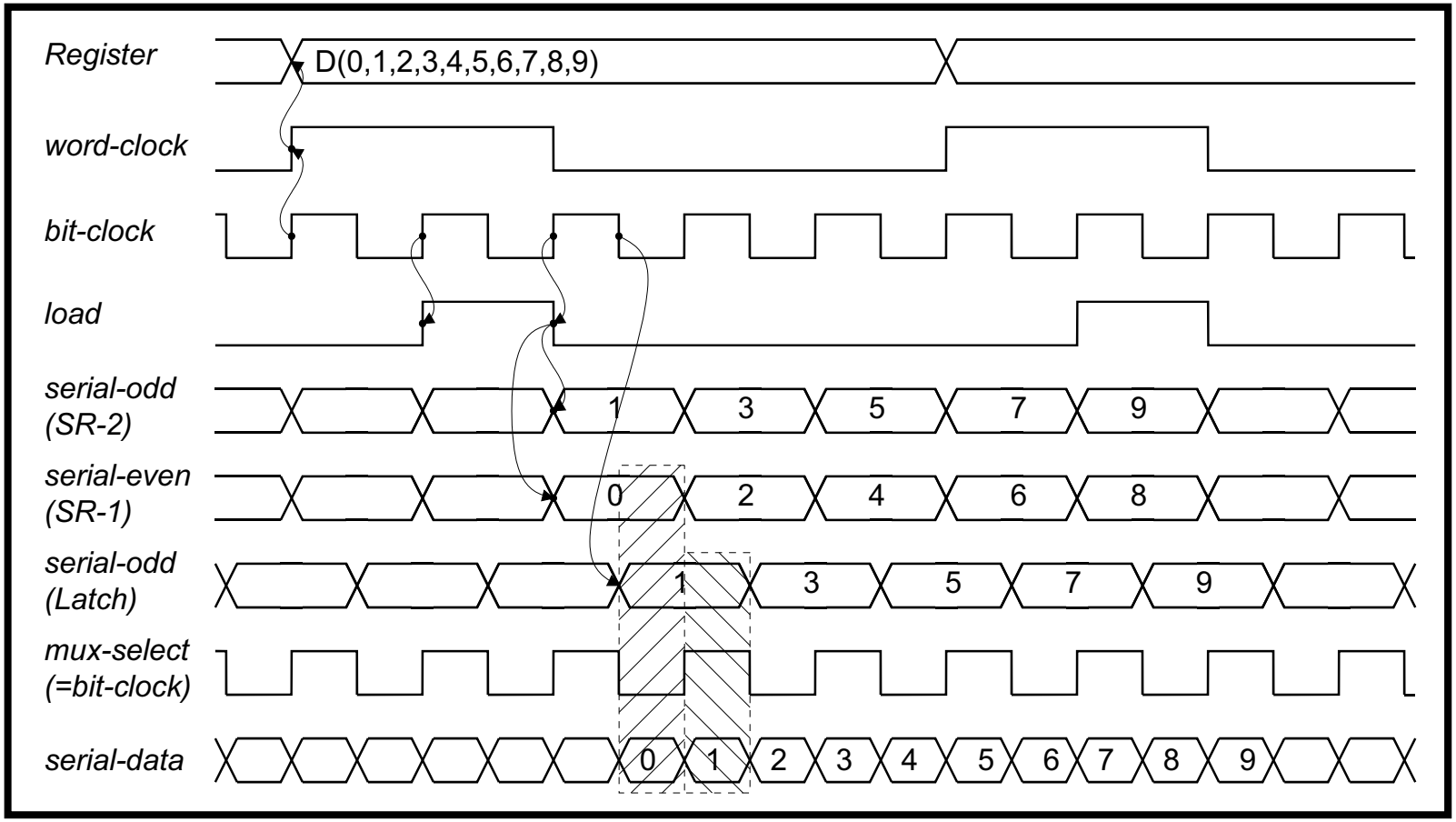
- Maximum operation speed
  - 1.6 GHz $\Rightarrow$ T = 625 ps
- Technology CMOS 0.25 μm
  - Static FF t(min) = 1292ps ! (worst case)
  - Dynamic FF t(min) = 768ps (worst case)
  - For a safe design (good yield) any of the two FF is too slow

	DFF t_{pd} (ps)	DFF t_{sup} (ps)	SFF t_{pd} (ps)	SFF t_{sup} (ps)	MUX t_{pd} (ps)
typical	145	60	309	107	104
worst	369	152	749	296	247

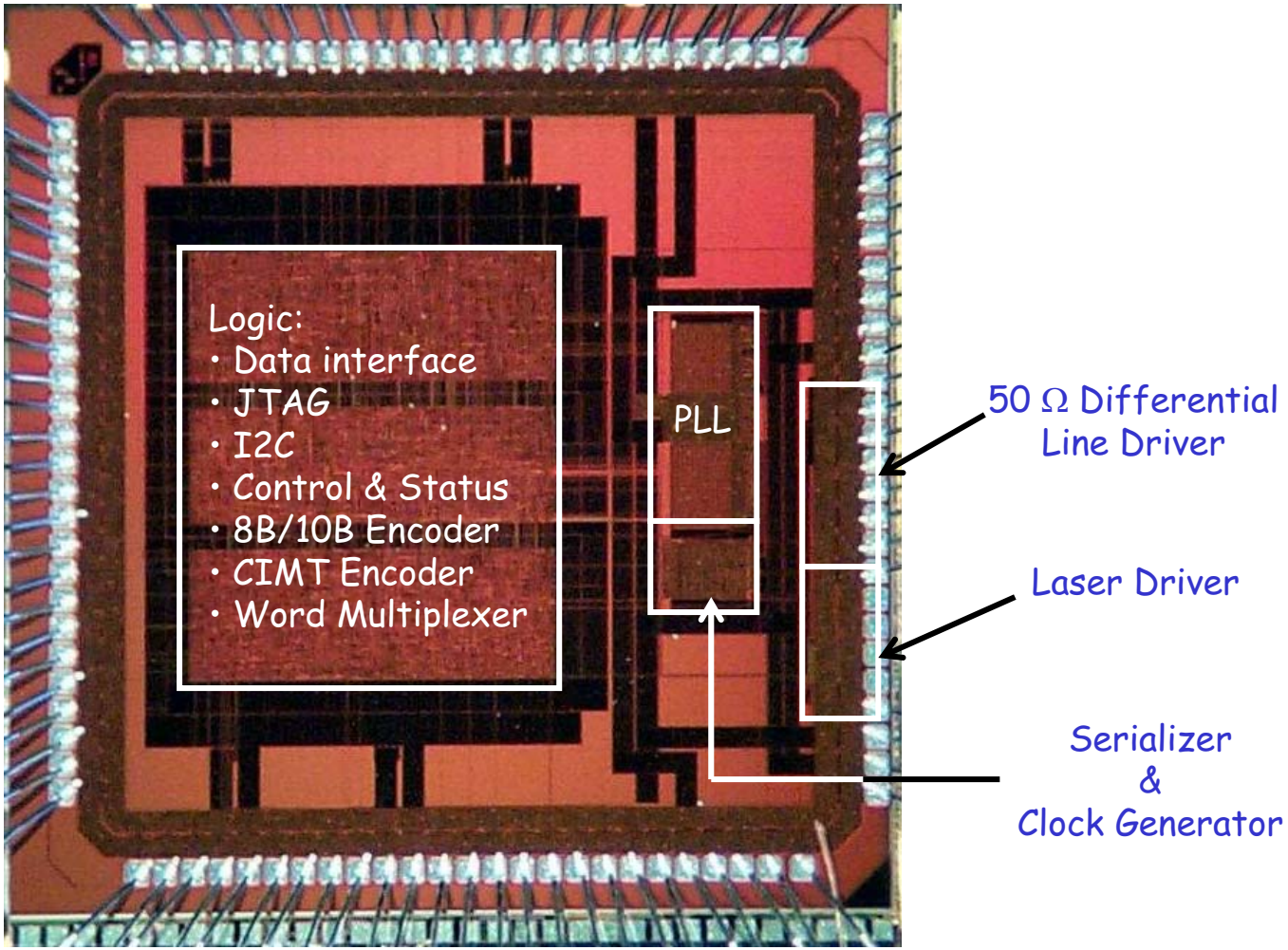
GOL: Serializer



GOL: Serializer



GOL Layout


Logic:
• Data interface
• JTAG
• I2C
• Control & Status
• 8B/10B Encoder
• CIMT Encoder
• Word Multiplexer
PLL
50 Ω Differential
Line Driver
Laser Driver
Serializer
&
Clock Generator