Table of contents

First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

Monday 23 June 2008

Laboratory Session. Parking Lot: VHDL Description, Simulation, Synthesis and Post-Synthesis Simulation (17:30-19:00)

time	title	presenter
17:30	Laboratory Session. Parking Lot: VHDL Description, Simulation, Synthesis and Post-Synthesis Simulation	MARIA LIZ CRESPO