

Laboratory Session. Implementation in the FPGA Development Platform. VHDL Package and Structural Design. Bidirectional Parallel Port Communication.

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Content

Summary

Primary author(s) : MARIA LIZ CRESPO

Presenter(s) : MARIA LIZ CRESPO

Session Classification : Laboratory Session. Implementation in the FPGA Development Platform. VHDL Package and Structural Design. Bidirectional Parallel Port Communication.