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First ICTP Regional Microelectronics Workshop and Training on VHDL for Hardware Synthesis and FPGA Design in Asia-Pacific | (smr 1977)

Monday 16 June 2008

REGISTRATION AND ADMIN FORMALITIES (08:15-09:30)

time	title	presenter
08:15	REGISTRATION AND ADMIN FORMALITIES	

Altera-MDEC FPGA Education Launch (09:30-10:15)

time	title	presenter
09:30	Altera-MDEC FPGA Education Launch	

Break (10:15-10:30)

time	title	presenter
10:15	Break	

Introduction (10:30-11:30)

time	title	presenter
10:30	Introduction	

Break (11:30-11:45)

time	title	presenter
11:30	Break	

Opening Ceremony (11:45-13:00)

time	title	presenter
11:45	Opening Ceremony	

Opening Lunch (13:00-15:00)

time	title	presenter
13:00	Opening Lunch	

Course Overview (15:00-15:30)

time	title	presenter
15:00	Course Overview	NIZAR ABDALLAH, ANDRES CICUTTIN

Effective FPGA/VLSI Education Techniques (15:30-16:30)

time	title	presenter
15:30	Effective FPGA/VLSI Education Techniques	STEPHEN BROWN

Break (16:30-17:00)

time	title	presenter
16:30	Break	

Introduction to FPGA Synthesis, Introduction to VHDL. (17:00-18:00)

time	title	presenter
17:00	Introduction to FPGA Synthesis, Introduction to VHDL.	NIZAR ABDALLAH

Introduction to Digital Design (Boolean logic) (18:00-19:00)

time	title	presenter
18:00	Introduction to Digital Design (Boolean logic)	PIROUZ BAZARGAN-SABET

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Tuesday 17 June 2008

Introduction to ACETEL Products. Libero IDE Overview and Design flow (09:30-10:30)

time	title	presenter
09:30	Introduction to ACETEL Products. Libero IDE Overview and Design flow	NIZAR ABDALLAH

Break (10:30-11:00)

time	title	presenter
10:30	Break	

Synthesis I - Introduction to VHDL (11:00-12:00)

time	title	presenter
11:00	Synthesis I - Introduction to VHDL	NIZAR ABDALLAH

Synthesis II - Introduction to VHDL (12:00-13:00)

time	title	presenter
12:00	Synthesis II - Introduction to VHDL	NIZAR ABDALLAH

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

(LiberoTM IDE) Design Entry (15:00-16:00)

time	title	presenter
15:00	(LiberoTM IDE) Design Entry	NIZAR ABDALLAH

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Digital Design I (combinatorial elements) (16:30-17:30)

time	title	presenter
16:30	Digital Design I (combinatorial elements)	PIROUZ BAZARGAN-SABET

Digital Design II (sequential elements, Mealy and Moore FSM) (17:30-19:00)

time	title	presenter
17:30	Digital Design II (sequential elements, Mealy and Moore FSM)	PIROUZ BAZARGAN-SABAT

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Wednesday 18 June 2008

(LiberoTM IDE) Functional Simulation. Synthesis (09:30-10:30)

time	title	presenter
09:30	(LiberoTM IDE) Functional Simulation. Synthesis	NIZAR ABDALLAH

Break (10:30-11:00)

time	title	presenter
10:30	Break	

Synthesis III - Advanced VHDL (11:00-12:00)

time	title	presenter
11:00	Synthesis III - Advanced VHDL	NIZAR ABDALLAH

Digital Design III (more complex elements: RAM, ROM, buses, pipeline concept, etc) (12:00-13:00)

time	title	presenter
12:00	Digital Design III (more complex elements: RAM, ROM, buses, pipeline concept, etc)	PIROUZ BAZARGAN-SABAT

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Laboratory Session. VHDL Simulation Environment. A design example (15:00-16:00)

time	title	presenter
15:00	Laboratory Session. VHDL Simulation Environment. A design example	MARIA LIZ CRESPO

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Laboratory Session. VHDL Simulation Environment. A design example. Contd. (16:30-19:00)

time	title	presenter
16:30	Laboratory Session. VHDL Simulation Environment. A design example. Contd.	MARIA LIZ CRESPO

Dinner (19:00-21:00)

time	title	presenter
19:00	Dinner	

Thursday 19 June 2008

(LiberoTM IDE) Place & Route (09:30-10:30)

time	title	presenter
09:30	(LiberoTM IDE) Place & Route	NIZAR ABDALLAH

Break (10:30-11:00)

time	title	presenter
10:30	Break	

Digital arithmetic I (number representations) (11:00-12:00)

time	title	presenter
11:00	Digital arithmetic I (number representations)	PIROUZ BAZARGAN-SABET

Digital arithmetic II (basic arithmetic operations) (12:00-13:00)

time	title	presenter
12:00	Digital arithmetic II (basic arithmetic operations)	PIROUZ BAZARGAN-SABAT

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Laboratory Session. VHDL Behavioral Description and Simulation of Combinational Circuits (15:00-16:00)

time	title	presenter
15:00	Laboratory Session. VHDL Behavioral Description and Simulation of Combinational Circuits	MARIA LIZ CRESPO

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Laboratory Session. VHDL Behavioral Description and Simulation of Combinational Circuits. Contd. (16:30-19:00)

time	title	presenter

16:30	Laboratory Session. VHDL Behavioral Description and Simulation of Combinational Circuits. Contd.	MARIA LIZ CRESPO

Dinner (20:00-20:00)

time	title	presenter
20:00	Dinner	

Friday 20 June 2008

Design Verification and Timing Concepts (09:30-10:30)

time	title	presenter
09:30	Design Verification and Timing Concepts	NIZAR ABDALLAH

Break (10:30-11:00)

time	title	presenter
10:30	Break	

(LiberoTM IDE) Timing Constraints and Analysis (11:00-12:00)

time	title	presenter
11:00	(LiberoTM IDE) Timing Constraints and Analysis	NIZAR ABDALLAH

Laboratory Session. VHDL Behavioral Description and Simulation of Sequential Circuits (12:00-13:00)

time	title	presenter
12:00	Laboratory Session. VHDL Behavioral Description and Simulation of Sequential Circuits	MARIA LIZ CRESPO

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Laboratory Session. VHDL Behavioral Description and Simulation of Sequential Circuits (15:00-16:00)

time	title	presenter
15:00	Laboratory Session. VHDL Behavioral Description and Simulation of Sequential Circuits	MARIA LIZ CRESPO

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Laboratory Session. Finite State Machine: VHDL Description and Simulation (16:30-19:30)

time	title	presenter
16:30	Laboratory Session. Finite State Machine: VHDL Description and Simulation	MARIA LIZ CRESPO

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Monday 23 June 2008

Programmable logic & FPGA architectures (09:30-10:30)

time	title	presenter
09:30	Programmable logic & FPGA architectures	NIZAR ABDALLAH

Break (10:30-11:00)

time	title	presenter
10:30	Break	

(LiberoTM IDE) Post-Layout Simulation. Programming (11:00-12:00)

time	title	presenter
11:00	(LiberoTM IDE) Post-Layout Simulation. Programming	NIZAR ABDALLAH

Microelectronics at CERN (12:00-13:00)

time	title	presenter
12:00	Microelectronics at CERN	PAULO MOREIRA

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Introduction to CMOS technology and VLSI design (15:00-16:00)

time	title	presenter
15:00	Introduction to CMOS technology and VLSI design	PAULO MOREIRA

Break (16:00-16:30)

time	title	presenter
16:00	Break	

CMOS Technology I (16:30-17:30)

time	title	presenter
16:30	CMOS Technology I	PAULO MOREIRA

Laboratory Session. Parking Lot: VHDL Description, Simulation, Synthesis and Post-Synthesis Simulation (17:30-19:00)

time	title	presenter
17:30	Laboratory Session. Parking Lot: VHDL Description, Simulation, Synthesis and Post-Synthesis Simulation	MARIA LIZ CRESPO

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Tuesday 24 June 2008

Actel Flash FPGA architecture (09:30-10:30)

time	title	presenter
09:30	Actel Flash FPGA architecture	NIZAR ABDALLAH

Break (10:30-11:00)

time	title	presenter
10:30	Break	

System-on-Chip concepts (11:00-12:00)

time	title	presenter
11:00	System-on-Chip concepts	NIZAR ABDALLAH

CMOS Technology II (12:00-13:00)

time	title	presenter
12:00	CMOS Technology II	PAULO MOREIRA

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

VLSI Design I (15:00-16:00)

time	title	presenter
15:00	VLSI Design I	PAULO MOREIRA

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Advance FPGA Applications (16:30-17:30)

time	title	presenter
16:30	Advance FPGA Applications	ALEXANDER KLUGE

Laboratory Session. Hardware Description of the FPGA Development Platform. FPGA Implementation Example. (17:30-20:00)

time	title	presenter
17:30	Laboratory Session. Hardware Description of the FPGA Development Platform. FPGA Implementation Example.	CARLOS SOSA PAEZ

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Wednesday 25 June 2008

DEMO Actel Fusion Evaluation Board (09:30-10:30)

time	title	presenter
09:30	DEMO Actel Fusion Evaluation Board	NIZAR ABDALLAH

Break (10:30-11:00)

time	title	presenter
10:30	Break	

VLSI design II (11:00-12:00)

time	title	presenter
11:00	VLSI design II	PAULO MOREIRA

Advance FPGA applications. A case study in HEP experiments (12:00-13:00)

time	title	presenter
12:00	Advance FPGA applications. A case study in HEP experiments	ALEXANDER KLUGE

Break (13:00-15:00)

time	title	presenter
13:00	Break	

Advance FPGA applications. A case study in HEP experiments (contd) (15:00-16:00)

time	title	presenter
15:00	Advance FPGA applications. A case study in HEP experiments (contd)	ALEXANDER KLUGE

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Laboratory Session. Hardware Description of the FPGA Development Platform. FPGA Implementation Example. (cont) (16:30-19:00)

time	title	presenter
16:30	Laboratory Session. Hardware Description of the FPGA Development Platform. FPGA Implementation Example. (cont)	CARLOS SOSA PAEZ

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Thursday 26 June 2008

Introduction to Fourier Theory (09:30-10:30)

time	title	presenter
09:30	Introduction to Fourier Theory	MARCELO MAGNASCO

Break (10:30-11:00)

time	title	presenter
10:30	Break	

Fourier Theory I (11:00-12:00)

time	title	presenter
11:00	Fourier Theory I	MARCELO MAGNASCO

Fourier Theory II (12:00-13:00)

time	title	presenter
12:00	Fourier Theory II	MARCELO MAGNASCO

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Laboratory Session. Synthesis, Pos-Synthesis Simulation and Implementation in the FPGA Development Platform (cont) (15:00-16:00)

time	title	presenter
15:00	Laboratory Session. Synthesis, Pos-Synthesis Simulation and Implementation in the FPGA Development Platform (cont)	MARIA LIZ CRESPO

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Laboratory Session. Synthesis, Pos-Synthesis Simulation and Implementation on the FPGA Development Platform (cont.) (16:30-19:00)

time	title	presenter

16:30	Laboratory Session. Synthesis, Pos-Synthesis Simulation and Implementation on the FPGA Development Platform (cont.)	MARIA LIZ CRESPO

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Friday 27 June 2008

Introduction to Digital Signal Processing (09:30-10:30)

time	title	presenter
09:30	Introduction to Digital Signal Processing	MARCELO MAGNASCO

Break (10:30-11:00)

time	title	presenter
10:30	Break	

Digital Signal Processing I (11:00-13:00)

time	title	presenter
11:00	Digital Signal Processing I	MARCELO MAGNASCO

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Laboratory Session. Implementation in the FPGA Development Platform. VHDL Package and Structural Design. (15:00-16:00)

time	title	presenter
15:00	Laboratory Session. Implementation in the FPGA Development Platform. VHDL Package and Structural Design.	MARIA LIZ CRESPO

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Laboratory Session. Implementation in the FPGA Development Platform. VHDL Package and Structural Design. Bidirectional Parallel Port Communication. (16:30-19:00)

time	title	presenter
16:30	Laboratory Session. Implementation in the FPGA Development Platform. VHDL Package and Structural Design. Bidirectional Parallel Port Communication.	MARIA LIZ CRESPO

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Monday 30 June 2008

Selected topics on Logic Synthesis and FPGA Debugging (09:30-10:30)

time	title	presenter
09:30	Selected topics on Logic Synthesis and FPGA Debugging	ANDRES CICUTTIN

Break (10:30-11:00)

time	title	presenter
10:30	Break	

Selected topics on Logic Synthesis and FPGA Debugging (cont.) (11:00-12:00)

time	title	presenter
11:00	Selected topics on Logic Synthesis and FPGA Debugging (cont.)	ANDRES CICUTTIN

Laboratory Session. Implementation in the FPGA Development Platform. Bidirectional Parallel Port Communication. (12:00-13:00)

time	title	presenter
12:00	Laboratory Session. Implementation in the FPGA Development Platform. Bidirectional Parallel Port Communication.	MARIA LIZ CRESPO

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Laboratory Session. Implementation on the FPGA Development Platform. Digital Arithmetic (cont.) (15:00-16:00)

time	title	presenter
15:00	Laboratory Session. Implementation on the FPGA Development Platform. Digital Arithmetic (cont.)	MARIA LIZ CRESPO

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Laboratory Session. Implementation on the FPGA Development Platform. Digital Arithmetic (cont.) (16:30-19:00)

time	title	presenter
16:30	Laboratory Session. Implementation on the FPGA Development Platform. Digital Arithmetic (cont.)	MARIA LIZ CRESPO

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Tuesday 01 July 2008

Models, Mechanics, and Opportunities for Collaborative Engineering and Design in the New Cyber Age. I (09:30-10:30)

time	title	presenter
09:30	Models, Mechanics, and Opportunities for Collaborative Engineering and Design in the New Cyber Age. I	KHAN JAVED IQBAL

Break (10:30-11:00)

time	title	presenter
10:30	Break	

Models, Mechanics, and Opportunities for Collaborative Engineering and Design in the New Cyber Age. II (11:00-12:00)

time	title	presenter
11:00	Models, Mechanics, and Opportunities for Collaborative Engineering and Design in the New Cyber Age. II	KHAN JAVED IQBAL

Reconfigurable Virtual Instrumentation (RVI) based on FPGA (12:00-13:00)

time	title	presenter
12:00	Reconfigurable Virtual Instrumentation (RVI) based on FPGA	ANDRES CICUTTIN

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Reconfigurable Virtual Instrumentation (RVI) based on FPGA (cont.) (15:00-16:00)

time	title	presenter
15:00	Reconfigurable Virtual Instrumentation (RVI) based on FPGA (cont.)	ANDRES CICUTTIN

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Laboratory Session. DEMO: ICTP RVI Platform. Virtual Instruments: Digital Oscilloscope and Waveform Generator. (16:30-19:00)

time	title	presenter
16:30	Laboratory Session. DEMO: ICTP RVI Platform. Virtual Instruments: Digital Oscilloscope and Waveform Generator.	MIGUEL RISCO CASTILLO

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Wednesday 02 July 2008

Introduction to two-dimensional digital signal processing. (09:30-10:30)

time	title	presenter
09:30	Introduction to two-dimensional digital signal processing.	FABIO MAMMANO

Break (10:30-11:00)

time	title	presenter
10:30	Break	

Two-dimensional digital signal processing I. (11:00-12:00)

time	title	presenter
11:00	Two-dimensional digital signal processing I.	FABIO MAMMANO

Laboratory Session. DEMO: ICTP RVI Platform. Virtual Instruments: Digital Oscilloscope and Waveform Generator (cont.) (12:00-13:00)

time	title	presenter
12:00	Laboratory Session. DEMO: ICTP RVI Platform. Virtual Instruments: Digital Oscilloscope and Waveform Generator (cont.)	MIGUEL RISCO CASTILLO

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Laboratory Session. RVI Architecture. Integration of new blocks (15:00-16:00)

time	title	presenter
15:00	Laboratory Session. RVI Architecture. Integration of new blocks	MIGUEL RISCO CASTILLO

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Laboratory Session. DEMO: ICTP RVI Platform. Virtual Instruments: Digital Oscilloscope and Waveform Generation. (16:30-19:00)

time	title	presenter

16:30	Laboratory Session. DEMO: ICTP RVI Platform. Virtual Instruments: Digital Oscilloscope and Waveform Generation.	MIGUEL RISCO CASTILLO

Dinner (20:00-20:00)

time	title	presenter
20:00	Dinner	

Thursday 03 July 2008

Two-dimensional digital signal processing II. Three-dimensional deconvolution in FPGA I (09:30-10:30)

time	title	presenter
09:30	Two-dimensional digital signal processing II. Three-dimensional deconvolution in FPGA I	FABIO MAMMANO

Break (10:30-11:00)

time	title	presenter
10:30	Break	

Two-dimensional digital signal processing III. Three-dimensional deconvolution in FPGA II (11:00-12:00)

time	title	presenter
11:00	Two-dimensional digital signal processing III. Three-dimensional deconvolution in FPGA II	FABIO MAMMANO

Laboratory Session. RVI Projects. Digital Signal Processing with FPGA (12:00-13:00)

time	title	presenter
12:00	Laboratory Session. RVI Projects. Digital Signal Processing with FPGA	MARIA LIZ CRESPO

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Laboratory Session. RVI Projects. Digital Signal Processing with FPGA. (15:00-16:00)

time	title	presenter
15:00	Laboratory Session. RVI Projects. Digital Signal Processing with FPGA.	MARIA LIZ CRESPO

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Laboratory Session. RVI Projects. Digital Signal Processing with FPGA (16:30-19:00)

time	title	presenter
16:30	Laboratory Session. RVI Projects. Digital Signal Processing with FPGA	MARIA LIZ CRESPO

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Friday 04 July 2008

Laboratory Session. RVI Projects. Digital Signal Processing with FPGA. (09:30-10:30)

time	title	presenter
09:30	Laboratory Session. RVI Projects. Digital Signal Processing with FPGA.	MARIA LIZ CRESPO

Break (10:30-11:00)

time	title	presenter
10:30	Break	

Laboratory Session. RVI Projects. Digital Signal Processing with FPGA (11:00-13:00)

time	title	presenter
11:00	Laboratory Session. RVI Projects. Digital Signal Processing with FPGA	MARIA LIZ CRESPO

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Laboratory Session. RVI Projects. Digital Signal Processing with FPGA. (15:00-16:00)

time	title	presenter
15:00	Laboratory Session. RVI Projects. Digital Signal Processing with FPGA.	MARIA LIZ CRESPO

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Laboratory Session. RVI Projects. Digital Signal Processing with FPGA. (16:30-19:00)

time	title	presenter
16:30	Laboratory Session. RVI Projects. Digital Signal Processing with FPGA.	MARIA LIZ CRESPO

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Monday 07 July 2008

System Design: Is Hardware Becoming Software? (09:30-11:00)

time	title	presenter
09:30	System Design: Is Hardware Becoming Software?	CHRIS OH

Break (11:00-11:30)

time	title	presenter
11:00	Break	

Laboratory Session. Introduction to designing FPGAs with Quartus II and Altera Development Kits (11:30-13:00)

time	title	presenter
11:30	Laboratory Session. Introduction to designing FPGAs with Quartus II and Altera Development Kits	KING KEONG WONG, THIAM SIN LAI

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Laboratory Session. Introduction to designing FPGAs with Quartus II and Altera Development Kits (15:00-16:00)

time	title	presenter
15:00	Laboratory Session. Introduction to designing FPGAs with Quartus II and Altera Development Kits	KING KEONG WANG, THIAM SIN LAI

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Laboratory Session. Introduction to designing FPGAs with Quartus II and Altera Development Kits (16:30-18:00)

time	title	presenter
16:30	Laboratory Session. Introduction to designing FPGAs with Quartus II and Altera Development Kits	KING KEONG WANG, THIAM SIN LAI

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Tuesday 08 July 2008

Formal Verification Techniques for FPGA (09:30-11:00)

time	title	presenter
09:30	Formal Verification Techniques for FPGA	ELISHA LYE

- (11:00-11:30)

time	title	presenter
11:00	-	

Laboratory Session. Designing Systems in Altera FPGAs Using Altera\'s System Level Development Tools. (11:30-13:00)

time	title	presenter
11:30	Laboratory Session. Designing Systems in Altera FPGAs Using Altera\'s System Level Development Tools.	. JIMMY YEAP

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Laboratory Session. Designing Systems in Altera FPGAs Using Altera\'s System Level Development Tools. (15:00-16:30)

time	title	presenter
15:00	Laboratory Session. Designing Systems in Altera FPGAs Using Altera\'s System Level Development Tools.	JIMMY YEAP

Break (16:30-17:00)

time	title	presenter
16:30	Break	

Laboratory Session. Designing Systems in Altera FPGAs Using Altera\'s System Level Development Tools. (17:00-18:30)

time	title	presenter
17:00	Laboratory Session. Designing Systems in Altera FPGAs Using Altera\'s System Level Development Tools.	JIMMY YEAP

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Wednesday 09 July 2008

An Overview of Microprocessor Architecture &. Implementation of a Large Bus Size VLIW Microprocessor on FPGA (09:30-10:30)

time	title	presenter
09:30	An Overview of Microprocessor Architecture &. Implementation of a Large Bus Size VLIW Microprocessor on FPGA	WENG FOOK LEE

Break (10:30-11:00)

time	title	presenter
10:30	Break	

An Overview of Microprocessor Architecture & Implementation of a Large Bus Size VLIW Microprocessor on FPGA. (11:00-12:00)

time	title	presenter
11:00	An Overview of Microprocessor Architecture & Implementation of a Large Bus Size VLIW Microprocessor on FPGA.	

Laboratory Session. Digital Design and Implementation on FPGA Using Mentor Graphics\' FPGA Advantage (12:00-13:00)

time	title	presenter
12:00	Laboratory Session. Digital Design and Implementation on FPGA Using Mentor Graphics\' FPGA Advantage	CHOONG YEE LEE

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Laboratory Session. Digital Design and Implementation on FPGA Using Mentor Graphics\' FPGA Advantage (15:00-16:00)

time	title	presenter
15:00	Laboratory Session. Digital Design and Implementation on FPGA Using Mentor Graphics\' FPGA Advantage	CHOONG YEE LEE

Break (16:00-16:30)

time	title	presenter

16:00	Break	

Laboratory Session. Digital Design and Implementation on FPGA Using Mentor Graphics\' FPGA Advantage (16:30-18:00)

time	title	presenter
16:30	Laboratory Session. Digital Design and Implementation on FPGA Using Mentor Graphics\' FPGA Advantage	CHOONG YEE LEE

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Thursday 10 July 2008

Validating the Intel Leading-Edge Architecture Microprocessor during Pre-Silicon (09:30-10:30)

time	title	presenter
09:30	Validating the Intel Leading-Edge Architecture Microprocessor during Pre-Silicon	CHEW BENG WAH

Break (10:30-11:00)

time	title	presenter
10:30	Break	

Validating the Intel Leading-Edge Architecture Microprocessor during Pre-Silicon (11:00-13:00)

time	title	presenter
11:00	Validating the Intel Leading-Edge Architecture Microprocessor during Pre-Silicon	CHEW BENG WAH

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Validating the Intel Leading-Edge Architecture Microprocessor during Pre-Silicon. (15:00-16:00)

time	title	presenter
15:00	Validating the Intel Leading-Edge Architecture Microprocessor during Pre-Silicon.	CHEW BENG WAN

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Challenges in Low Power Design (16:30-17:30)

time	title	presenter
16:30	Challenges in Low Power Design	JASMINE NG

SYNOPSIS Representative: Variation Aware Static Timing Analysis for sub-65nm ASIC Design (17:30-18:30)

time	title	presenter
17:30	SYNOPSIS Representative: Variation Aware Static Timing Analysis for sub-65nm ASIC Design	

Dinner (20:00-22:00)

time	title	presenter
20:00	Dinner	

Friday 11 July 2008

SYNOPSIS Representative: Variation Aware Static Timing Analysis for sub-65nm ASIC Design (09:30-10:30)

time	title	presenter
09:30	SYNOPSIS Representative: Variation Aware Static Timing Analysis for sub-65nm ASIC Design	

Break proceed to Sport Complex (UA113) (10:30-11:00)

time	title	presenter
10:30	Break proceed to Sport Complex (UA113)	

Closing Ceremony (UA113, Sport Complex) (11:00-13:00)

time	title	presenter
11:00	Closing Ceremony (UA113, Sport Complex)	

Lunch (13:00-15:00)

time	title	presenter
13:00	Lunch	

Certificates of Participation (DK E) (15:00-16:00)

time	title	presenter
15:00	Certificates of Participation (DK E)	

Break (16:00-16:30)

time	title	presenter
16:00	Break	

Open Discussion (16:30-18:30)

time	title	presenter
16:30	Open Discussion	

Dinner (20:00-22:00)

time	title	presenter

20:00	Dinner	