



2025-7

Satellite Navigation Science and Technology for Africa

23 March - 9 April, 2009

Introduction to GPS Receiver Design Principles (Part 4)

> Ward Phillip. W. Navward U.S.A

### Session IV Carrier tracking loop design

- Generic GPS receiver carrier tracking loop block diagram
- Phase lock loops
- I,Q diagram depicting true PLL phase error
- Frequency lock loops
- I,Q diagram depicting true frequency error

## Generic GPS receiver carrier tracking loop block diagram

- Carrier tracking loop description spread out over several block diagrams
  - Carrier synthesis hardware
  - Carrier then code wipe-off hardware
  - Predetection integration hardware
  - Baseband software
    - Carrier loop discriminator and filter
- Discriminator defines carrier loop type
  - Phase or frequency lock loop (PLL or FLL)

#### **Carrier tracking loops**

The description of the carrier tracking loop has been spread out over several block diagrams. These consist of the carrier wipe-off hardware, the code wipe-off hardware, the predetection integration hardware (some additional predetection integration may take place in the software), the baseband software which consists of the carrier loop discriminator and the carrier loop filter and finally the carrier synthesis hardware, which consists of the carrier NCO and the sine and cosine map functions. All of the component parts of the carrier tracking loop are shown in the next figure.

The carrier loop discriminator defines the type of carrier tracking loop as a PLL, a Costas PLL (which is a PLL discriminator that tolerates the presence of data modulation on the baseband signal), or a frequency lock loop (FLL). The PLL and the Costas loops are the most accurate but are more sensitive to dynamic stress than the FLL. The PLL and Costas loop discriminators produce phase errors at their outputs. The FLL discriminator produces a frequency error. Because of this, there is also a difference in the architecture of the loop filter, described in Part II. There is an additional integration in the FLL versus the PLL filter for the same loop filter order.

## Generic GPS receiver carrier tracking loop block diagram



## Baseband components of GPS carrier tracking loop (PLL, FLL)



### Designing PLL carrier tracking loop discriminators

- Phase lock loop (PLL) discriminators
- Common phase lock loop discriminators
- Comparison of PLL discriminators
- I,Q diagram depicting true PLL phase error

# Common phase lock loop discriminators

Discriminator	Output	Characteristics
algorithm	phase	(First four are data insensitive.
	error	Last is pure PLL)
Sign (I <sub>PS</sub> )*Q <sub>PS</sub>	sin (φ)	Decision directed Costas. Near optimal at high SNR. Slope proportional to signal amplitude A. Least computational burden.
I <sub>PS</sub> *Q <sub>PS</sub>	sin (2φ)	Costas. Near optimal at low SNR. Slope proportional to sig amplitude squared A <sup>2</sup> . Moderate computational burden.
Q <sub>PS</sub> /I <sub>PS</sub>	tan (φ)	Suboptimal but good at high and low SNR. Slope not signal amplitude dependent. Higher computational burden and must check for divide by zero error near ± 90 degrees.
ATAN (Q <sub>PS</sub> /I <sub>PS</sub> )	φ	Two-quadrant arctangent. Optimal (maximum likelihood estimator) at high and low SNR. Slope not signal amplitude dependent. Highest computational burden.
ATAN2 (Q <sub>PS</sub> , I <sub>PS</sub> )	φ	Four-quadrant arctangent. Optimal (maximum likelihood e estimator) at high and low SNR. Slope not signal amplitude dependent. Highest computational burden.

#### **Comparison of PLL discriminators**

The input/output relationships of the four PLL discriminators that are insensitive to data transitions in the previous table are plotted below. The true input error in degrees is plotted as the abscissa and the discriminator output error is plotted as the ordinate. Note that the output of all these discriminators repeat every 180 degrees (1/.2 cycle). The ATAN 2 four-quadrant pure PLL discriminator input/output characteristic looks like the two-quadrant ATAN discriminator input/output characteristic, except that it repeats every 360 degrees (cycle). Therefore both its input and output range are doubled. Because the input error range is double the ATAN 2 discriminator, the pure PLL discriminator has 6 dB more noise error tolerance.

The ideal input/output relationship is linear. Therefore, only the ATAN discriminator is optimal. All of the others are simply approximations to minimize the computational burden. As a result, their discriminator performance is suboptimal. Their advantages and limitations are summarized in the table below.

# Comparison of PLL discriminators



### PLL I, Q phasor diagram: Phase error between replica carrier and incoming carrier



# I,Q "fuzz ball" of PLL signal with data plus noise



### Pure phase lock loops

- Pure PLL discriminator provides 6 dB improvement but cannot be used with C/A or P(Y) code
  - 50 Hz data requires data insensitive PLL discriminator
  - Pure PLL can be used for data-less L2 P(Y) code, but this SV mode not likely to be turned on by Control Segment
- Data wipeoff can provide short term pure PLL mode a hold on by your teeth mode (HOBYT)
  - Receiver reads full navigation message after 25 iterations of the five subframes
  - Requires 12.5 minutes thereafter, data wipeoff works until SV message changes
  - Alternative: navigation message provided by external source

### Designing FLL carrier tracking loop discriminators

- Frequency lock loop (FLL) discriminators
- Common FLL discriminators
- Comparison of FLL discriminators
- I,Q diagram depicting true frequency error

### Frequency lock loops (FLLs)

- FLLs replicate frequency of SV carrier
- Also called automatic frequency control (AFC) loops
- GPS FLLs must be insensitive to 180-degree reversals in I and Q signals
- Sample times of I and Q signals should not straddle data bit transitions
- Receiver does not know phase of data transition boundaries during initial signal acquisition - FLL is less sensitive than PLL

# Common frequency lock loop discriminators

Discriminator algorithm	Output frequency error	Characteristics
$\frac{sign(dot) cross}{t_2 - t_1}$	$\frac{\sin{[2(\phi_2 - \phi_1)]}}{t_2 - t_1}$	Near optimal at high SNR. Slope proportional to signal amplitude A. Moderate computational burden.
where: $dot = I_{PS1}*I_{PS2} + Q_{PS1}*Q_{PS2}$ $cross = I_{PS1}*Q_{PS2} - I_{PS2}*Q_{PS1}$		
$\frac{cross}{t_2 - t_1}$	$\frac{\sin\left(\phi_2 - \phi_1\right)}{t_2 - t_1}$	Near optimal at low SNR. Slope proportional to signal amplitude squared A <sup>2</sup> . Least computational burden.
$\frac{ATAN2(cross, dot)}{(t_2 - t_1)360}$	$\frac{\Phi_2 - \Phi_1}{(t_2 - t_1)360}$	Four-quadrant arctangent. Maximum likelihood estimator. Optimal at high and low SNR. Slope not signal amplitude dependent. Highest computational burden.

# Comparison of FLL discriminators



### FLL I, Q phasor diagram: frequency error between replica carrier and incoming carrier





