The Abdus Salam International Centre for Theoretical Physics

United Nations Educational, Scientific and Cultural Organization

IAEA International Atomic Energy Agency

2025-8

Satellite Navigation Science and Technology for Africa

23 March - 9 April, 2009

Introduction to GPS Receiver Design Principals
(Part 5)

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Session V
Code and carrier loops filter design

- Loop filter overview
- First, second, and third order analog loop filters
- Loop filter design characteristics
- Replacing analog with digital integrators
- First, second, and third order digital loop filters
- Block diagrams of two FLL-assisted PLL filters
- Loop filter parameter design example

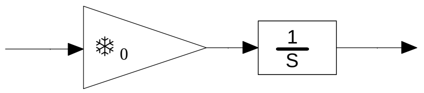
Loop filter overview

- Objective of loop filter is to reduce noise
  - Produce accurate estimate of original signal (without noise) at its output
- Loop filter's output signal used as an error signal that is fed back to the input stages (carrier replica and wipeoff, code replica and correlation) in a closed loop process
- Digital filter design approach draws on existing knowledge of analog loop filters, then adapts these into digital implementations

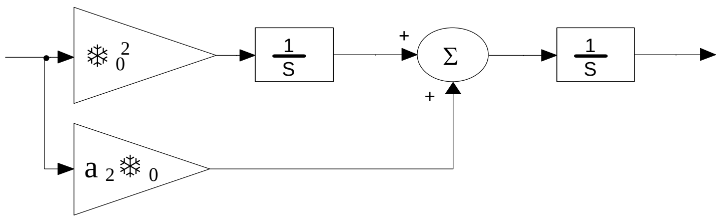
First, second and third order analog loop filters

The figure below shows block diagrams of first, second and third order analog filters. Analog integrators are represented by 1/s, the Laplace transform of the time domain integration function. The number of integrators determine the loop filter order. The first order loop filter has one integrator, etc. The input signal is multiplied by the multiplier coefficients, then processed as shown in the figure. These multiplier coefficients and the number of integrators completely determine the loop filter's characteristics.

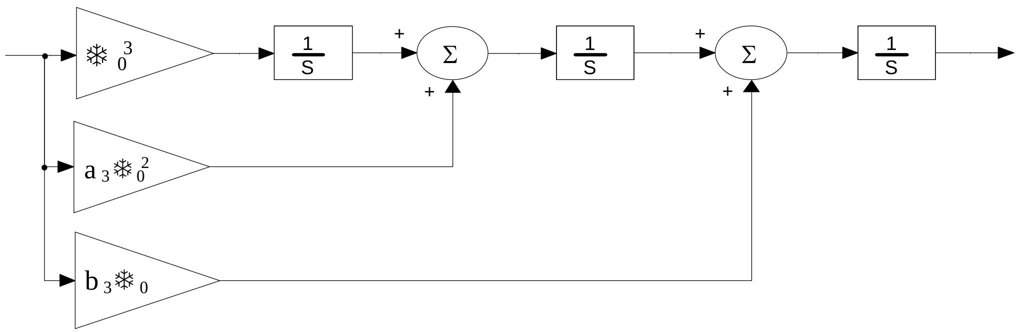
First, second, and third order analog loop filters



(a) First order analog filter.



(b) Second order analog filter.



(c) Third order analog filter.

Loop filter design characteristics

The table below summarizes the filter characteristics and provides all the information required to compute the filter coefficients for first, second or third order loop filters. Only the filter order and noise bandwidth must be determined to complete the design.

Notes: (1)The loop filter natural radian frequency, ω_o, is computed from the value of the loop filter noise bandwidth, B_n, selected by the designer. (2) R is the line-of-sight range to the satellite. (3) The steady state error is inversely proportional to the tracking loop bandwidth and directly proportional to the nth derivative of range, where n is the loop filter order.

Loop filter design characteristics

Loop order	Noise bandwidth B_n (Hz)	Typical filter values	Steady state error	Characteristics
First	$\frac{\omega_o}{4}$	ω_o $B_n = 0.25\ \omega_o$	$\frac{(dR/dt)}{\omega_o}$	Sensitive to velocity stress. Used in aided code loops. Unconditionally stable at all noise bandwidths.
Second	$\frac{\omega_o(1 + a_2^2)}{4a_2}$	ω_o^2 $a_2\ \omega_o = 1.414\ \omega_o$ $B_n = 0.53\ \omega_o$	$\frac{(d^2R/dt^2)}{\omega_o^2}$	Sensitive to acceleration stress. Used in aided and unaided carrier loops. Unconditionally stable at all noise bandwidths.
Third	$\frac{\omega_o(a_3b_3^2 + a_3^2 - b_3)}{4(a_3b_3 - 1)}$	ω_o^3 $a_3\ \omega_o^2 = 1.1\ \omega_o^2$ $b_3\ \omega_o = 2.4\ \omega_o$ $B_n = 0.7845\ \omega_o$	$\frac{(d^3R/dt^3)}{\omega_o^3}$	Sensitive to jerk stress. Used in unaided carrier loops. Remains stable at $B_n \leq 18$ Hz.

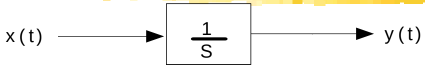
Replacing analog with digital integrators

The figure below depicts the block diagram representations of analog and digital integrators. The analog integrator of Figure (a) operates with a continuous time domain input, $x(t)$, and produces an integrated version of this input as a continuous time domain output, $y(t)$. Theoretically, $x(t)$ and $y(t)$ have infinite numerical resolution and the integration process is perfect. In reality, the resolution is limited by noise which significantly reduces the dynamic range of analog integrators. There are also problems with drift.

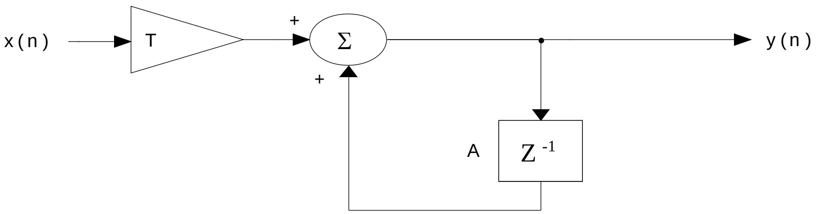
The boxcar digital integrator of Figure (b) operates with a sampled time domain input, $x(n)$, which is quantized to a finite resolution, and produces a discrete integrated output, $y(n)$. The time interval between each sample, T, represents a unit delay, z^{-1}, in the digital integrator. The digital integrator performs discreet integration perfectly with a dynamic range limited only by the number of bits used in the accumulator, A. This provides a dynamic range capability much greater than can be achieved by its analog counterpart and the digital integrator does not drift. The boxcar integrator performs the function $y(n) = T[x(n)] + A(n-1)$, where n is the discreet sample sequence number.

Figure (c) depicts a digital integrator which linearly interpolates between input samples and more closely approximates the ideal analog integrator. This is called the bilinear z-transform integrator. It performs the function $y(n) = T/2[x(n)] + A(n-1) = 1/2[A(n) + A(n-1)]$.

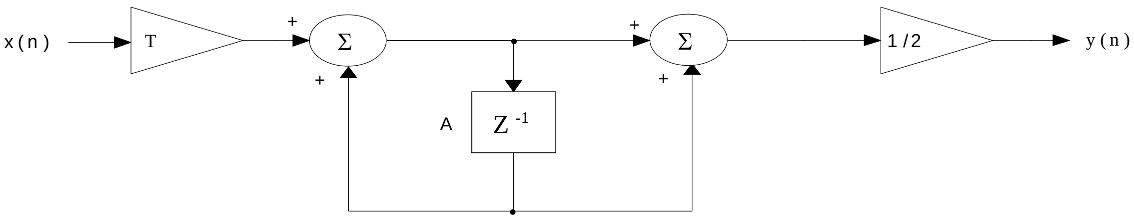
Replacing analog with digital integrators



(a) Analog integrator



(b) Digital boxcar integrator

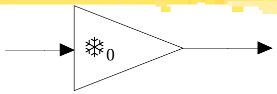


(c) Digital bilinear transform integrator

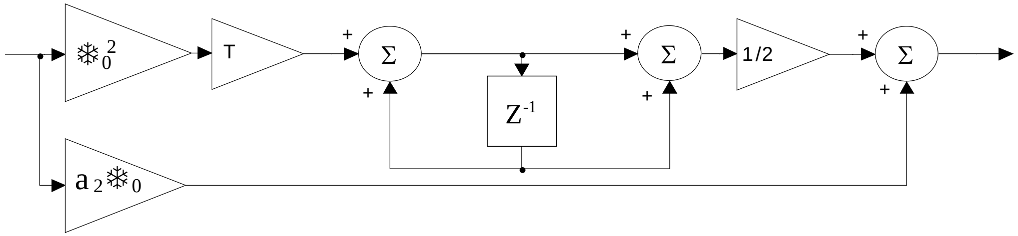
Block diagram of three digital loop filters

The digital filters depicted in the figure below result when the Laplace integrators of the analog loop filters shown in the earlier figure are replaced with bilinear z-transform integrators. The last digital integrator, which is the NCO, is not shown to emphasize the fact that the NCO is implemented separately from the programmable loop filter. The NCO is characterized as a boxcar integrator

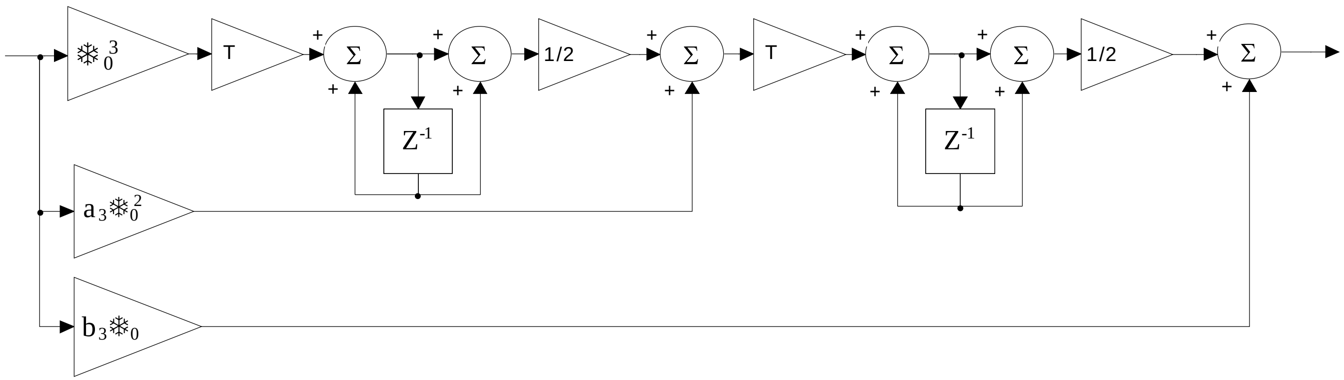
First, second, and third order digital loop filters



(a) First order digital filter.



(b) Second order digital filter.

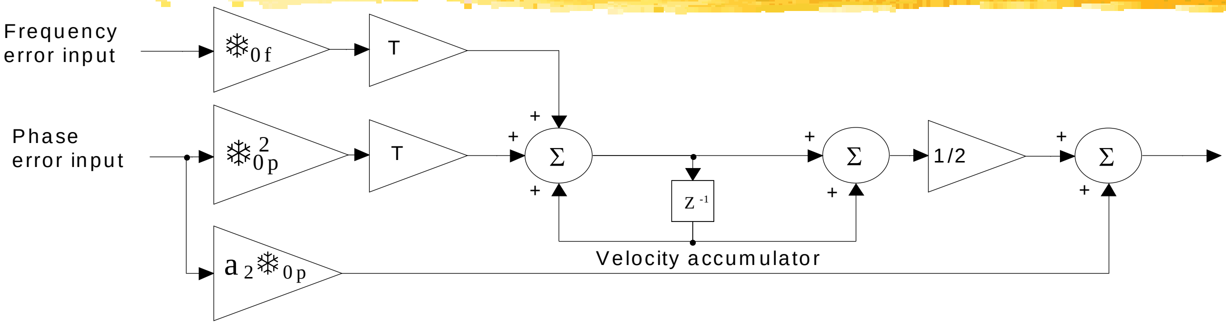


(c) Third order digital filter.

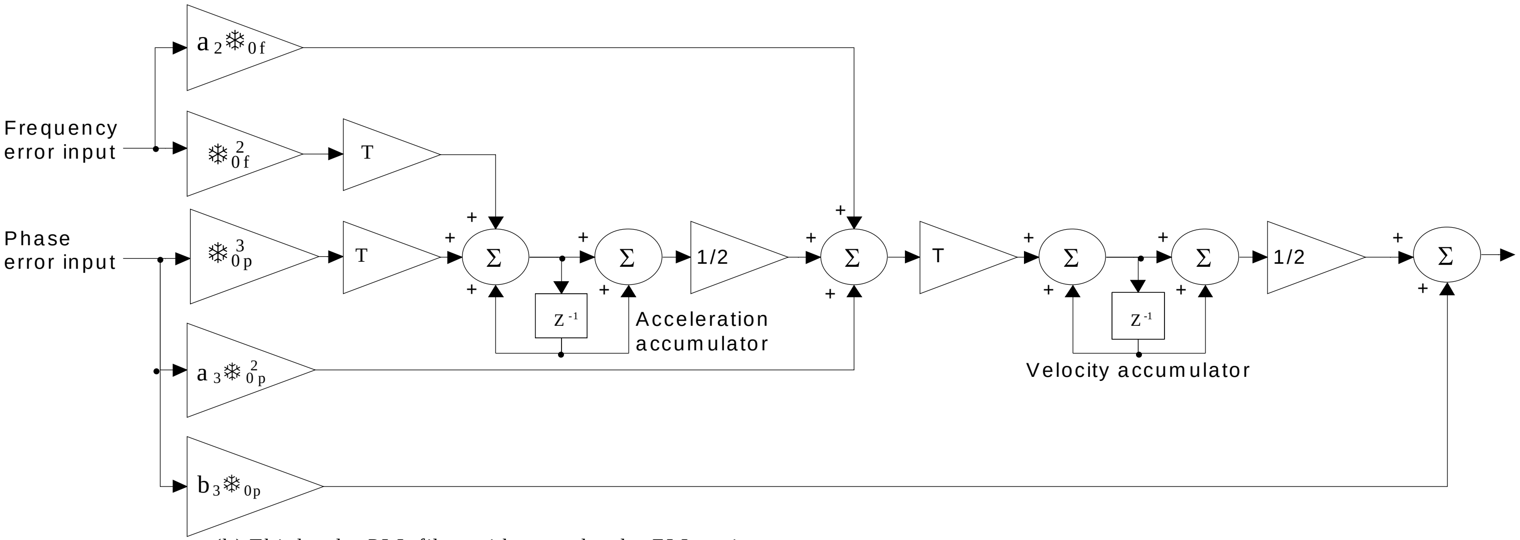
Block diagrams of two FLL-assisted PLL filters

The figure below illustrates two FLL assisted PLL loop filter designs. Figure (A) depicts a second order PLL filter with a first order FLL assist. Figure (B) depicts a third order PLL filter with a second order FLL assist. If the PLL error input is zeroed in either of these filters, the filter becomes a pure FLL. Similarly, if the FLL error input is zeroed, the filter becomes a pure PLL. The typical loop closure process is to close in pure FLL, then apply the error inputs from both discriminators as an FLL assisted PLL until phase lock is achieved, then convert to pure PLL until phase lock is lost. In general, the natural radian frequency of the FLL, ❄$_{of}$, is different from the natural radian frequency of the PLL, ❄$_{op}$. These natural radian frequencies are determined from the desired loop filter noise bandwidths, B_{nf} and B_{np}, respectively. The values for the second order coefficient a_2 and third order coefficients a_3 and b_3 can be determined from the table of loop filter characteristics shown earlier. These coefficients are the same for FLL, PLL or DLL applications if the loop order and the noise bandwidth, B_n, are the same. Note that the FLL coefficient insertion point into the filter is one integrator back from the PLL and DLL insertion points. This is because the FLL error is in units of Hz (change in range per unit of time), whereas the PLL and DLL errors are in units of phase (range).

Block diagrams of two FLL-assisted PLL filters



(a) Second order PLL filter with first order FLL assist.



(b) Third order PLL filter with second order FLL assist.

Loop filter parameter design example

- Assume selection of third order loop because it is insensitive to acceleration stress
  - Minimize sensitivity to jerk stress by choosing widest possible noise bandwidth, consistent with stability: B_n = 18 Hz
- For noise bandwidth, B_n = 18 Hz
  - $\omega_o = B_n/0.7845 = 22.94455$ radians/s
  - Multipliers: $\omega_o^3 = 12079.214$, $a_3\,\omega_o^2 = 1.1\,\omega_o^2 = 579.098$, $b_3\,\omega_o = 2.4\,\omega_o = 55.067$
  - For 200 Hz loop iteration rate: $T = 0.005$ s

Session VI - Code