The Abdus Salam
International Centre for Theoretical Physics

United Nations Educational, Scientific and Cultural Organization

IAEA International Atomic Energy Agency

Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis

26 October – 20 November 2009

Trieste – Italy

The Abdus Salam International Centre for Theoretical Physics (ICTP) will organize the above mentioned course, to be held at ICTP, Trieste, Italy, from 26 October to 20 November 2009. Drs. Nizar Abdallah (Actel Corp.), Alessandro Marchioro (CERN) and Andres Cicuttin (ICTP) will direct the Course. Dr. Maria Liz Crespo (ICTP) will be in charge of the laboratory activity. Experienced tutors will guide and assist participants during the laboratory sessions. The course will count on prestigious lecturers from Universities, Industry and Research Institutions.

SUMMARY AND PURPOSE

This Course is intended as an advanced training activity in Microelectronics, to introduce physicists, engineers and computer scientists to state-of-the-art design methodologies for Programmable Logic Devices (PLD). Emphasis will be placed on electronic system development with Field Programmable Gate Arrays (FPGA) using a Hardware Description Language, VHDL, as cost effective solution for research and training in microelectronics. With recent PLD architectural evolutions and ever-increasing capacity, it is today possible and affordable to implement all elements of a digital design within an FPGA device. FPGAs are becoming very attractive for cost-effective system prototyping based on advantages such as low cost or free of charge design tools, flexible design cycle, virtually unlimited re-configurability, extreme versatility and performance, and the ability to easily implement and evaluate alternative design architectures. These financial and technological advantages are increasingly attracting the attention of experimental physicists, electronic engineers and computing scientists who see FPGAs as an affordable solution for implementing high performance designs in areas such as: Scientific Instrumentation, Telecommunications, Data Acquisition, Digital Signal Processing, Reconfigurable Computing, etc.

The purpose of this activity is to provide training in the latest FPGA design methodologies based on hardware description languages and logic synthesis. It will also be offered a broad view of modern integrated circuits and VLSI design. This course offers a unique opportunity to get into the FPGA world from basic to complex aspects through its intensive program, from step-by-step tutorials to implementation of fairly complex projects.

Some of the topics to be covered will include:

- **FPGA**: Technologies, Architectures, Design Methodology and Design Flow, Debugging Techniques
- **VHDL**: Modeling and Simulation, VHDL for Synthesis
- **Digital System Design**: combinational and sequential circuits. Digital Arithmetic
- **Digital Signal Processing**: Fourier Theory, Sampling Theory, Digital filters
- **Reuse methodology for System-on-a-Chip Designs**
- **Introduction to CMOS technology and VLSI design**
- **Reconfigurable Virtual Instrumentation based on FPGA**
- **Hands-on Laboratory Exercises**: VHDL Modeling, Simulation and FPGA Design
- **Actel**: Mixed signal analog-digital FPGA design

PARTICIPATION

Scientists, technologists, teachers and students from countries that are members of the United Nations, UNESCO or IAEA may attend the Course. As the Course will be conducted in English, participants must have a good working knowledge of that language. A basic knowledge of digital electronics is also required.

As a rule, travel and subsistence expenses of the participants are borne by the home institution. However, limited funds are available for some participants from, and working in, developing countries, to be selected by the organizers. Such financial support is available only for those who attend the entire activity. Every effort should be made by candidates to secure support for their fare (or at least half fare) from their home country. **There is no registration fee to attend the Course**.

HOW TO APPLY FOR PARTICIPATION

The application form can be accessed at the activity website http://agenda.ictp.it/smr.php?2065
Once in the website, comprehensive instructions will guide you step-by-step, on how to fill out and submit the application form.

ACTIVITIY SECRETARIAT:

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E-mail: smr2065@ictp.it ICTP Home Page: http://www.ictp.it/

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Directors

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Laboratory Sessions led by

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ICTP, Trieste, Italy

DEAD LINE
for submitting applications

8 June 2009