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Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis | (smr 2065)

Tuesday 27 October 2009

Sinthesis I - Introduction to VHDL - Adriatico Guest House Kastler Lecture Hall (12:00-13:00)

time title	presenter
12:00 Sinthesis I - Introduction to VHDL	N. ABDALLAH