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Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis | (smr 2065)

Monday 16 November 2009

Laboratory Session: Digital Signal Processing with FPGA. A design example. - Adriatico Guest House Informatics Lab. (16:00-18:00)

time	title	presenter
16:00	Laboratory Session: Digital Signal Processing with FPGA. A design example.	C. SOSA PAEZ