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Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis | (smr 2065)

Wednesday 28 October 2009

(LiberoTM IDE) Timing Constraints and Analysis - Adriatico Guest House Kastler Lecture Hall (17:00-18:00)

time	title	presenter
17:00	(LiberoTM IDE) Timing Constraints and Analysis	N. ABDALLAH