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Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis | (smr 2065)

Friday 30 October 2009

Laboratory Session. VHDL Behavioral Description and Simulation of Sequential Circuits. - Adriatico Guest House Informatics Lab. (14:30-15:30)

time	title	presenter
14:30	Laboratory Session. VHDL Behavioral Description and Simulation of Sequential Circuits.	M.L. CRESPO