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Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis | (smr 2065)

Monday 02 November 2009

Laboratory Session. Laboratory Session. Finite State Machine: VHDL Description and Simulation (cont.) - Adriatico Guest House Informatics Lab. (14:30-15:30)

time	title	presenter
14:30	Laboratory Session. Laboratory Session. Finite State Machine: VHDL Description and Simulation (cont.)	M.L. CRESPO